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The limiting performance of a CMOS bistable register based on waveform considerations

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The fundamental latching behaviour of a CMOS bistable register is described. The circuit response of two cross coupled NAND gates being driven by a data and a clock signal can be decomposed into four individual regions of operation. Closed form small signal solutions for each region of operation are described and favourably compared with SPICE. The third region of operation contains the closed loop regenerative mode of operation inherent to the bistable NAND gate configuration and fundamental to the latching behaviour of a register. From these results, necessary and sufficient conditions for latching data into a bistable register are developed. Finally, from these necessary and sufficient conditions, the limiting condition for latching is presented and verified by SPICE.

1. Introduction

The specific emphasis of this paper is the analysis of the fundamental limitations of moving data through a synchronous digital system. The minimum functional requirement of all synchronous digital systems is the ability to latch data into a register element. A fundamental form of a register element is the bistable latch configuration which can be constructed from either two NAND gates or two NOR gates. Either circuit performs the basic latching operation upon which other more complicated types of latches and registers can be constructed.

Previous work in this area has focused on the design of sense amplifiers in memory circuits. In early work (Lynch and Boll 1974) an optimal waveform shape for latching data into a two transistor (with pull-ups) sense amplifier cell is derived. Recently, this work was extended by considering effects such as capacitive coupling on the waveform shape required for latching data in a DRAM sense amplifier (Yuan and Liou 1990). In this paper, however, the optimal latching requirements of a different, though related, and very common circuit structure, a CMOS bistable register, is described. Some relevant research analysing this type of latch circuit and its response due to non-step input waveforms has been performed while studying metastability (Jackson and Albicki 1989, Kacprzak 1988, Kacprzak and Albicki 1987, Calvo *et al.* 1991, Liu and Gallagher 1977, Kim *et al.* 1989, Horstmann *et al.* 1989, Rosenberger and Molnar 1992). This paper differs from this related research on metastability in that necessary and sufficient conditions for latching data into a bistable register are determined, not the point at which a register enters the metastable state.

The basic circuit configuration of the bistable NAND gate latch is described in § 2 of this paper. An overview of the circuit operation of the CMOS bistable latch driven by clock and data ramp signals is discussed in § 3. The circuit behaviour of the latch can be broken up into four separate regions of operation. Each of these regions

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is analysed in detail, and small signal closed form solutions of the output response for each region are given in § 4. The closed loop regenerative latch behaviour occurs in the third region of operation. This permits the development of necessary and sufficient conditions for latching data into a register. From these conditions, the fundamental limiting condition for latching data into a CMOS bistable register is presented and experimentally verified. These are described in § 5 of this paper. Finally, some concluding remarks are made in § 6.

2. Bistable NAND gate configuration

The cross coupled NAND gate implementation of the bistable latch, shown in Fig. 1, has been chosen instead of the NOR gate version, since its response in CMOS technology is faster (due to the higher mobilities of the serial N-channel devices than that of the serial P-channel devices) and is therefore more commonly used. However, all physical theory and algorithmic solutions described in this paper are easily applied to a cross coupled NOR gate implementation of the CMOS bistable register.

A CMOS implementation of the bistable NAND gate structure has been chosen to evaluate how data is fundamentally performance limited by the ability to latch data into a register. The CMOS bistable register circuit is shown in Fig. 2. The clock signal drives the input of one NAND gate (labelled 'A' in Fig. 2); the data signal is the input to the second NAND gate (labelled 'B' in Fig. 2). The other input of each NAND gate is furnished by the output signal of its complementary NAND gate. Given an initial voltage at V_1 and its complement at V_2, the input data and clock signal are chosen so as to maintain or flip the output logic states. Once the new state of the register is reached and a set of necessary and sufficient conditions for latching is satisfied, the input data signal is considered to have been latched into the register.

3. Latching of data into register

In order to latch data into a register, the clock and data signals must appear at the inputs of the register at their correct relative times and voltage magnitudes. These time and voltage requirements are described in analytical form in §§ 4 and 5 of this paper. In this analysis, the input clock and data waveforms have been assumed to behave as ramp signals, not as step inputs, in order to describe more accurately the register latching characteristics in terms of the data and clock input signal waveforms of the bistable register.

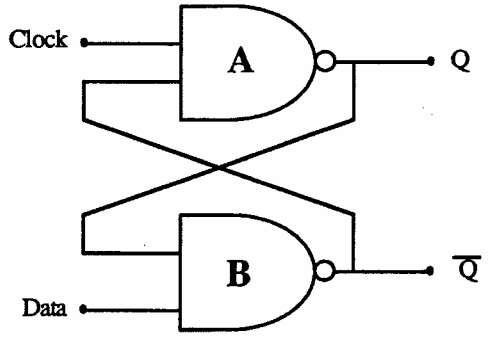

Figure 1. Bistable NAND gate circuit configuration.

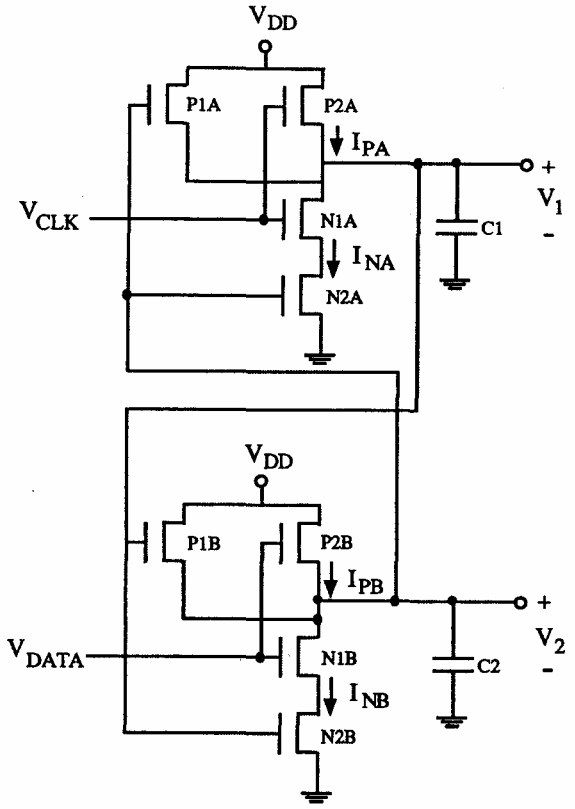

Figure 2. CMOS implementation of bistable register.

The initial conditions of $V_1(0)=0\,V$ and $V_2(0)=5\,V$ have been chosen to exemplify the latching phenomenon. Assuming the clock signal, V_{CLK}, is at 5 V and the data signal, V_{DATA}, is at 0 V, the circuit is in a restoring equilibrium state. In order to change the polarity of the output voltages at V_1 and V_2, both the clock and data input signals must switch. The clock signal must decrease from 5 V, and the data signal must increase from 0 V.

As shown in Fig. 2, as V_{CLK} decreases from V_{DD} to $V_{DD}+V_{TP}$, where V_{DD} is the power supply voltage and V_{TP} is the threshold voltage of the P-channel device, no current will flow in the top device since both of the P-channel devices remain cut-off. Once V_{CLK} equals $V_{DD}+V_{TP}$, P_{2A} turns on and enters the saturation region. This permits current to flow within the top NAND gate. Once I_{PA} becomes greater than I_{NA}, V_1 will increase. When V_1 equals V_{TN}, the threshold voltage of the N-channel device, the lower N-channel device of the lower NAND gate turns on. If V_{DATA} is greater than V_{TN} of the top device plus V_{DS} of the lower device, the lower NAND gate will also conduct current. Assuming these conditions exist and V_{CLK} continues to decrease (thereby increasing V_1), the bistable NAND gate register will enter the regenerative latch mode. Thus, as V_1 increases above V_{TN} and assuming V_{DATA} remains above V_{TN}, the N-channel tree of the lower device will sink current to ground. Once I_{NB}, shown in Fig. 2, becomes greater than I_{PB}, V_2 will decrease from

its equilibrium potential of V_{DD} volts. As V_2 decreases below $V_{DD}+V_{TP}$, P_{1A} turns on, and this further accelerates the rising voltage at V_1, which in turn further decreases V_2. This closed loop regenerative action permits the bistable register to respond quickly to its changing input signals and to latch the input data, and in effect to change the state of the register. As V_1 increases toward V_{DD}, V_{DS} across both of the P-channel devices becomes very small, and the amount of output voltage change caused by a change in input voltage decreases until the regenerative loop is broken. The final region of operation is a non-regenerative open loop in which the P-channel devices charge the output capacitor C_1 up to V_{DD}. These four regions of operation are quantitatively described in the following section.

4. Regions of operation of bistable register

The response of the bistable register to its changing input signals can be decomposed into four separate regions. Each region describes the bistable register operating under different circuit conditions, and therefore each regional output is different.

Region 1

As V_{CLK} decreases from V_{DD} to $V_{DD}+V_{TP}$, no current can flow through the upper NAND gate (see Fig. 3) since: (1) both P-channel devices are cut-off, P_{2A} due to $V_{CLK} \geq V_{DD}+V_{TP}$ and P_{1A} due to $V_2 \geq V_{DD}+V_{TP}$; and (2) V_1 is at the same potential as the sources of the two N-channel devices. Thus, Region 1 represents the time required for V_{CLK} to reach $V_{DD}+V_{TP}$ and turn on P_{2A}, thereby permitting current to flow. Throughout this region, V_1 remains at 0 V, as shown in Fig. 4, and the time delay, T_1, of this region is given by (1).

$$T_1 = \left| \frac{V_{TP}}{k_c} \right| \tag{1}$$

where the clock signal deceases at k_c volts per second and V_{TP} is negative for an enhancement mode P-channel device.

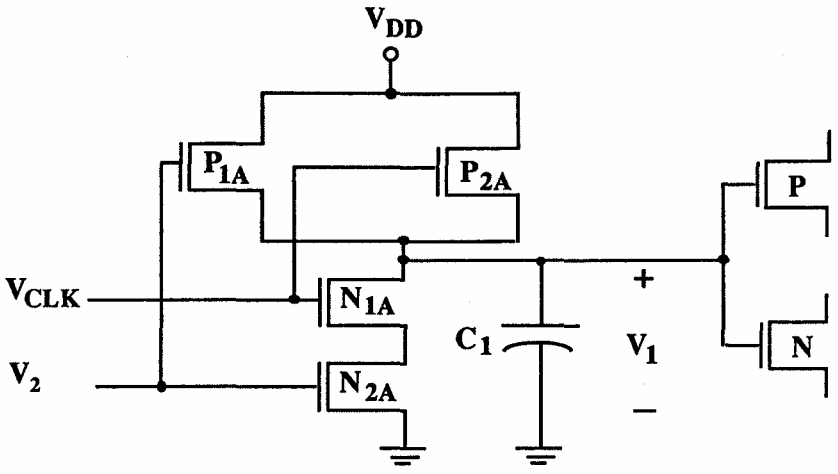

Figure 3. Circuit diagram of upper NAND gate in Region 1.

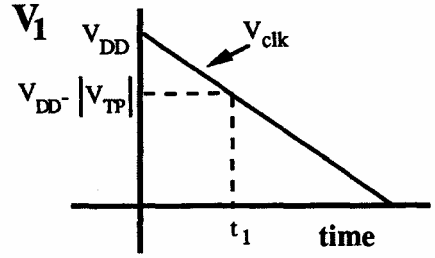

Figure 4. Region 1 timing diagram.

Region 2

Once V_{CLK} decreases below $V_{DD}+V_{TP}$, current will flow between V_{DD} and ground. As V_{CLK} decreases further, the current supplied by P_{1A} will become greater than the current sunk by the N-channel tree. Once this occurs, $V_1(t)$ will begin to rise. In this region, the bistable NAND gate register can be represented by a single NAND gate with one changing input (since $V_2 = V_{DD}$), as shown in Fig. 5. The circuit depicted in Fig. 5 can be represented by the small signal model shown in Fig. 6, where v_c represents the incremental change in V_{CLK} and v_1 represents the incremental change in V_1.

From this model, $V_1(t)$ can be determined for a ramp input clock signal decreasing at a rate of $k_c\,\mathrm{V\,s^{-1}}$. $V_1(t)$ for Region 2 is given by

$$V_1(t)=k_c\frac{AC_1}{B^2}\left[\exp\left(-Bt/C_1\right)+\frac{Bt}{C_1}-1\right] \tag{2}$$

Note that $V_1(t)$ increases from 0 V and terminates at V_{TN} volts within this region, as shown in Fig. 7. Since region 2 ends once V_1 reaches V_{TN}, and assuming V_{DATA} remains greater than V_{TN}, the circuit will enter the regenerative region of operation. A and B represent the transconductance and output conductance of the single NAND gate in Region 2, respectively, and are given by (3) and (4):

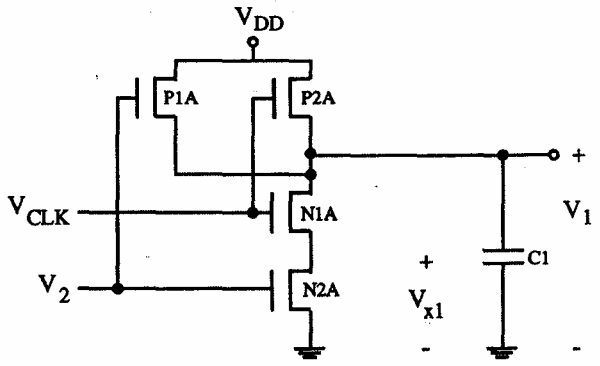

Figure 5. Region 2 circuit configuration.

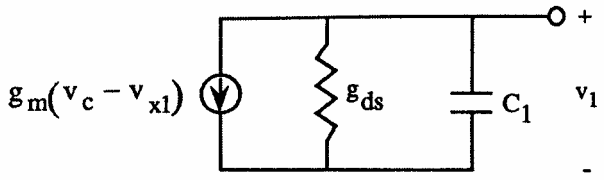

Figure 6. Small signal model of Region 2.

$$A = g'_m + g_{mp} - \frac{g'_m g_{mn}}{g_{n1} + g_{n2} + g_{mn}} \tag{3}$$

$$B = g_{ds} - \frac{g'_m g_{n1}}{g_{n1} + g_{n2} + g_{mn}} \tag{4}$$

where

$$g'_m = \frac{g_{mn} g_{n2}}{g_{n1} + g_{n2}} \tag{5}$$

$$g_{ds} = \frac{g_{n1} g_{n2}}{g_{n1} + g_{n2}} \tag{6}$$

The terms g_{mn} and g_{mp} represent the transconductance of the N-channel tree and the P-channel tree, respectively, when driven by the input clock signal. The terms g_{n1} and g_{n2} are the output conductances of the two serial N-channel transistors.

The operating point for Region 2 from which the small signal parameter values can be derived is approximately halfway between 0 and V_{TN}, as shown in (7). V_{x1}, the potential at the common source/drain node between N_{1A} and N_{2A} (see Fig. 5), which is used to determinine the values of the small signal parameters, is provided in (8).

$$V_1 = (\text{Region 2 operating point}) \approx \frac{V_{TN}}{2} \tag{7}$$

$$V_{x1} = \frac{(V_{CLK} - V_{TN}) + (V_2 - V_{TN})}{2} - \left(\frac{[(V_{CLK} - V_{TN}) + (V_2 - V_{TN})]^2}{4} - (V_{CLK} - V_{TN}) V_1 + \frac{V_1^2}{2} \right)^{1/2} \tag{8}$$

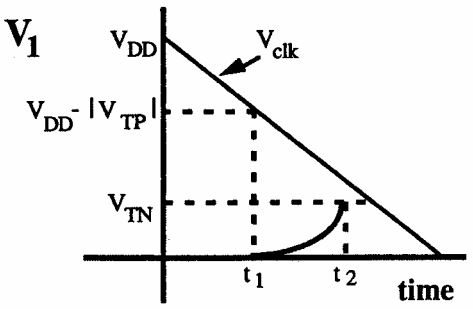

Figure 7. Region 2 timing diagram.

Note that $V_2 = V_{DD}$ and $V_{CLK} = V_{DD} + 2V_{TP}$ around the operating point of $V_1 = V_{TN}/2$. From the above information, the process dependent parameters K'_p and K'_n, and the geometric W/L ratios of each of the P- and N-channel transistors, the output response $V_1(t)$ of Region 2 for a decreasing ramp clock input signal can be determined.

Region 3

Once V_1 reaches V_{TN} volts, N_{2B} is turned on (see Fig. 2). If V_{DATA} is also greater than V_{TN} of the top N-channel device plus V_{DS} of the lower N-channel device, N_{1B} will also turn on; with both on, current can flow between V_{DD} and ground. At a specific point in time, depending upon the magnitude of V_{DATA} and V_1 and the relative transistor device characteristics, the N-channel tree will sink more current than the P-channel tree will source. At this point, $V_2(t)$ will decrease from V_{DD} volts. Once V_2 decreases below $V_{DD} + V_{TP}$, P_{1A} will turn on and source additional current, furthering the rate of increase of V_1. This in turn will improve the ability of the N-channel tree of the lower NAND gate to sink more current, further decreasing V_2. Herein lies the closed loop regenerative mode of operation inherent to the bistable NAND gate circuit configuration and fundamental to the latching behaviour of a register. Note that the circuit is a two time constant system.

At a certain operating point, the data will be fully latched into the register and the clock input signal can be returned to V_{DD} and the state of the register will still enter its correct state ($V_1 = V_{DD}$ and $V_2 = 0$). This irreversible latching point represents the limiting ability to latch data into a register and is further described in § 5 of this paper.

The circuit configuration of Region 3 is shown in Fig. 8. This regenerative circuit can be represented by the small signal models depicted in Figs 9 and 10, where Fig. 9 represents the small signal model for the upper NAND gate, A, and Fig. 10 represents the small signal model for the lower NAND gate, B.

In the regenerative mode of Region 3 with a constantly decreasing clock input signal, $V_1(t)$ is composed of three terms (as shown in (9)): one due to the initial

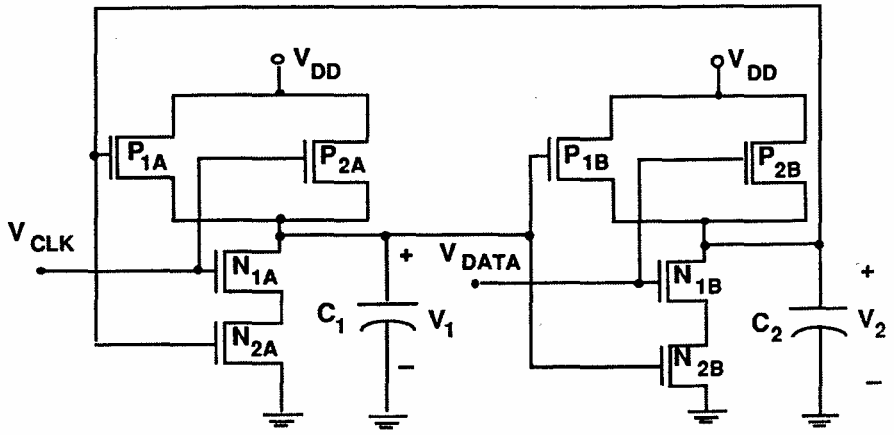

Figure 8. Circuit diagram of Region 3.

condition of Region 3, $V_{23}(0)$; one due to the input clock signal; and the third due to the input data signal.

$$V_1(t)=V_{1A}+V_{1C}+V_{1D} \tag{9}$$

Each term is described individually below:

$$V_{1A}(t)=V_{23}(0)[R_{1A}+R_{2A}+R_{3A}] \tag{10}$$

$$R_{1A}=\frac{(\alpha_1-D)\exp(-\alpha_1 t)}{\alpha_1(\alpha_2-\alpha_1)} \tag{11}$$

$$R_{2A}=\frac{(\alpha_2-D)\exp(-\alpha_2 t)}{\alpha_2(\alpha_1-\alpha_2)} \tag{12}$$

$$R_{3A}=\frac{D}{\alpha_1\alpha_2} \tag{13}$$

$$V_{1C}(t)=\frac{-A_2k_c}{C_1}\left[[(R_{1C}+R_{2C}+R_{3C})U(t)]-(R_{1C}+R_{2C}+R_{3C})\Big|_{t=E/k_c}U\left(t-\frac{E}{k_c}\right)\right] \tag{14}$$

$$R_{1C}=\frac{(D-\alpha_1)\exp(-\alpha_1 t)}{\alpha_1^2(\alpha_2-\alpha_1)} \tag{15}$$

$$R_{2C}=\frac{(D-\alpha_2)\exp(-\alpha_2 t)}{\alpha_2^2(\alpha_1-\alpha_2)} \tag{16}$$

$$R_{3C}=\frac{\alpha_1\alpha_2(1+Dt)-D(\alpha_1+\alpha_2)}{\alpha_1^2\alpha_2^2} \tag{17}$$

$$V_{1D}(t)=\frac{-A_1B_1k_D}{C_1C_2}\left[[(R_{1D}+R_{2D}+R_{3D})U(t)]-(R_{1D}+R_{2D}+R_{3D})\Big|_{t=E/k_D}U\left(t-\frac{E}{k_D}\right)\right] \tag{18}$$

$$R_{1D}=\frac{\exp(-\alpha_1 t)}{\alpha_1^2(\alpha_2-\alpha_1)} \tag{19}$$

$$R_{2D}=\frac{\exp(-\alpha_2 t)}{\alpha_2^2(\alpha_1-\alpha_2)} \tag{20}$$

$$R_{3D}=\frac{\alpha_1\alpha_2 t-(\alpha_1+\alpha_2)}{\alpha_1^2\alpha_2^2} \tag{21}$$

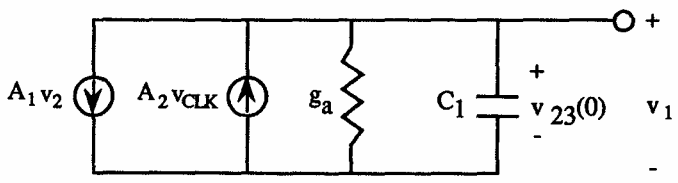

Figure 9. Small signal model of Device A in Region 3.

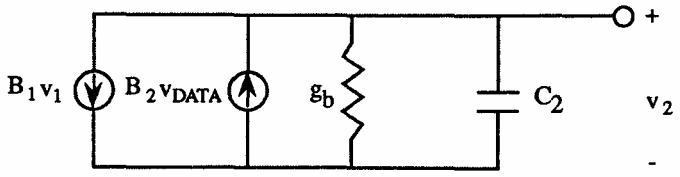

Figure 10. Small signal model of Device B in Region 3.

$$D=\frac{g_b}{C_2} \tag{22}$$

$$\alpha_1=\frac{-\left(\frac{g_a}{C_1}+\frac{g_b}{C_2}\right)+Q}{2} \tag{23}$$

$$\alpha_2=\frac{-\left(\frac{g_a}{C_1}+\frac{g_b}{C_2}\right)-Q}{2} \tag{24}$$

$$Q=\left[\left(\frac{g_a}{D_1}\right)^2+\left(\frac{g_b}{C_2}\right)^2-2\frac{g_a g_b}{C_1C_2}+4\frac{A_1B_1}{C_1C_2}\right]^{1/2} \tag{25}$$

where $V_{23}(0)$ is the initial condition of Region 3 and k_c (k_D) is the rate of change of the input clock (data) signal. Thus, (9)-(25) represent the output voltage across C_1, $V_1(t)$, when operating in the closed loop regenerative mode during Region 3. Figure 11 describes the $V_1(t)$ waveform in Region 3.

Each of the transconductance and output conductance terms shown in Figs 9 and 10 require definition. A_1 and B_1 represent the transconductance of the two feedback output voltages, V_2 and V_1, respectively. A_2 and B_2 are the transconductances of the input clock and data signals, respectively. A_1, B_1, A_2 and B_2 are shown below in (26)-(29) in terms of their small signal parameters.

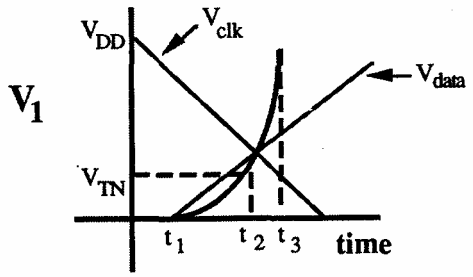

Figure 11. Region 3 timing diagram.

$$V_1(t) = V_{DD} - [V_{DD} - V_{34}(0)] \exp(-g_{a4}t/C_1) \tag{35}$$

where

$$g_{a4} = g_{p1a} + g_{p2a} \tag{36}$$

Equation (37) gives the approximate operating point for Region 4 at which the small signal parameters, g_{p1a} and g_{p2a}, should be derived and V_{x1} is provided by (38):

$$V_1 \text{ (Region 4 operating point)} \cong V_{DD} + \frac{V_{TP}}{2} \tag{37}$$

$$V_{x1} = \frac{(V_{CLK} - V_{TN}) + (V_2 - V_{TN})}{2} - \left\{ \frac{[(V_{CLK} - V_{TN}) + (V_2 - V_{TN})]^2}{4} - \frac{(V_{CLK} - V_{TN})^2}{2} \right\}^{1/2} \tag{38}$$

Register output waveform

Figure 13 shows the output voltage waveform at node V_1 of the bistable register for an input clock signal decreasing at $1\,V\,ns^{-1}$ and a data signal increasing at $1\,V\,ns^{-1}$, skewed from the clock signal, $T_{D\text{-}C}$, by 1 ns. This analytically derived output waveform has been compared to a waveform generated from the SPICE circuit simulator program (Nagel 1975) using Level 1 Shichman-Hodges device equations (Shichman and Hodges 1968) with the same circuit, geometric, and process characteristics. Close agreement within each region is apparent. A BASIC program which generates the output waveform for any clock signal fall time, data signal rise time, data-to-clock timing skew, as well as K'_p, K'_n and geometric W/L ratio was developed to calculate the bistable register output response.

5. Conditions for latching

As mentioned above, necessary and sufficient conditions must be satisfied to latch data irreversibly into a bistable register. This latch condition, which occurs in Region 3, permits the development of fundamental limiting relationships that define, for a given combination of clock and data input signals, K'_p, K'_n, $(W/L)_n$ and $(W/L)_p$ parameters, whether the bistable register will latch. Once a register has irreversibly latched, the clock signal can be returned to V_{DD} and still the register will maintain its correct state. This is the minimum required time for a CMOS bistable register to latch, assuming a given set of input, geometric, and process conditions.

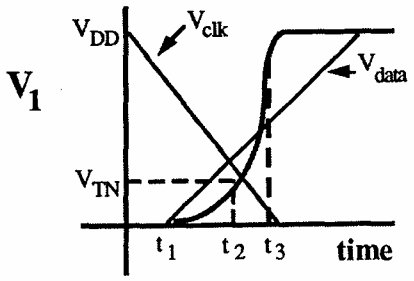

Figure 12. Region 4 timing diagram.

$$A_1 = \frac{g_{mn1a} g_{mn2a}}{g_{n2a} + g_{mna1}} - g_{mp1a} \tag{26}$$

$$B_1 = \frac{g_{mn1b} g_{mn2b}}{g_{n2ba} + g_{mnb1}} - g_{mp1b} \tag{27}$$

$$A_2 = \frac{g_{mn1a} g_{n2a}}{g_{mn1a} + g_{n2a}} - g_{mp2a} \tag{28}$$

$$B_2 = \frac{g_{mn1b} g_{n2b}}{g_{mn1b} + g_{n2b}} - g_{mp2b} \tag{29}$$

The output conductances of device A and device B are given in (30) and (31):

$$g_a = 0 \tag{30}$$

$$g_b = g_{p1b} + g_{p2b} \tag{31}$$

Since in Region 3 all of the ON transistors in the upper device are saturated and the channel length modulation is assumed to be zero, g_a is equal to zero.

The operating point for Region 3, from which the small signal parameters can be derived is approximately halfway between the end points of Region 3 as shown in (32).

$$V_1 \text{ (Region 3 operating point)} \cong \frac{V_{DD}}{2} \tag{32}$$

V_{x1} and V_{x2}, the common source/drain nodes between N_{1A} and N_{2A} and N_{1B} and N_{2B}, respectively, in Region 3 can be derived from (33) and (34):

$$V_{x1} = \frac{(V_{CLK} - V_{TN}) + (V_2 - V_{TN})}{2} - \left\{ \frac{[(V_{CLK} - V_{TN}) + (V_2 - V_{TN})]^2}{4} - (V_{CLK} - V_{TN}) V_1 + \frac{V_1^2}{2} \right\}^{1/2} \tag{33}$$

$$V_{x2} = \frac{(V_{DATA} - V_{TN}) + (V_1 - V_{TN})}{2} - \left\{ \frac{[(V_{DATA} - V_{TN}) + (V_1 - V_{TN})]^2}{4} - \frac{(V_{DATA} - V_{TN})^2}{2} \right\}^{1/2} \tag{34}$$

From these values, each of the small signal parameters in (26)–(31) can be determined.

Region 4

As V_1 increases toward V_{DD} and as V_2 decreases toward ground, V_{DS} across P_{1A}, P_{2A}, N_{1B} and N_{2B} becomes very small, and both A_1 and A_2 approach zero. This breaks the regenerative loop of Region 3, and the bistable register becomes once again an open loop single time constant system in which the P-channel devices charge the capacitor C_1 up to V_{DD} (see Fig. 12). Equations (35) and (36) define $V_1(t)$ within Region 4 where $V_{34}(0)$ is the initial condition of Region 4.

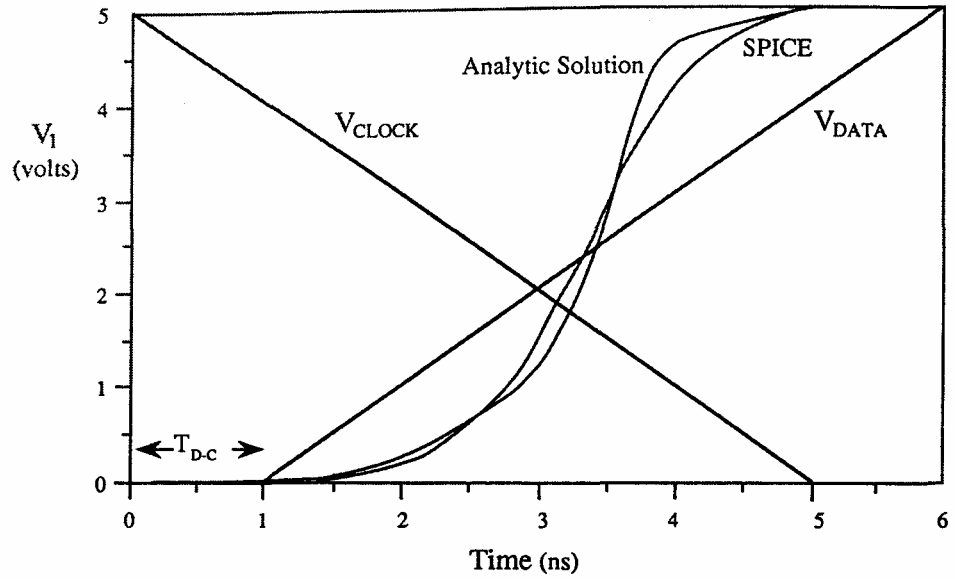

Figure 13. Transient response of bistable register.

Necessary and sufficient conditions for latching

Equations (39) through (42) describe the four necessary and sufficient conditions for latching data into a bistable register.

$$V_{CLK} < V_{DD} + V_{TP} \tag{39}$$

$$V_{DATA} > V_{TN} + V_{X2} \tag{40}$$

$$A_1 V_2 + A_2 V_{CLK} > 0 \tag{41}$$

$$B_1 V_1 + B_2 V_{DATA} > 0 \tag{42}$$

The terms A_1, A_2, B_1 and B_2 represent the transconductance parameters developed in Region 3 and given as (26)–(29). Equation (41) states that the P-channel tree in device A sources more current than the N-channel tree in device A sinks, thereby increasing V_1. Equation (42) states that the N-channel tree in device B sinks more current than the P-channel tree in device B sources, thereby decreasing V_2. If these four conditions are satisfied for all operating points within Region 3, the device will latch.

Limiting requirement for latching

Equation (41) provides the fundamentally limiting condition for latching. As V_{CLK}(min) is reached (see Fig. 14) and the clock signal is returned to V_{DD}, V_2 continues to decrease from V_{DD} to ground. If at the operating point, $V_{CLK} = V_{DD} + V_{TP}$ (P_{2A} becomes cut off), the current supplied by P_{1A} (and driven by V_2) is larger than the current sunk by the N-channel tree of device A, thereby maintaining a

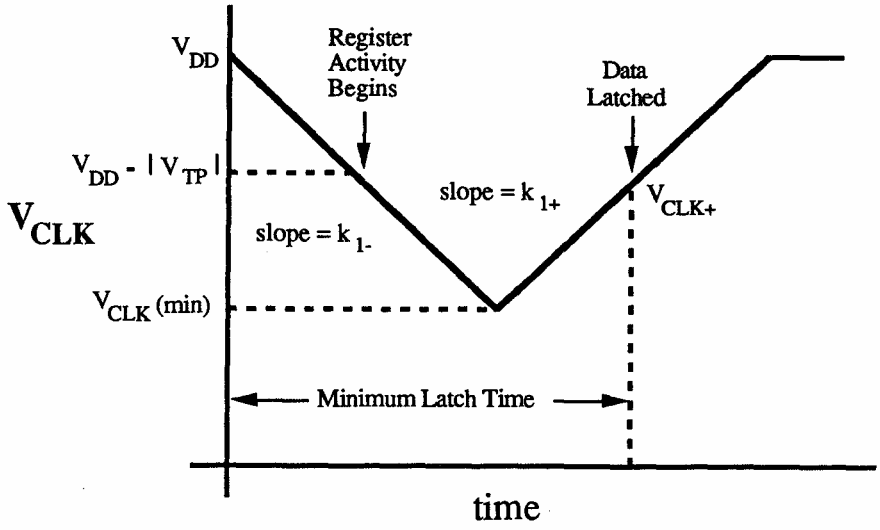

Figure 14. Timing diagram of limiting condition for latching.

monotonically increasing voltage at V_1, the device will latch. This condition can be represented by the inequality shown below:

$$A_1V_2 > A_2V_{CLK} \quad \text{and} \quad A_1V_2 \text{ is a positive quantity} \tag{43}$$

In terms of its small signal parameters, (43) can be presented in the form of (44):

$$g_{mp1a} \geq g_{mn} = \left.\frac{g_{mn1a}\,g_{mn2a}}{g_{n2a}+g_{mn1a}}\right|_{V_{CLK_+}=V_{DD}+V_{TP}} \tag{44}$$

where V_{CLK_+} represents the operating point at which $V_{CLK} = V_{DD} + V_{TP}$ after reaching its minimum value and rising to $V_{DD} + V_{TP}$. Equation (44) represents the ultimate limiting condition for latching data into a bistable register. The Table describes an example circuit which operates just at the latch breakpoint. One parameter, V_{DATA}, was varied to exemplify the limiting nature of (44). The other circuit characteristics were kept constant and are listed below:

$$V_{CLK}(\text{min}) = 1{\cdot}7\,\text{V}$$
$$K'_p,\ K'_n = 4{\cdot}316 \times 10^{-5}\,\text{A V}^{-2}$$
$$k_{1-},\ k_{1+} = 1\,\text{V ns}^{-1}$$
$$W/L \text{ ratio} = 5$$

As shown from the results described within this paper, the magnitude and transition times of the input clock and data signals, as well as the skew between these two signals, $T_{D\text{-}C}$, have a direct influence on whether or not the bistable register will latch.

V_{data} (V)	g_{mp} (Ω^{-1})	g_{mn} (Ω^{-1})	Latch?
2·55	$6{\cdot}578 \times 10^{-4}$	$6{\cdot}603 \times 10^{-4}$	No
2·60	$7{\cdot}907 \times 10^{-4}$	$7{\cdot}907 \times 10^{-4}$	Breakpoint
2·65	$1{\cdot}548 \times 10^{-3}$	0	Yes

Example of limiting latch condition.

6. Conclusions

Closed form solutions of each of the four regions of operation of a bistable register have been developed. Close agreement with a SPICE generated output waveform for an equivalent circuit has been shown. Necessary and sufficient conditions for latching data into a bistable register have been developed. From these conditions, the limiting requirement for latching data into a bistable register have been defined. This result has been corroborated by testing (44) at $V_{CLK+} = V_{DD} + V_{TP}$ with breakpoint conditions, and the result fully agrees with expectations. From these results, fundamentally limiting conditions for latching data into a CMOS bistable register have been described quantitatively.

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