Circuit Synthesis of Clock Distribution Networks based on Non-Zero Clock Skew

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ABSTRACT

A methodology is presented in this paper for synthesizing clock distribution networks by inserting circuit structures to emulate the delay values assigned to specified branches of the clock tree. These clock distribution networks are designed with localized non-zero clock skew [1] so as to improve circuit performance and reliability. The design methodology is targeted for CMOS technology.

The clock lines are transformed from distributed resistive-capacitive interconnect lines into purely capacitive interconnect lines by partitioning the RC interconnect lines with inverting repeaters. The inverters are specified by the geometric size of the transistors, the slope of the ramp shaped input/output waveform, and the output load capacitance. The branch delay model integrates both an inverter delay model and an interconnect delay model. Maximum errors of less than 3% for the delay of the clock paths and 6% for the clock skew between any two registers belonging to the same global data path are obtained as compared to SPICE Level-3.

1. INTRODUCTION

Most existing digital systems utilize fully synchronous timing, requiring a reference signal to control the temporal sequence of operations. Globally distributed signals, such as clock signals, are used to provide this synchronous time reference. These signals can dominate and limit the performance of VLSI-based systems. This is, in part, due to the continuing reduction of feature size concurrent with increasing chip dimensions. Thus interconnect delay has become increasingly significant, perhaps of greater importance than active device delay. Furthermore, the design of the clock distribution network, particularly in high speed applications, requires significant amounts of time, inconsistent with the high design turnaround of the more common data flow portion of a VLSI circuit.

Several techniques have been developed to improve the performance and design efficiency of clock distribution networks, such as repeater insertion [2] to convert highly resistive-capacitive networks into effectively capacitive networks, symmetric distribution networks [3], such as H-tree structures, to ensure minimal clock skew, and zero-skew clock routing algorithms [e.g., 4,5], to automatically layout clock nets. A common weakness of these approaches is that the clock distribution network is designed so as to minimize the clock skew between each register, not recognizing that localized clock skew [6,7] can be used to improve synchronous circuit performance and minimize the likelihood of any race conditions. Furthermore, no known techniques exist today that can automatically synthesize high speed and robust clock distribution techniques while including distributed buffers along the clock path. A novel methodology is therefore presented in this paper for efficiently synthesizing distributed buffer tree-structured clock distribution networks.

The methodology is divided into four major phases. The first phase is the determination of an optimal clock schedule [8,9], defining the localized clock skew schedule which maximizes circuit performance and reliability. In the second phase, a topological design of the clock distribution network is obtained [1], producing a clock tree with minimum delay values assigned to each branch. In the third phase, circuit structures are designed to implement the branch delay values. The final phase is the geometric layout of the clock distribution network. The third phase is the focus of this paper, although the second phase is briefly reviewed to motivate and provide background to the circuit synthesis of clock distribution networks.

In Section 2, the topological design of clock distribution networks is briefly reviewed. The process of implementing branch delay values with CMOS inverters is described in Section 3. Clock path delays derived from this approach are compared to SPICE and presented in Section 4. Finally, the primary results described in this paper are summarized in Section 5.

2. TOPOLOGICAL DESIGN

The topological synthesis of clock distribution networks is divided into three steps. In the first step, the minimum clock path delay of each register in the circuit is determined from the specified clock skew schedule. This task is made possible by recognizing that the clock skew between any two registers in the same global data path is the sum of the clock skews between each pair of registers along the data path formed by the two registers. Furthermore, the clock skew in a feedback path between any two registers is the negative of the clock skew in the forward path. In the next step, the topology of the clock distribution network is determined from the hierarchical description of the circuit. In the final step, delay values are attached to each branch of the clock distribution network, satisfying the initial clock skew assignment. A detailed explanation of each step can be found in [1].

Figure 1 illustrates the topology of a clock distribution network of an example circuit composed of twenty registers.

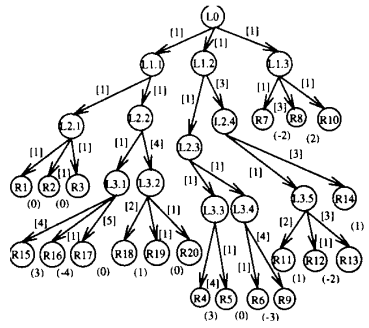

Figure 1: Clock delay and skew assignment for an example clock distribution network

This research is based upon work supported by Grant 200484/89.3 from CNPq (Conselho Nacional de Desenvolvimento Científico e Tecnológico - Brasil) and the National Science Foundation under Grant No. MIP-9208165.

The numbers in parenthesis are the original clock skew specifications, derived from the optimal clock scheduling phase, while the numbers in brackets are the minimum delay values assigned to each branch.

The clock skew between two sequentially adjacent registers is defined in this paper as positive if the clock signal arrives at the final register before arriving at the initial register. The clock skew is negative if the clock signal arrives at the initial register before arriving at the final register. The clock skew is zero if the clock signal arrives at both registers at the same time [6].

3. DESIGN OF CIRCUIT DELAY ELEMENTS

The delay of the circuit structures that emulates the delay values associated with each branch of the network requires high precision, because variations in the delays of the internal branches are propagated throughout the network, causing unacceptable variations in the desired clock skew. It is important to note that it is much more difficult and significant to satisfy the clock skew *between* any two clock paths rather than to satisfy each individual clock path delay.

Delay elements can either be composed of passive or active circuit elements. Implementing the delay elements within the clock distribution network as a passive RC network is unacceptable for several reasons; 1) the delay of each branch is highly dependent on the delay of every other branch, 2) the clock signal waveform would degrade, limiting system performance and reliability, 3) an accurate delay model of a passive clock distribution network for a circuit with thousands of registers is difficult to obtain, and 4) the layout of the passive RC network is highly sensitive to small variations in position or length of the clock lines, producing unacceptable variations in the localized clock skew. Therefore, two criteria must be met to successfully synthesize a clock distribution network. First, the delay of each branch must be implemented such that each branch is independent of the delay of the other branches. Second, the clock branches must be designed such that no physical layout constraints are created which are difficult to implement.

To satisfy both of these criteria, the strategy adopted is to implement the delay segments with active elements, specifically CMOS inverters. Due to the high input impedance of a CMOS inverter, the inverter effectively isolates each clock branch from each other. Additionally, the interconnect lines can be modeled as purely capacitive lines by properly inserting these distributed CMOS inverters as repeaters along the clock signal path [2]. The insertion points are chosen such that the output impedance of each inverter is much greater than the resistance of that portion of the driven interconnect line. This strategy permits the length of a single interconnect line to be accurately modeled as a lumped capacitance with negligible resistance. However, the strategy also places a maximum constraint on the length of an individual portion of an interconnect line between inverting repeaters, thereby limiting the placement of a clock branch within the circuit layout.

3.1 Preserving Clock Signal Polarity

Using a single inverter to produce a specific branch delay may invert the polarity of the clock signal for those clock paths consisting of an odd number of branches. To maintain the proper signal polarity, the tree structured graph representing the topology of the clock distribution network is searched to identify those branches requiring two inverters, ensuring that the number of inverters from the clock source to every register remains even (or odd), while utilizing a minimum number of inverters. As shown in Figure 1, the clock paths that require an extra inverter are those branches which drive R_1, R_2, R_3, and R_{14}, since these paths have an odd number of branches.

3.2 Implementation of Clock Path Delay

Since a signal path in a clock distribution network is typically composed of more than one branch, the total delay of the clock path t_{cpd} is given by the summation of the delays of each individual branch along the clock path τ_{bi}, as

$$t_{cpd} = \sum_{i=1}^{n} \tau_{bi} \tag{1}$$

In order to accurately sum the individual delay components along a clock signal path, four circuit characteristics must be considered: the output impedance of the inverter as compared to the resistance of the interconnect lines driven by the inverter, the capacitance of the interconnect line as compared to the input capacitance of the branches and/or registers driven by the inverter, the output waveform shape of the driving inverter, and the input waveform shape of the driven inverters. These circuit characteristics are considered in order to 1) isolate each branch delay, 2) determine the geometric size of the transistors and load capacitance of each branch, and 3) integrate the inverter and interconnect delay equations used to calculate the delay of each clock path.

The capacitive load at the output of the inverting buffer is composed of the capacitance of an interconnect line plus the input capacitance of each inverter driven by that interconnect line, shown as

$$C_L = C_{line} + \#\ of branches * C_g, \tag{2}$$

where Cg is the input gate capacitance of an inverter and the inverters are assumed to be of equal size. If the inverters are not of equal size, the second term in (2) becomes a summation among all the branches connected to the driving point.

The output waveform of an inverter belonging to one branch is the input waveform of the inverter(s) driving the following branch. This circuit configuration is illustrated in Figure 2, where s_i is the slope of the input signal, s_o is the slope of the output signal, and C_{Li} is the capacitive load of each branch i.

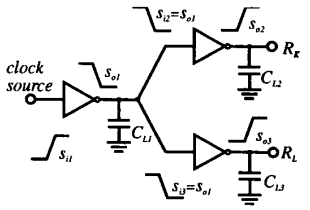

Figure 2: Integration of input/output waveform in a clock path

Under the assumption that the output impedance of the inverter is much larger than the interconnect resistance, the interconnect lines are modeled as lumped capacitors and the slope of the output waveform of the driving inverter is equal to the slope of the input waveform of the driven inverter(s). The slope of the input/output waveform can be characterized by two parameters, the geometric size and the capacitive output load of the driving inverter. Since the capacitive load includes the interconnect line capacitance and the input gate capacitance of each driven inverter, the transistor size and output load of each branch are each determined such that the branch delay and the total delay of a clock path are both satisfied.

3.3 Branch Delay Modeling

The delay equations describing the inverting repeater, shown in (3)-(5), are used to determine the geometric dimensions of the transistors and are based on the MOSFET α-power law I-V model developed by Sakurai and Newton [10].

$$I_{DS} = \begin{cases} 0 & (V_{GS} \le V_{th} \quad : cutoff) \\ (\frac{I'_{DO}}{V'_{DO}})V_{DS} & (V_{DS} < V'_{DO} \quad : linear) \\ I'_{DO} & (V_{DS} \ge V'_{DO} \quad : saturation) \end{cases} , \quad (3)$$

where

$$I'_{DO} = I_{DO}\left(\frac{V_{GS}-V_{th}}{V_{DD}-V_{th}}\right)^{\alpha} = \frac{W}{L_{eff}} P_C (V_{GS}-V_{th})^{\alpha} \quad , \quad (4)$$

$$V'_{DO} = V_{DO}\left(\frac{V_{GS}-V_{th}}{V_{DD}-V_{th}}\right)^{\alpha/2} = \frac{W}{L_{eff}} P_V (V_{GS}-V_{th})^{\alpha/2} \quad , \quad (5)$$

and where I_{DO} is the drain current at $V_{GS} = V_{DS} = V_{DD}$, V_{DO} is the drain saturation voltage at $V_{GS} = V_{DD}$, V_{th} is the threshold voltage, α is the velocity saturation index, and V_{DD} is the supply voltage. The parameters α, V_{DO}, I_{DO}, and V_{th} are calculated as explained in [10].

The input of each clock branch is assumed to be driven by a ramp signal with rising and falling slopes, s_r and s_f, respectively, selected such that during discharge (charge), the effects of the PMOS (NMOS) transistor can be neglected [11]. The circuit structure of the inverter is illustrated in Figure 3a, with the shape of the input and output waveforms illustrated in Figure 3b.

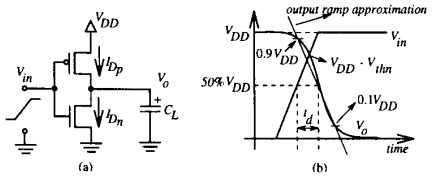

Figure 3: (a) Delay element; (b) Input/output waveforms of the delay element

The time t_d from the 50% V_{DD} point of the input waveform to the 50% V_{DD} point of the output waveform is defined as the delay of the circuit element. Equation (6), derived from (3)-(5) [10], describes the delay of a CMOS inverter in terms of its load capacitance C_L.

$$C_L = \frac{2I_{DO}}{V_{DO}}\left[t_d - \left(\frac{1}{2} - \frac{1-v_T}{1+\alpha}\right)s_r\right], \quad where\ v_T = \frac{V_{th}}{V_{DD}} \quad (6)$$

The output waveform of the driving inverter is the input signal to all the branches connected to this inverter and is approximated by a ramp shaped waveform. This approximation is achieved by linearly connecting the points $0.1V_{DD}$ and $0.9V_{DD}$ of the output waveform and is accurate as long as the interconnect resistance is negligible as compared to the inverter output impedance. The slope is expressed as

$$s_r = \frac{t_{0.9}-t_{0.1}}{0.8} = \frac{C_L V_{DD}}{I_{DO}}\left(\frac{0.9}{0.8} + \frac{V_{DO}}{0.8V_{DD}} ln \frac{10V_{DO}}{eV_{DD}}\right) \quad . \quad (7)$$

Equations (6) and (7) provide the necessary relationships to design the circuit elements of a clock signal path, as explained below:

Design of clock signal path - The initial branch of each clock signal path is the branch connected directly to the clock source. The input slope is assumed zero for this branch, since the source of the clock signal is assumed to behave as a step function. Given the branch delay, the capacitive load of the inverter is determined from (6). The effective interconnect capacitance is the capacitance derived from (6) minus the gate capacitance of the branches connected to the driving buffer. The slope of the output signal is obtained from (7) and is the input slope of the following stage. To design the circuit structures of the following branches, the previous steps are used recursively by first calculating the required load capacitance, and then using this value of capacitance to calculate the slope of the signal waveform of the following stage. This procedure is continued until each register driven by the clock distribution network is reached.

For a certain range of branch delay, the load capacitance obtained with (6) may be small enough to be of the same order of magnitude as the drain capacitance of the buffer, compromising the accuracy of the buffer delay. To overcome this uncertainty, the load capacitance is increased, requiring the driving buffer to be resized by the same order of magnitude. Assuming that the geometric channel length remains fixed, the width of a resized transistor is [10]

$$I_{DO(new)} = \frac{W_{new}}{W_{measured}} I_{DO(measured)} \quad (8)$$

Equations (6)-(8) are sufficient to determine the geometry and load capacitance of every inverter along the branches of the clock distribution network.

4. EXPERIMENTAL RESULTS

Table 1 compares the difference between the calculated and measured clock path delays for the circuit shown in Figure 1. The second column depicts the desired delay obtained from the topological and circuit design of the clock distribution network. The third column shows the delay values of each clock path derived from SPICE circuit simulation using Level-3 device

Table 1: Comparison between calculated and measured clock path delay

Clock Path	Delay (ns)	SPICE (ns)	Error (%)
R_1, R_2, R_3	3.0	3.07	2.3
R_{15}, R_4, R_9	7.0	7.11	1.6
R_{18}	8.0	8.10	1.3
R_{19}, R_{20}	7.0	7.04	<1
R_5, R_6, R_{16}	4.0	4.06	1.5
R_{17}	8.0	8.06	<1
R_{14}	7.0	7.17	2.4
R_{11}	7.0	7.16	2.3
R_{12}	6.0	6.14	2.3
R_{13}	8.0	8.20	2.5
R_7, R_{10}	2.0	1.98	1.0
R_8	4.0	4.07	1.8

models, while the fourth column depicts the per cent error between the calculated and the numerically derived delay, where the maximum error is less than 3%.

A more significant measure of the effectiveness of this clock distribution network design methodology is to guarantee that the clock skew between any pair of registers in the same global data path is accurately satisfied, rather than the delay of each individual

clock path. Table 2 illustrates the clock skew between registers for the circuit illustrated in Figure 1. Column two shows the scheduled clock skew implemented with the design methodology described in this paper for the pair of registers presented in column one. Column three depicts the values obtained from SPICE circuit simulation, while column four shows the per cent error between both measurements. Note that the maximum error is 6%, a number well within practical and useful limits.

Table 2: Comparison between specified and measured clock skew values

Registers	Specified Skew (ns)	Measured (ns)	Error (%)
R_1 - R_3	0.0	0.0	0.0
R_{15} - R_{16}	3.0	3.0	0.0
R_{12} - R_{13}	-2.0	-2.06	3.0
R_{17} - R_{19}	1.0	1.03	3.0
R_4 - R_{14}	0.0	0.06	6.0
R_6 - R_{12}	-2.0	-2.08	4.0
R_5 - R_{13}	-4.0	-4.14	3.5

The individual data paths have been selected to illustrate several types of clock skew situations, such as non-zero clock skew between registers in the same data path or in separate data paths. More specifically, zero clock skew between registers in the same data path is illustrated by the path between registers R_1 and R_3. The path between registers R_{15} and R_{16} illustrates positive clock skew for registers in the same data path, while the path between registers R_{12} and R_{13} illustrates negative clock skew for registers in the same data path. In these three examples, the clock skew is only dependent upon the delay of the external branches, and therefore these clock paths are independent of the delay variations of the internal branches of the clock distribution network. Other examples are more illustrative of the possible effects of internal branch delays within the clock path. The path between registers R_{17} and R_{19} illustrates non-zero clock skew in a data path with feedback which is dependent on the delay of its internal branches. The last three examples illustrate the clock skew between two registers belonging to interconnected data paths. The first example, the path between registers R_4 and R_{14}, illustrates zero clock skew between two registers. The final examples, the path between registers R_5 and R_{13} and registers R_6 and R_{12}, illustrate the effects of negative clock skew on two registers. Observe that in the last examples, the error tolerance of the clock skew is still within acceptable margins, exhibiting good accuracy, even for those paths in which the clock skew between two registers have a significant portion of the clock distribution network in common.

5. CONCLUSIONS

VLSI/ULSI-based synchronous systems require the efficient synthesis of high speed clock distribution networks in order to obtain higher levels of circuit performance. In this paper, circuit performance is improved by using non-zero localized clock skew to reduce the minimum clock period. An integrated methodology is presented for synthesizing clock distribution networks and is divided into four phases, 1) optimal clock scheduling, 2) topological design of the clock distribution network, 3) design and modeling of the circuit delay elements, and 4) layout implementation. The focus of this paper is the third phase, the design and modeling of the circuit delay elements.

A strategy for implementing the branch delay values of the clock distribution network is presented, using CMOS inverters for the delay elements. The minimum number of inverters to satisfy the branch delay is obtained, while preserving the polarity of the signal driving the clock input of each register. Delay equations of an inverter, derived from the α-power law I-V model, are described. The inverter delay model accurately determines the delay of each clock path by considering the fanout, interconnect capacitance, and the slope of the input and output waveforms of each branch along the clock path. Comparisons between expected and simulated delays of each individual clock signal path produce circuits with a maximum error of less than 3%. Furthermore, the maximum error between scheduled and simulated clock skew for any two registers belonging to the same global data path is 6%.

Thus, an integrated methodology for synthesizing clock distribution networks for high performance VLSI circuits is presented. This methodology, based on inserted delay elements, accurately synthesizes localized clock skews. Furthermore, this methodology utilizes non-zero clock skew to improve overall system performance.

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