Repeater Design to Reduce Delay and Power in Resistive Interconnect

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Abstract – In large chips, the propagation delay of the data and clock signals is limited due to long resistive interconnect. The insertion of repeaters alleviates the quadratic increase in propagation delay with interconnect length while decreasing power dissipation by reducing short-circuit current. Design equations for determining the optimum number of repeaters to be inserted along a resistive interconnect line for reduced delay are presented. Power dissipation in repeater chains is also analyzed. The analytical model used in these design equations is based on the α-power law I-V equations for modeling short-channel devices and exhibits a maximum error of 16% for typical *RC* loads as compared to SPICE.

I. Introduction

As the size of CMOS integrated circuits continues to increase, interconnections have become increasingly significant. With a linear increase in length, interconnect delay increases quadratically due to a linear increase in both interconnect resistance and capacitance [1]. Also, large interconnect loads not only affect performance but cause excess power to be dissipated. A large *RC* load degrades the waveform shape, dissipating excessive short circuit power in the following stages loading a CMOS logic gate.

Several methods have been introduced to reduce interconnect delay so that these impedances do not dominate the delay of a critical path [1–4]. Furthermore, with the introduction of portable computers, power has become an increasingly important factor in the circuit design process. Thus, power consumption must be both estimated and minimized when developing design techniques that improve the speed of long resistive interconnections.

In this paper, the propagation delay and transition time characteristics of a system of repeaters driving a large resistive interconnect is analyzed. A methodology is presented for determining the number and size of the repeaters to attain the minimum propagation delay and transition time based on an analytical expression derived from the α-power law model for short-channel devices [5].

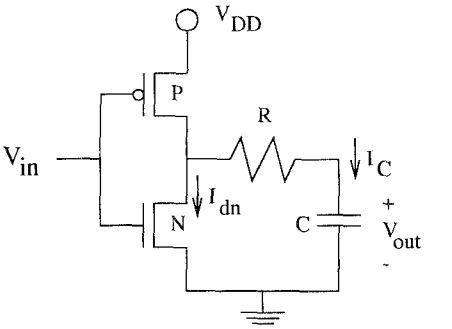

Figure 1. A CMOS inverter driving an *RC* load.

The issue of minimum power dissipation is also analyzed. An empirical analysis is presented for determining the optimal number of repeaters to attain the minimum power when considering both short-circuit power and dynamic power dissipation.

The paper is organized as follows: a methodology for determining the minimum delay and transition time is discussed in Section II. A comparison of the analytical results to SPICE is described in Section III. An empirical analysis of repeater design with respect to short-circuit power is shown in Section IV. Finally, some concluding remarks are offered in Section V.

II. Delay of a Repeater Chain Driving an *RC* Load

Analytical expressions describing the behavior of an inverter driving a lumped *RC* load (as shown in Fig. 1) based on Sakurai's α–power law model [6] are presented in [5]. This model assumes the transistor operates in the linear region when driving an *RC* load, since the linear region is the dominant region of operation when operating with fast inputs. In [5] it is shown that for a step input, the time to reach a given output voltage V_{out} is

$$t_{out} = \frac{\upsilon_{do} RC + C}{\upsilon_{do}} \ln\left(\frac{V_{DD}}{V_{out}}\right) , \qquad (1)$$

where υ_{do} is the saturation conductance, a device parameter from the α-power law model derived from $\frac{I_{do}}{V_{do}}$. I_{do} is the saturation current of the device when $V_{DS}=V_{DD}$. V_{do} is the voltage at which the device begins to operate in the saturation region [5,6].

Equation (1) describes the time t_{out} an inverter driving an *RC* load takes to reach an output voltage V_{out} given a step input. This equation can be expanded

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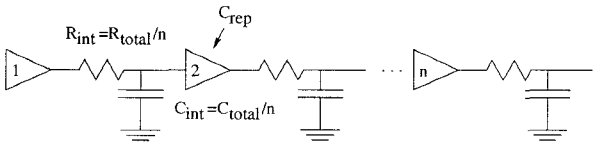

Figure 2. n equal sized CMOS inverting repeaters driving an *RC* load.

to include the parasitic capacitances of the following inverting repeater, as

$$t_{out} = \frac{(1+\mho_{do}R)(C_{rep}+C_{int})}{\mho_{do}} \ln\left(\frac{V_{DD}}{V_{out}}\right) \quad . \quad (2)$$

C_{rep} and C_{int} are the capacitances of the following inverter and the interstage load capacitance, respectively.

The delay required to propagate a signal through a large resistive interconnect can be reduced if the interconnect is broken up and distributed among a number of repeaters such as shown in Fig. 2. However, the delay of this signal path will increase if a non-optimal number of repeaters is chosen. In order to choose the optimal number of repeaters for a given *RC* load, the delay from the input of the first repeater to the output of the last repeater is first determined.

The switching characteristics of an n–stage repeater system determined from both SPICE and an analytical expression developed below are shown in Fig. 3. The analytical expression for the total time t_{total} from a step input to the output of the n-stage repeater is the sum of several expressions,

$$t_{total} = t_{first\ stage} + (n-2)t_{int.\ stage} + t_{final\ stage} \quad . \quad (3)$$

The first term $t_{first\ stage}$ is the time required for the output of the first repeater to reach the turn-on voltage of the second repeater assuming the output voltage is initially at V_{DD}. The term $t_{int.\ stage}$ describes the time required for each repeater between the first and last stage to transition from V_{DD}+V_{TP} to V_{TN} or vice versa. The time required for the output of the final repeater to reach either 10%, 90%, or 50% of V_{DD} from one threshold voltage is described by the third component of (3), $t_{final\ stage}$. Equation (3) is described in more detail below with reference to Fig. 3.

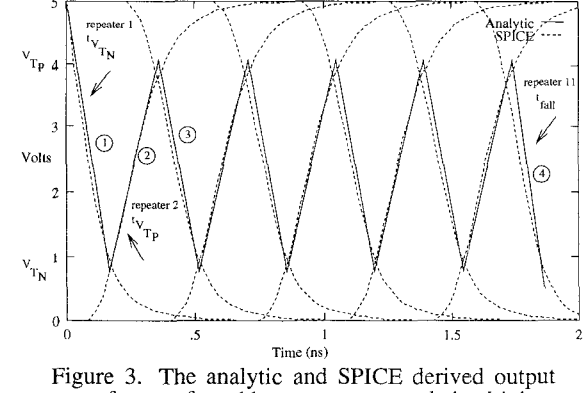

Figure 3. The analytic and SPICE derived output waveforms of an 11–stage repeater chain driving an evenly distributed *RC* load of 1 KΩ and 1 pF.

The first component of t_{total}, $t_{first\ stage}$, is the time required for the output signal of the first repeater to drop from V_{DD} to V_{TN}, the threshold voltage of the N-channel device (labeled 1 in Fig. 3). V_{TN} is chosen as the end point because it is assumed during fast switching that the pull-up device of the following repeater turns on hard near the voltage the pull-down device turns off. Therefore, $t_{first\ stage}$ is

$$t_{V_{T_N}} = \frac{\left(1+\mho_{do_N}R_{int}\right)\left(C_{int}+C_{rep}\right)}{\mho_{do_N}} \ln\left(\frac{V_{DD}}{V_{T_N}}\right) . \quad (4)$$

This equation also describes the time for the signal to transition from ground to V_{DD}+V_{TP} when each N–channel transistor is replaced by a P–channel transistor. All of the following equations can be similarly expressed for a P-channel device. Note that V_{TP} is the P-channel threshold voltage and is negative for an enhancement mode device.

The delay of each successive stage (n-2)$t_{int.\ stage}$, excluding the final stage, is modeled as the time required for the signal to transition from V_{DD}+V_{TP} to V_{TN}. Equation (4) describes the time for the output signal to change from V_{DD} to V_{TN}. Therefore, the time for the signal to transition from V_{DD} to V_{DD}+V_{TP} must be subtracted from (4). Equation (5) describes the time for the output signal to change from V_{DD} to V_{DD}+V_{TP},

$$t_{t_P} = \frac{\left(1+\mho_{do_N}R_{int}\right)\left(C_{int}+C_{rep}\right)}{\mho_{do_N}} \ln\left(\frac{V_{DD}}{|V_{TP}|}\right) . \quad (5)$$

Therefore, an intermediate stage delay $t_{int.\ stage}$ is described by $\left(t_{V_{T_P}} - t_{t_N}\right)$ for a rising repeater output and $\left(t_{V_{T_N}} - t_{t_P}\right)$ for a falling repeater output (labeled 2 and 3, respectively, in Figure 3). The two preceding expressions are alternately added to the total delay for each corresponding repeater stage up to the input of the final stage of the chain.

As previously mentioned, t_{total} describes the output of the complete repeater system in terms of either: (1) the delay at 10% or 90% of V_{DD} which is defined as the transition time t_t or (2) the delay at 50% V_{DD} which is defined as the propagation delay t_{PD}. In order to determine t_t at the output of the chain of repeaters, the final term in t_{total}, $t_{final\ stage}$, describes the time required for the signal to transition from V_{DD}+V_{TP} to .1V_{DD}. If t_{PD} is desired, the time for the output to change from V_{DD}+V_{TP} to .5V_{DD} is determined. The term for the final stage is labeled 4 in Figure 3 and the expressions for t_t and t_{PD} for the last stage are

$$t_t = 2.3\frac{(1+\mho_{do}R_{int})C_{int}}{\mho_{do}} \quad (6)$$

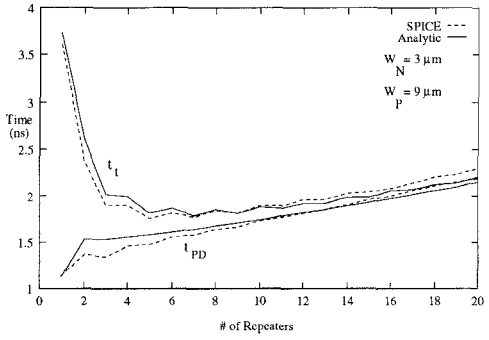

Figure 4. The analytical and simulated propagation delay and rise (or fall times) for a 1 KΩ and 1 pF load evenly distributed across a number of uniformly sized repeaters.

and

$$t_{PD} = .693\frac{(1+\mho_{do}R_{int})C_{int}}{\mho_{do}} \quad (7)$$

In calculating both t_t and t_{PD}, the initial voltage is assumed to be V_{DD}, therefore t_{t_P} must be subtracted from the final term in (3). The total time from the step input at the first repeater to the output of an even number of repeaters (for a 90% transition time) is

$$t_{total(even)} = t_{V_{T_N}} + \frac{(n-2)}{2}\left(t_{V_{T_P}} - t_{t_N} + t_{V_{T_N}} - t_{t_P}\right) + \left(t_t - t_{t_N}\right) \quad (8a)$$

$$t_{total(odd)} = \frac{(n-1)}{2}\left(t_{V_{T_P}} - t_{t_N} + t_{V_{T_N}} - t_{t_P}\right) + t_t \quad (8b)$$

III. Analysis of Analytical Delay versus SPICE

Two different *RC* loads have been chosen to investigate the effects of interconnect resistance and capacitance on repeater design (the *RC* loads are 1 KΩ and 1 pF and 3 KΩ and 3 pF). These experiments are based on a 0.8 μm technology. The plots shown in Fig. 4 depict the transition time and the propagation delay of an *RC* load of 1 KΩ and 1 pF distributed evenly among one to 20 repeaters. The size of each repeater is uniform (W_N = 3 μm and W_P = 9 μm), although this analysis does not restrict the geometric widths to be uniform. The rise and fall time of each individual repeater is ratioed to maintain nearly equal transition times.

In Fig. 4, the propagation delay of a chain of repeaters driving an *RC* load as a function of the number of repeater stages is shown for both the analytic expression and SPICE. The maximum errors of the propagation delay and the transition time are 12% and 8%, respectively. Note that the greatest error occurs when the repeater chain is two or three stages. The model is most accurate when the loaded inverter operates predominately in the linear region. With only two or three repeaters, the inverters operate outside of the linear region for a longer period of time than with more than three repeaters.

The error of the analytical delay as compared with the delay derived from SPICE for a given *RC* load, repeater size, and number of repeaters is shown in Table I and presented in graphical form in Fig. 5. The deviation of the analytical result from SPICE is shown as a function of the number of stages in Fig. 5. As shown in Fig. 5, for large *RC* loads (*e.g.*, 3 KΩ and 3 pF), the model becomes less accurate since the repeaters operate for relatively less time within the linear region.

# of Stages	R=1 KΩ, C=1 pF W_N=1 μm W_P=3 μm		R=1 KΩ, C=1 pF W_N=3 μm W_P=9 μm		R=3 KΩ, C=3 pF W_N=3 μm W_P=9 μm	
	t_{PD}	t_t	t_{PD}	t_t	t_{PD}	t_t
1	-16%	-2%	0%	3%	2%	2%
2	-6%	1%	9%	8%	31%	20%
3	-2%	-2%	12%	6%	35%	22%
4	-5%	0%	5%	5%	27%	21%
5	-3%	-2%	5%	3%	25%	20%
6	-5%	-1%	1%	3%	20%	18%
7	-3%	-3%	2%	1%	19%	15%
8	-5%	-2%	0%	-1%	15%	14%
9	-4%	-2%	4%	0%	14%	13%
10	-5%	-2%	0%	-1%	11%	11%
11	-4%	-4%	0%	-1%	11%	10%
12	-4%	-3%	-1%	-2%	9%	9%
13	-5%	-4%	-1%	-2%	8%	8%
14	-5%	-3%	-1%	-2%	7%	7%
15	-5%	-4%	-2%	-2%	7%	5%
16	-4%	-3%	-2%	-1%	7%	5%
17	-5%	-5%	-3%	-3%	5%	4%
18	-6%	-5%	-3%	-4%	5%	6%

Table I. Per cent error of analytical delay versus SPICE for a given *RC* load, repeater size, and number of repeater stages. Negative numbers indicate the analytical solution is less than SPICE.

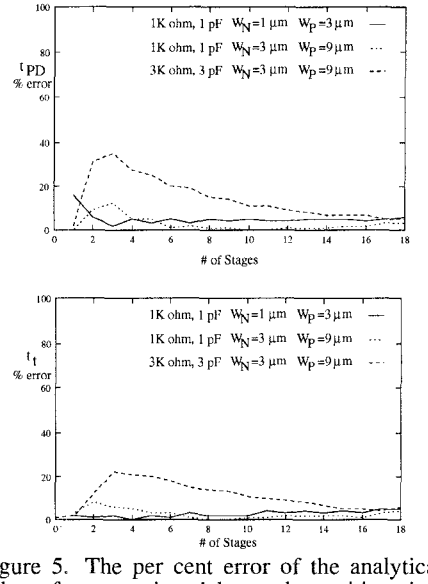

Figure 5. The per cent error of the analytical value of propagation delay and transition time versus SPICE for various loads and repeater sizes.

IV. Short-Circuit Power in Repeater Chains

For every signal transition, there is a period of time during which both the N-channel and P-channel devices of a repeater are turned on. During this time, a DC path

from power to ground occurs in each repeater, permitting short-circuit current to flow [7–9]. An example of short-circuit current and power is shown in Figure 6. As the input transition slows, more short-circuit power is dissipated within the repeater stage. The input signal transition time can be controlled by the number of repeaters in the chain. If additional repeaters are inserted into a line to drive a long interconnect, each repeater drives a smaller *RC* load, therefore, the input transition of the following repeater is faster. However, these additional repeaters may increase the short-circuit power of the total repeater system. The peak short-circuit current, which is proportional to the device width, is the other primary factor that determines the short-circuit power [5,9].

Empirical evidence shows that when device sizes are small, the contribution of short-circuit power is small in comparison to dynamic power, typically ranging from 1% to 5%. As the geometric width of the repeaters is increased, the contribution of the short-circuit and dynamic power also increases. However, as the geometric width and the number of repeaters increases, dynamic power increases linearly, whereas short-circuit power changes non-linearly. A comparison of short-circuit power versus dynamic power for an *RC* load of 1 KΩ and 1 pF is shown in Figure 7. Both the short-circuit power and the dynamic power dissipated within the repeater chain versus the number of repeaters are shown. For the larger sized repeater, the peak short-circuit power is about 30% of the dynamic power at two stages; at five stages short-circuit power is 12% of the dynamic power; and at nine stages, about 5%. Five stages of this particular repeater circuit are found to minimize the transition time for this *RC* load. Thus, reducing the repeater size to 15 μm and 45 μm from 25 μm and 75 μm saves 40% in area (200–240 μm^2), reduces the short-circuit power by 60%, and reduces the dynamic power by 12% in return for a 5% increase in transition time. Note that the minimum savings occurs when the input transition time of each repeater is approximately equal to the repeater output transition time [7,9]. An analytical method to determine the short-circuit power dissipation in repeater chains is currently under investigation.

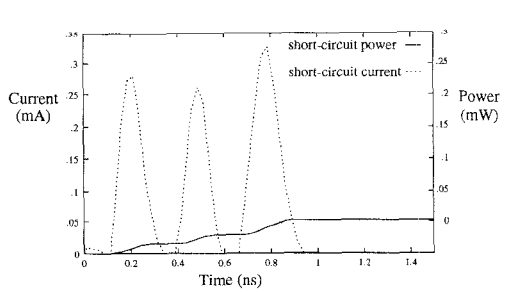

Figure 6. Short-circuit current and power dissipated in a four–stage repeater with W_N=5 μm and W_P=15 μm, f = 10 MHz.

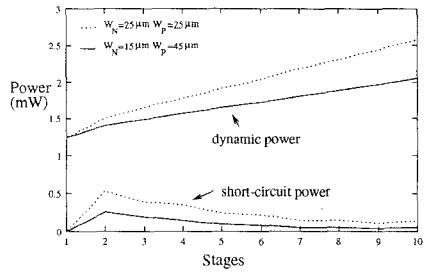

Figure 7. The short-circuit and dynamic power dissipated in an inverter chain versus the number of stages. Note the small increase in short-circuit power from nine to ten stages for the larger sized repeater.

V. Conclusions

Design equations for determining the optimum number of uniformly sized repeater to be inserted along a resistive interconnect line for reduced delay and power have been presented. Analytical estimates of delay are within 16% of SPICE. Using these analytical expressions to determine the optimal number of repeaters, only a 4% loss in transition time is experienced in return for a significant savings in area and a modest savings in power.

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