Transient Analysis of a CMOS Inverter Driving Resistive Interconnect

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Abstract— **Expressions characterizing the output voltage and propagation delay of a CMOS inverter driving a resistive-capacitive interconnect are presented in this paper. The MOS transistors are characterized by the nth power law model. In order to emphasize the nonlinear behavior of a CMOS inverter, the interconnect is modeled as a lumped RC load. The propagation delay of a CMOS inverter is characterized for both a fast ramp and a slow ramp input signal. The waveform of the output voltage based on these analytic equations is quite close to SPICE assuming a fast ramp input signal. The accuracy of the propagation delay model for both fast ramp and slow ramp input signals is within 7% as compared to SPICE simulations.**

I. Introduction

As integrated circuit technologies continue to improve, the feature size of MOS transistors and interconnect lines has decreased. Since the chip size and the integration density have increased dramatically, the average interconnect length has not scaled down with feature size. Therefore, on-chip interconnect has become increasingly important [1]. The delay of these highly scaled circuits is now dominated by the interconnect [2], [3]. Furthermore, up to 30% of the dynamic power is due to the interconnect [4].

Interconnect in CMOS circuits has historically been modeled as a capacitive load [5]. Analytic expressions characterizing the propagation delay and short-circuit power based on a capacitive model have been previously addressed in the literature [6–9]. However, the parasitic interconnect resistance has increased significantly due to technology scaling. If the interconnect resistance is comparable to the effective output resistance of a CMOS logic gate, the interconnect impedance should be modeled as a resistive-capacitive load [10]. Furthermore, the interconnect parasitic capacitance does not decrease with scaling due to fringing fields between neighboring interconnections. If the length of an interconnect line increases linearly, the interconnect impedance increases quadratically [2] due to a linear increase in both the interconnect capacitance and resistance. Therefore, the effect of the RC interconnect impedance on the overall propagation delay is significant.

The Shichman-Hodges model [11] for a MOSFET is widely used in analyzing the characteristics of a CMOS circuit [12], [13]. However, the model is not accurate for short-channel transistors because velocity saturation effects of the carriers are neglected. The alpha power law model [7] has been proposed to fill the gap between the classical Shichman-Hodges model and more accurate, albeit complicated, I-V models. However, this model is not sufficiently accurate in the linear region or to characterize the drain-to-source saturation voltage of a MOS transistor. An improved model, the nth power law model [14], has also been proposed by Sakurai. The nth power law model is used in this paper to derive tractable analytic equations to characterize the behavior of the circuit, thereby maintaining an intuitive understanding of the device and circuit behavior when operating within the deep submicrometer region.

The propagation delay model based on [15] and [16] is not physically intuitive, which involves curve fitting techniques and does not explicitly consider the device parameters. The MOS transistors are modeled as a linear resistor in [10], neglecting the nonlinear behavior of the MOS transistors.

In this paper, an extension of previous work [17], [18] is presented in which the interconnect is modeled as a lumped RC load. The more accurate nth power law model is used to characterize the deep submicrometer MOS transistors. Analytic expressions characterizing the propagation delay of both fast and slow ramp input signals are presented. The output voltage of a CMOS inverter is based on a fast ramp input signal. The interconnect resistance shields the load capacitance in the saturation region as compared to a purely capacitive load [15]. The signal quality is also degraded by the interconnect resistance, causing additional short-circuit power to be dissipated by the following logic stage. The accuracy of these analytic equations is compared with SPICE simulations. The waveform of the estimated output voltage based on these analytic equations is quite close to SPICE for fast ramp input signals. The accuracy of the estimated propagation delay for both fast ramp and slow ramp input signals is within 7% as compared to SPICE simulations.

The analytic equations describing the propagation delay of a CMOS inverter driving a resistive-capacitive load for both fast and slow ramp input signals, and the closed form expressions characterizing the output voltage of a CMOS inverter for a fast ramp input signal are presented in Section II. The effects of interconnect resistance on the propagation delay and short-circuit power dissipation of a CMOS inverter are discussed in Section III. The application of these analytic equations to circuit analysis is presented in Section IV, followed by some concluding remarks in Section V.

II. Output Voltage and Propagation Delay

The propagation delay of a CMOS inverter depends upon the load conditions, device parameters, and input transition times. In this section, the characteristics of a CMOS inverter driving a resistive-capacitive load is described based on the nth power law model and the input slew rate. Closed form expressions characterizing the output voltage of a CMOS inverter are derived in subsection A under an assumption of a fast ramp input signal. The temporal properties of a CMOS inverter are discussed in subsection B for a fast ramp input signal. The propagation delay of a CMOS inverter driven by a slow ramp input signal is discussed in subsection C.

A. The Output Voltage

A circuit diagram of a CMOS inverter driving a lumped RC load is shown in Fig. 1. R and C are the load resistance and capacitance, respectively. The input is assumed to be a rising ramp signal, defined as

$$V_{in}(t) = \frac{t}{\tau_r} V_{dd} \qquad 0 \le t \le \tau_r, \tag{1}$$

where τ_r is the input transition time. The initial states of both V_o and V_1 are V_{dd}; therefore, the PMOS transistor is ON and the

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NMOS transistor is OFF. No current flows through the PMOS transistor because the drain-to-source voltage is zero.

The output voltage of a CMOS inverter, *i.e.*, V_o as shown in Fig. 1, is based on the nth power law model, the load conditions, and a fast ramp input signal. The effect of the PMOS transistor is neglected based on an assumption of a fast ramp input signal, where the input exceeds one-third of the output slope [5]. This assumption is not valid if the input is slow as compared to the output signal.

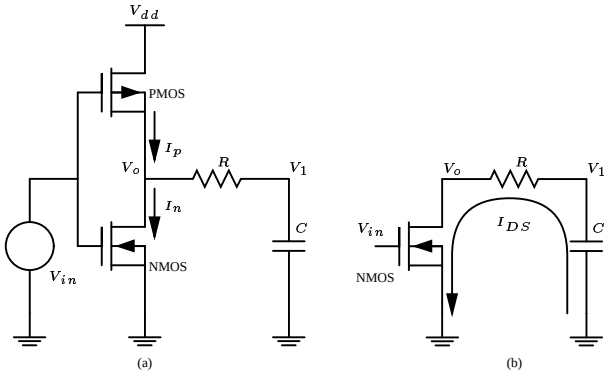


Fig. 1. A CMOS inverter driving a resistive-capacitive load. (a) A circuit diagram of a CMOS inverter driving a lumped RC load. (b) A circuit schematic of an NMOS transistor driving an RC load assuming the short-circuit current is neglected.

The relations among V_o, V_1, and I_{DS} as shown in Fig. 1 are

$$V_1 = V_o + RI_{DS}, \tag{2}$$

$$C\frac{dV_1}{dt} = -I_{DS}. \tag{3}$$

Before the input voltage reaches V_{TN}, the NMOS transistor is OFF and no current will flow. Therefore, the output voltage V_o remains at V_{dd}.

Once the input voltage reaches V_{TN}, the NMOS transistor turns ON and starts to operate in the saturation region. Once I_n exceeds I_p, V_o drops below the initial voltage V_{dd}. The output voltage is

$$\begin{aligned} V_o(t) = & V_{dd} - \frac{B'V_{dd}^n\tau_r}{C}\frac{1}{n+1}(\frac{t}{\tau_r} - \nu_T)^{n+1} \\ & - RB'V_{dd}^n(\frac{t}{\tau_r} - \nu_T)^n \quad \text{for} \quad \tau_n \le t \le \tau_r, \end{aligned} \tag{4}$$

where $\nu_T = V_{TN}/V_{dd}$ and τ_n is the time when the input voltage reaches V_{TN}, $\tau_n = \nu_T\tau_r$.

After τ_r, the transition of a fast ramp input signal is completed and the input voltage is fixed at V_{dd}. The NMOS transistor remains in the saturation region. Therefore, the discharge current is the saturated drain-to-source current of the NMOS transistor, *i.e.*, a constant I_{DSAT}. The output voltage is obtained based on the condition at $t = \tau_r$,

$$\begin{aligned} V_o(t) = & V_{dd} - \frac{B'V_{dd}^n}{C}(1-\nu_T)^n(t - \frac{n+\nu_T}{1+n}\tau_r) \\ & - RB'V_{dd}^n(1-\nu_T)^n \quad \text{for} \quad \tau_r \le t \le \tau_{sat}, \end{aligned} \tag{5}$$

where τ_{sat} is the time when the NMOS transistor leaves the saturation region.

The NMOS transistor operates in the linear region after τ_{sat}, the input voltage remains at V_{dd} and the output voltage falls below V_{DSAT}. The solutions of V_o and the time constant τ become

$$V_o(t) = \frac{2(V_{DSAT} + 2RI_{DSAT})V_{DSAT}}{(V_{DSAT} - 2RI_{DSAT}) + V_C e^{\frac{t-\tau_{sat}}{\tau}}}, \tag{6}$$

$$\tau = \frac{(V_{DSAT} + 2RI_{DSAT})C}{2I_{DSAT}}, \tag{7}$$

respectively, where $I_{DSAT} = B'V_{dd}^n(1-\nu_T)^n$ and $V_C = V_{DSAT} + 6RI_{DSAT}$.

B. Propagation Delay Assuming a Fast Ramp Input Signal

The propagation delay of a CMOS inverter $t_{0.5}$ is typically defined as the time from the 50% V_{dd} point of the input to the 50% V_{dd} point of the output. The high-to-low propagation delay $t_{p_{HL}}$ of a CMOS inverter is approximated as

$$\begin{aligned} t_{p_{HL}} &= t_{0.5} - \frac{\tau_r}{2} \\ &= \frac{C}{I_{DSAT}}(\frac{V_{dd}}{2} - RI_{DSAT}) + (\frac{n+\nu_T}{n+1} - \frac{1}{2})\tau_r, \end{aligned} \tag{8}$$

where $I_{DSAT} = B'(V_{dd} - V_{TN})^n$.

Similarly, the low-to-high propagation delay of a CMOS inverter can be derived based on the time required to charge up a load capacitor. Note that there are two terms in the delay expression in (8). The first term linearly depends upon the load capacitance and the difference between $V_{dd}/2$ and RI_{DSAT}. The second term is linearly proportional to the input transition time τ_r.

C. Propagation Delay Assuming a Slow Ramp Input Signal

The analyses presented in subsections A and B are based on an assumption of a fast ramp input signal, *i.e.*, the NMOS transistor remains in the saturation region before the input transition is completed. Therefore, the fast ramp condition can be quantified based on the previous analysis, *i.e.*, τ_r is compared to the time when the output signal reaches the saturated voltage τ_{sat}. If τ_r is greater than τ_{sat}, *i.e.*, the NMOS transistor enters the linear region before the input transition is completed, the input should be treated as a slow ramp signal. A criterion for a fast ramp input signal is

$$f(\tau_r) = \tau_{sat} - \tau_r \ge 0. \tag{9}$$

Quantitatively, if $f(\tau_r) \ge 0$, the input is a fast ramp signal, otherwise, it is a slow ramp signal.

For a slow ramp input signal, when the input signal is greater than V_{TN}, the NMOS transistor is ON and starts operating in the saturation region. The output voltage can therefore be expressed as (4). τ_{sat} for a slow ramp input signal is also determined from (4)

In the aforementioned analysis of a slow ramp input signal, the effect of the PMOS transistor is neglected. In order to accurately estimate the propagation delay for a slow ramp input signal, some assumptions are necessary. The high-to-low propagation delay is approximated as

$$t_{p_{HL}} = \frac{\tau_r}{\tau_{sat}}(t_{0.5} - \frac{\tau_r}{2}), \tag{10}$$

where the ratio τ_r/τ_{sat} characterizes the degree to which the input signal deviates from a fast ramp input signal. Both $t_{0.5}$ and τ_{sat} can be obtained from (4). Therefore, the propagation delay for both a fast ramp and a slow ramp input signal is described analytically in (8) and (10), respectively.

III. Effects of Interconnect Resistance

The waveform shape of the output voltage of a CMOS inverter as expressed in (8) is degraded with increasing interconnect resistance due to the $\frac{V_{dd}}{2} - RI_{DSAT}$ term in (8), where the output voltage decreases due to the RI_{DS} term in the saturation region as compared to a capacitive load [7], [14]. Therefore, the interconnect resistance reduces the time during which a CMOS inverter remains in the saturation region. This effect is called resistive shielding [15], where a portion of the load capacitance is shielded in the saturation region when the load resistance is comparable to the effective output resistance of a CMOS logic gate.

The second effect of the interconnect resistance is the degraded waveform shape of the output voltage. If the interconnect resistance is comparable to the effective output resistance of a CMOS inverter, *i.e.*, $V_{DSAT} \approx RI_{DSAT}$, the time constant τ in region IV can be approximated as

$$\tau = \frac{3V_{DSAT}}{2I_{DSAT}}C. \tag{11}$$

The time constant τ increases by almost 50% if the load is primarily capacitive. Therefore, the signal quality has a deleterious effect on the following logic stage because the MOS transistors of the following stage cannot turn off quickly due to the slow transition time of the input signal. Extra short-circuit power and subthreshold current at the following logic stage occur. Therefore, it is important to include short-circuit power in the analysis of the total transient power consumption when the interconnect is modeled as a resistive-capacitive load [17].

IV. Application to Circuit Analysis

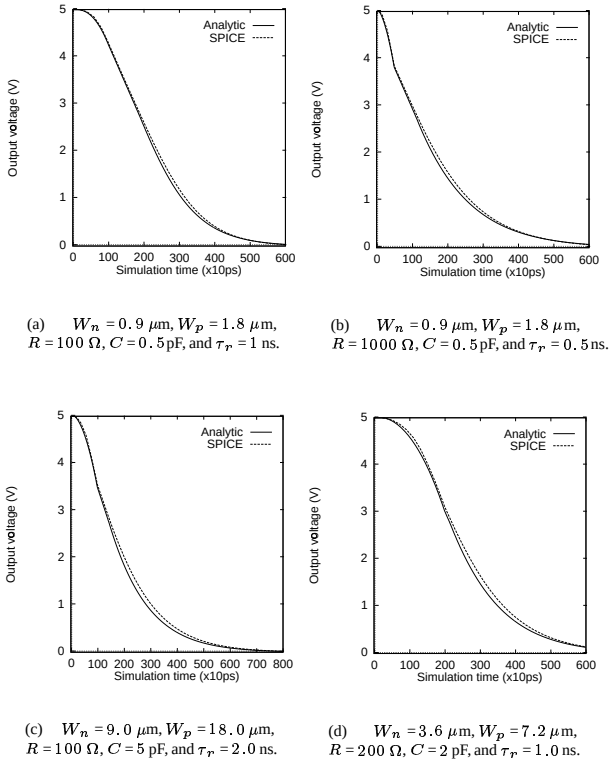
Closed form expressions of the output voltage for a fast ramp input signal, as discussed in subsection II-A, are compared with SPICE simulations in this section. Analytic expressions of the high-to-low propagation delay for both a fast ramp and a slow ramp input signal, expressed in (8) and (10), respectively, are evaluated for different transistor sizes, input transition times, and load conditions.

A. Output Voltage of a CMOS Inverter

The definition of a fast ramp input signal is based on the relationship between the input transition time τ_r and the time τ_{sat}. There are two terms in the expression of τ_{sat}. The first term is proportional to the load capacitance and decreases as the load resistance increases. The second term is proportional to the input transition time τ_r. To determine whether an input is a fast ramp signal, the input transition time τ_r is not the only concern because the decision also depends upon the load conditions. Even for the same input transition time τ_r, different conclusions exist under different load conditions.

For a fast ramp input signal, the output voltage of a CMOS inverter based on these analytic equations is compared with SPICE simulations. The results are shown in Fig. 2. In Fig. 2(a), the load condition is $R = 100\ \Omega$, $C = 0.5$ pF, the input transition time $\tau_r = 1$ ns, and $W_n = 0.9\ \mu$m. For this case, $\tau_{sat} = 1.89$ ns, which is greater than τ_r, therefore the input is considered to be a fast ramp signal. For a large resistive load, the resulting simulation is depicted in Fig. 2(b), while the simulation in which the load is a large capacitance is illustrated in Fig. 2(c). For a medium resistive and capacitive load, the resulting simulation is shown in Fig. 2(d).

Note that the output voltage based on the analytic expression is quite close to the SPICE simulation for each condition. The relative accuracy of the analytic propagation delay model can be found in Table I. These analytic expressions can therefore be used to approximate the output voltage for a fast ramp input signal. These expressions avoid the computational complexity required by SPICE while providing intuition into the effects of the physical parameters and related circuit sensitivities.



(a) $W_n = 0.9\ \mu$m, $W_p = 1.8\ \mu$m, $R = 100\ \Omega$, $C = 0.5$ pF, and $\tau_r = 1$ ns.

(b) $W_n = 0.9\ \mu$m, $W_p = 1.8\ \mu$m, $R = 1000\ \Omega$, $C = 0.5$ pF, and $\tau_r = 0.5$ ns.

(c) $W_n = 9.0\ \mu$m, $W_p = 18.0\ \mu$m, $R = 100\ \Omega$, $C = 5$ pF, and $\tau_r = 2.0$ ns.

(d) $W_n = 3.6\ \mu$m, $W_p = 7.2\ \mu$m, $R = 200\ \Omega$, $C = 2$ pF, and $\tau_r = 1.0$ ns.

Fig. 2. Comparison of the output voltage to SPICE for a fast ramp input signal.

B. Propagation Delay Comparison with SPICE

The high-to-low propagation delay of a CMOS inverter driving a resistive-capacitive load is shown in Table I under a variety of transistor sizes, input transition times, and load conditions. The geometric width of both the NMOS and PMOS transistors is listed in the first two columns. The load resistance, load capacitance, and rise time of the input signal, respectively, are listed in the following three columns. Results of the SPICE simulations are listed in column six and in the seventh column, the high-to-low propagation delay estimated from (8) or (10) is listed. Whether the input is a fast ramp signal and the error of the delay model as compared to the SPICE simulations are listed in the final two columns.

The size of the NMOS transistor varies from $0.9\ \mu$m to $9.0\ \mu$m and the input transition time ranges from 0.5 ns to 2.0 ns. For a variety of load conditions, the error of the high-to-low propagation delay is less than 7% as compared to SPICE simulations. Note, in particular, the case of $W_n = 0.9\ \mu$m and $R = 300\ \Omega$ where the load resistance is greater than the effective output resistance of the CMOS inverter ($280\ \Omega$); the predicted delay based on the analytic model assuming a slow ramp input signal is still quite accurate.

V. Conclusions

The assumption of a fast ramp input signal, which is widely used in the transient analysis of CMOS logic gates, is quantified in this paper. A criterion for characterizing the input signal de-

TABLE I

HIGH-TO-LOW PROPAGATION DELAY OF A $0.5\,\mu m$ CMOS INVERTER

Transistor size					$t_{p_{HL}}$ (ns)			
W_n (μm)	W_p (μm)	R (Ω)	C (pF)	τ_r (ns)	SPICE	Analytic	Fast Ramp	Error (%)
0.9	1.8	100	0.5	0.5	1.51	1.47	Yes	2.6
0.9	1.8	500	0.5	0.5	1.32	1.27	Yes	3.7
0.9	1.8	1000	0.5	0.5	1.09	1.03	Yes	5.5
3.6	7.2	100	2.0	0.5	1.35	1.32	Yes	2.2
3.6	7.2	500	2.0	0.5	0.57	0.54	Yes	5.3
3.6	7.2	1000	2.0	0.5	0.17	0.16	No	5.8
9.0	18.0	100	5.0	0.5	1.12	1.08	Yes	3.8
9.0	18.0	200	5.0	0.5	0.57	0.54	Yes	5.5
9.0	18.0	300	5.0	0.5	0.24	0.23	No	4.2
0.9	1.8	100	0.5	1.0	1.58	1.53	Yes	3.2
0.9	1.8	500	0.5	1.0	1.38	1.33	Yes	3.6
0.9	1.8	1000	0.5	1.0	1.16	1.08	Yes	6.9
3.6	7.2	100	2.0	1.0	1.42	1.38	Yes	2.8
3.6	7.2	500	2.0	1.0	0.68	0.64	No	5.8
3.6	7.2	800	2.0	1.0	0.37	0.39	No	5.4
9.0	18.0	100	5.0	1.0	1.17	1.09	Yes	6.8
9.0	18.0	200	5.0	1.0	0.70	0.67	No	4.3
9.0	18.0	300	5.0	1.0	0.42	0.42	No	0.0
0.9	1.8	100	0.5	2.0	1.72	1.66	Yes	3.5
0.9	1.8	500	0.5	2.0	1.53	1.45	Yes	5.2
0.9	1.8	1000	0.5	2.0	1.28	1.21	Yes	5.8
3.6	7.2	100	2.0	2.0	1.57	1.38	Yes	3.8
3.6	7.2	500	2.0	2.0	0.89	0.90	No	1.1
3.6	7.2	800	2.0	2.0	0.62	0.64	No	3.2
9.0	18.0	100	5.0	2.0	1.28	1.21	Yes	5.4
9.0	18.0	200	5.0	2.0	0.90	0.90	No	0.0
9.0	18.0	300	5.0	2.0	0.67	0.68	No	1.5
Maximum error (%)								6.90
Average error (%)								3.96

pends upon the input transition time, the device parameters, and the load conditions. Simple, general, yet accurate analytic expressions characterizing the output voltage of a CMOS inverter driving a resistive-capacitive load under the condition of a fast ramp input signal are also presented.

Based on an analysis of the output voltage of a CMOS inverter, the effect of the interconnect resistance is evaluated. The interconnect resistance shields the load capacitance in the saturation region as compared to a purely capacitive load. In addition, the signal quality is also degraded by the interconnect resistance due to the slower waveform shape of the output voltage signal, causing additional short-circuit power and subthreshold current in the following logic stage.

The propagation delay for both a fast ramp and slow ramp input signal has also been presented. The error of the propagation delay model based on these analytic expressions as compared to SPICE is less than 7% for a variety of transistor sizes, input transition times, and load conditions.

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