Delay and Power Expressions Characterizing a CMOS Inverter Driving an RLC Load

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Abstract—**On-chip parasitic inductance has become an important design issue in high speed integrated circuits. On-chip inductance may degrade on-chip signal quality, affect transmission delay, and cause additional short-circuit power dissipation. The effects of on-chip inductance on the output voltage, propagation delay, and short-circuit power of a CMOS inverter are presented in this paper. Analytic equations characterizing the output voltage are derived based on an assumption of a fast ramp input signal. Closed form expressions describing the short-circuit power are also presented. The accuracy of these analytic equations is within 10% as compared to SPICE simulations. It is demonstrated that large inductive loads and fast input transition times can increase short-circuit current.**

I. Introduction

As integrated circuit technologies continue to improve, the feature size of MOS transistors and interconnect lines has decreased. Since the chip size as well as the integration density have increased dramatically, the average interconnect length has not scaled with feature size. On-chip interconnect has therefore become increasingly important [1].

If the transition times in high speed VLSI circuits are comparable to the time of flight of the signals propagating along a low resistivity interconnect line (or the inductive time constant of an interconnection exceeds the resistive time constant), the inductance should also be considered in the interconnect model [2–5]. The interconnect in these high speed circuits should therefore be modeled as a lumped or distributed RLC line.

In order to evaluate the effects of on-chip inductance on the behavior of a CMOS inverter, the interconnect is modeled here as a lumped RLC, which is the load impedance of an interconnect line. The nth power law model [6] is used to characterize the submicrometer MOS transistors. The nth power law model is more accurate in the linear region and in determining the drain-to-source saturation voltage as compared to the alpha power law model [7], avoiding any discontinuity between the linear and saturation regions. Large inductive loads and fast input transition times can result in significant short-circuit currents. The short-circuit power of a CMOS inverter driving a lossless transmission line is presented in [8], in which the device is modeled by the alpha power law model. The short-circuit current is included in the analytic expressions characterizing the output voltage. Analytic expressions for the short-circuit power are derived based on the load conditions and the shape of the input waveform. The waveform of the output voltage based on these analytic equations is quite close to SPICE for fast ramp input signals. The predicted propagation delay is within 10% and the estimated peak short-circuit current is less than 7% as compared to SPICE.

The closed form expressions characterizing the output voltage and propagation delay of a CMOS inverter driving an RLC load are addressed in Section II. The effects of the inductive load on the output voltage, propagation delay, and short-circuit power are discussed in Section III. A discussion of the short-circuit power is addressed in Section IV followed by some concluding remarks in Section V.

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II. Waveform Shape of the Output Voltage

The equivalent circuit of a CMOS inverter driving an RLC load is shown in Fig. 1. R, L, and C are the effective load resistance, inductance, and capacitance of an interconnect line, respectively. V_o and V_1 are the output voltage of the CMOS inverter and the voltage across the load capacitance C, respectively. The input voltage is a ramp signal,

$$V_{in}(t) = \frac{t}{\tau_r} V_{dd} \qquad \text{for} \qquad 0 \le t \le \tau_r, \tag{1}$$

where τ_r is the rise time of the input signal.

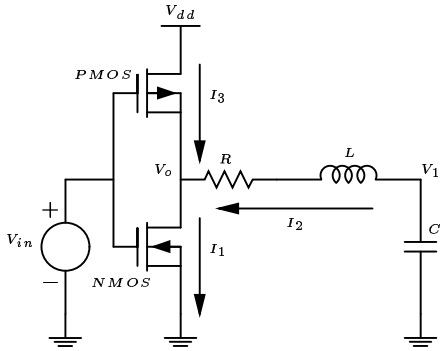


Fig. 1. A CMOS inverter driving an RLC load

A fast ramp signal is assumed in this discussion, where the input slope exceeds one-third of the output slope [9]. The effect of the PMOS transistor is neglected based on this assumption of a fast ramp input signal.

If the input voltage is greater than V_{TN}, the NMOS transistor is ON and operates in the saturation region. The output voltage satisfies the following KVL and KCL equations,

$$V_1(t) = L\frac{dI_{DS}}{dt} + RI_{DS} + V_o(t), \tag{2}$$

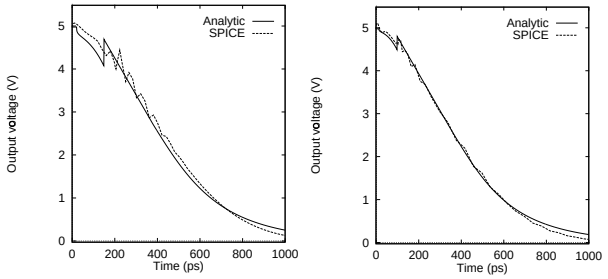
$$C\frac{dV_1(t)}{dt} = -I_{DS}. \tag{3}$$

The solution of $V_o(t)$ is

$$\begin{aligned} V_o(t) &= V_{dd} - V_c(t) - V_r(t) - V_l(t), \\ V_c(t) &= \frac{B_n \tau_r}{C(n_n+1)V_{dd}} \left(\frac{t}{\tau_r} V_{dd} - V_{TN}\right)^{n_n+1}, \\ V_r(t) &= RB_n \left(\frac{t}{\tau_r} V_{dd} - V_{TN}\right)^{n_n}, \\ V_l(t) &= LB_n \frac{n_n V_{dd}}{\tau_r} \left(\frac{t}{\tau_r} V_{dd} - V_{TN}\right)^{n_n-1}, \end{aligned} \tag{4}$$

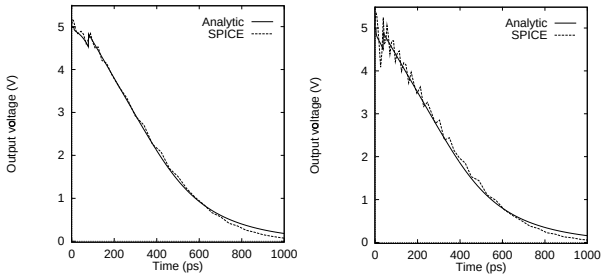
where $\tau_n \le t \le \tau_r$. τ_n is the time for the input voltage to reach V_{TN}.

After τ_r, the input voltage is fixed at V_{dd} and the NMOS transistor continues to operate in the saturation region. Therefore, the discharge current is equal to the saturated drain-to-source



(a) τ_r = 150 ps, R = 10 Ω, L = 4 nH, and C = 1 pF.

(b) τ_r = 100 ps, R = 10 Ω, L = 2 nH, and C = 1 pF.



(c) τ_r = 80 ps, R = 5 Ω, L = 1 nH, and C = 1 pF.

(d) τ_r = 40 ps, R = 5 Ω, L = 1 nH, and C = 1 pF.

Fig. 2. Comparison of the analytically derived output voltage with SPICE simulations.

current of the NMOS transistor, *i.e.*, I_{nsat}, which is a constant. The output voltage $V_o(t)$ in this region is

$$V_o(t) = V_1(\tau_r) - \frac{B_n}{C}(V_{dd} - V_{TN})^{n_n}(t - \tau_r) - RB_n(V_{dd} - V_{TN})^{n_n}, \quad (5)$$

where

$$V_1(\tau_r) = V_{dd} - \frac{B_n \tau_r (V_{dd} - V_{TN})^{n_n+1}}{C(n_n + 1)V_{dd}}, \quad (6)$$

and $\tau_r \leq t \leq \tau_{nsat}$. τ_{nsat} is the time when the NMOS transistor leaves the saturation region and is determined from (5).

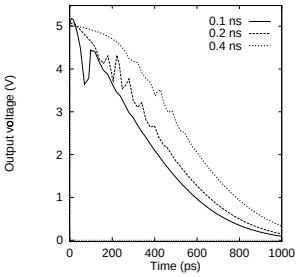
After V_o drops below V_{nsat}, the NMOS transistor enters the linear region. However, there is no tractable solution of (2) and (3) in this region. In order to derive an analytic solution, the drain-to-source current of the NMOS transistor is approximated by the effective output conductance γ_n. The output voltage in this region is therefore

$$V_o = K_1 e^{-\alpha_1 t} + K_2 e^{-\alpha_2 t} \qquad \text{for} \quad t \geq \tau_{nsat}, \quad (7)$$

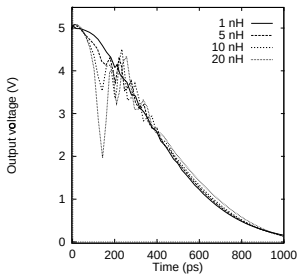
where

$$\alpha_1 = \frac{\frac{1+R\gamma_n}{L\gamma_n} + \sqrt{(\frac{1+R\gamma_n}{L\gamma_n})^2 - \frac{4}{LC}}}{2},$$
$$\alpha_2 = \frac{\frac{1+R\gamma_n}{L\gamma_n} - \sqrt{(\frac{1+R\gamma_n}{L\gamma_n})^2 - \frac{4}{LC}}}{2}. \quad (8)$$

K_1 and K_2 can be determined from $V_o(\tau_{nsat})$ and $V_o'(\tau_{nsat})$.



(a) Dependence of the output voltage on the input ramp time. The solid line, dashed line, and dotted line are for 0.1 ns, 0.2 ns, and 0.4 ns, respectively.



(b) Dependence of the output voltage on the inductive load. The inductive loads are 1 nH, 5 nH, 10 nH, and 20 nH from the top to the bottom line, respectively.

Fig. 3. Dependence of the output voltage on the input ramp time and the inductive load.

However, the effective output conductance of the NMOS transistor in (8) depends upon the output voltage in the linear region, changing from γ_{sat} to $2\gamma_{sat}$. Therefore, in order to accurately characterize the output voltage, γ_n in (8) is chosen between γ_{nsat} and $2\gamma_{nsat}$.

The output voltages predicted by these analytic expressions are compared to SPICE simulations. The results are shown in Fig. 2. Note that the output voltage waveforms are quite close to the waveforms derived from the SPICE simulations.

The propagation delay can be determined from the waveform of the output voltage described by (5). The output voltage in the linear region is described by (7). $t_{0.5}$ can be determined from (7) using a Newton-Raphson iteration. However, α_1 is typically much greater than α_2, therefore the output voltage can be approximated as a single pole system in the linear region,

$$V_o = V_{nsat} e^{-\alpha_2 (t - \tau_{nsat})}. \quad (9)$$

The high-to-low propagation delay $t_{p_{HL}}$ of a CMOS inverter is

$$T_{p_{HL}} = \frac{1}{\alpha_2} ln \frac{2V_{nsat}}{V_{dd}} + \tau_{nsat} - \frac{\tau_r}{2}. \quad (10)$$

III. Effects of an Inductive Load

An inductive load may cause large short-circuit currents if the input transition time is short, as described by the term $V_i(t)$ in (4). SPICE simulation results depicted in Figs. 3(a) and 3(b) demonstrate that for a fast ramp input signal or a large inductive load, the short-circuit current cannot be neglected. The spikes shown in Figs. 3(a) and 3(b) are caused by large short-circuit currents.

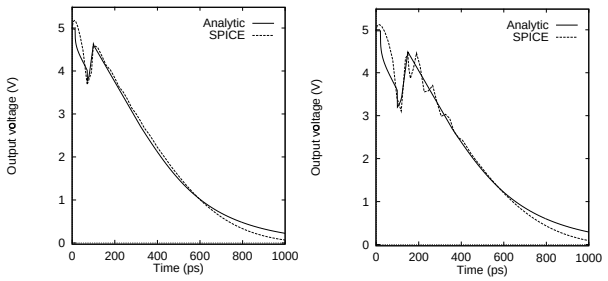
The short-circuit current I_3 through the PMOS transistor reduces the discharge current I_2, as shown in Fig. 1. The PMOS transistor operates in the linear region when the NMOS transistor turns on initially (assuming a fast ramp input signal). The current through the PMOS transistor can be approximated by an effective output conductance in the linear region,

$$I_3 \approx \alpha_p \frac{B_p}{K_p}(V_{dd} - \frac{t}{\tau_r} V_{dd} - V_{TP})^{n_p - m_p}(V_{dd} - V_o), \quad (11)$$

where α_p is between 1.0 and 2.0 depending upon V_o and V_{TP} is the absolute value of the PMOS threshold voltage.

The relationship between $V_o(t)$ and the current through the NMOS transistor I_1, the discharge current I_2, and the short-circuit current I_3 is

$$-\frac{I_2}{C_L} - \frac{dV_o(t)}{dt} = R\frac{dI_2}{dt} + L\frac{d^2 I_2}{d^2 t} \quad \tau_n \leq t \leq \tau_{poff}, \quad (12)$$



(a) τ_r = 100 ps, R = 10 Ω, C = 1 pF, and L = 5 nH.

(b) τ_r = 150 ps, R = 20 Ω, C = 1 pF, and L = 10 nH.

Fig. 4. Comparison of the analytically derived output voltage with SPICE simulations.

where τ_{poff} is the time when the PMOS transistor turns off. In order to simplify this analysis, the voltage across the load capacitance $V_1(t)$ is assumed to remains at V_{dd} when the PMOS transistor operates in the linear region. To derive an analytic solution of $V_o(t)$, it is assumed that $V_o(t)$ changes sufficiently slowly such that $\frac{dV_o(t)}{dt}$ can be neglected. The approximate solution is listed in Table I.

If $V_{dd} - V_o(t)$ is greater than $V_{psat}(t)$, the PMOS transistor starts operating in the saturation region. V_1 is no longer assumed to remain at V_{dd} after τ_{psat}. The analytic solutions of $V_o(t)$ and $V_1(t)$ during the input transition are listed in Table I, where K_3, K_4, K_5, and K_6 can be determined from the initial conditions of $V_o(t)$ and $V_1(t)$, respectively. The output voltage based on the analytic expressions listed in Table I is compared to SPICE for a large inductive load, as shown in Fig. 4. Note that these analytic expressions predict the voltage spike during the input transition, permitting the peak short-circuit current to be accurately estimated.

Similar to the analysis used in Section II, τ_{nsat} is determined based on $V_1(\tau_r)$. The propagation delay can also be determined by (10). The load inductance affects the propagation delay of a CMOS inverter as described in (10). These analytic expressions are used to estimate the propagation delay of a CMOS inverter. The estimated delays as compared to SPICE simulations are shown in Table II. The error is within 10% for most of the operating regimes.

TABLE II
PROPAGATION DELAY OF A CMOS INVERTER DRIVING AN RLC LOAD

τ_r (ps)	R (Ω)	L (nH)	C (pF)	$t_{p_{HL}}$ (ps) SPICE	$t_{p_{HL}}$ (ps) Analytic	Error %
40.0	5.0	1.0	1.0	344.0	329.0	4.36
50.0	5.0	1.0	1.0	377.0	353.0	6.37
50.0	5.0	2.0	1.0	350.0	323.0	7.71
50.0	10.0	5.0	1.0	325.0	305.0	6.16
50.0	20.0	5.0	1.0	325.0	302.0	7.08
100.0	30.0	10.0	1.0	325.0	351.0	8.00
100.0	20.0	10.0	1.0	322.0	353.0	9.63
100.0	10.0	10.0	1.0	322.0	356.0	10.56
100.0	20.0	10.0	2.0	678.0	695.0	2.51
150.0	20.0	10.0	1.0	419.0	390.0	6.92
Maximum error						10.56
Average error						6.90

IV. SHORT-CIRCUIT POWER

A DC path from V_{dd} to ground exists when the input signal transitions from low-to-high or from high-to-low. The short-circuit current cannot be neglected because short transition times and large inductive loads can cause a significant amount of short-circuit current [8].

To develop an expression for the short-circuit power, the NMOS transistor is assumed to operate in the saturation region during most of the time when the short-circuit current flows. Based on this assumption, the expressions listed in Table I can be used to approximate the output voltage to provide an expression for the short-circuit power dissipation. The short-circuit power during the high-to-low transition $P_{sc_{HL}}$ is

$$P_{sc_{HL}} = fV_{dd} \int I_p(t)dt, \tag{28}$$

where f is the switching frequency of the inverter and $I_p(t)$ is the current through the PMOS transistor.

During the time interval from τ_n to τ_{psat}, the PMOS transistor operates in the linear region. $I_p(t)$ can be expressed as

$$I_p(t) = I_{psat}(2 - \frac{V_{DSP}(t)}{V_{psat}})\frac{V_{DSP}(t)}{V_{psat}}. \tag{29}$$

This integral does not have an analytic solution after substituting $I_p(t)$ from (29).

The peak short-circuit current occurs in the time interval between τ_n and τ_{psat} because $I_p(t)$ decreases from τ_{psat} to τ_{poff}. The time when the peak current occurs can be determined from (29),

$$I_p'(t_{peak}) = 0. \tag{30}$$

This equation can be solved by using a Newton-Raphson iteration which requires only two to four iterations to obtain the solution of t_{peak}, permitting the peak short-circuit current to be determined.

However, based on the assumption that the peak current occurs near the middle of the input waveform for a balanced inverter [10], the peak current is

$$I_{peak} = B_p(\frac{V_{dd}}{2} - V_{TP})^{n_p}(2 - \frac{V_{DSP}(\frac{\tau_r}{2})}{K_p(\frac{V_{dd}}{2} - V_{TP})^{m_p}}) \frac{V_{DSP}(\frac{\tau_r}{2})}{K_p(\frac{V_{dd}}{2} - V_{TP})^{m_p}}. \tag{31}$$

Note, consistent with the literature [9], that the peak short-circuit current depends on both the input waveform shape and the load impedance.

Knowing I_{peak}, the short-circuit current $I_{sc}(t)$ can be approximated by the area of a triangle [10]. The short-circuit power during the high-to-low transition can therefore be approximated by the product of the area of the triangle and V_{dd}, *i.e.*,

$$P_{sc_{HL}} = \frac{1}{2} I_{peak}(\tau_{poff} - \tau_n)V_{dd}f, \tag{32}$$

where f is the switching frequency of the inverter and I_{peak} is determined from (30) or (31).

The peak current based on these analytic equations is compared to SPICE simulations and the results are listed in Table III. The analytic results of the final three rows are calculated from (30). The accuracy of these analytic expressions is within 7% of SPICE.

TABLE I

ANALYTIC EXPRESSIONS OF THE OUTPUT VOLTAGE INCLUDING THE SHORT-CIRCUIT CURRENT

Time region	Analytic expressions of the output voltage $V_o(t)$ and $V_1(t)$
$\tau_n \leq t \leq \tau_{psat}$	$V_o(t) = V_{dd} - \frac{RI_1 + LI_1'}{1 + R\gamma_p - L\gamma_p'}$ (13) $I_1' = \frac{B_n n_n V_{dd}}{\tau_r}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n - 1}$ (14) $\gamma_p = \frac{\alpha_p B_p}{K_p}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p - m_p}$ (15) $\gamma_p' = \frac{\alpha_p B_p (n_p - m_p) V_{dd}}{K_p \tau_r}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p - m_p - 1}$ (16)
$\tau_{psat} \leq t \leq \tau_{poff}$	$V_o(t) = K_3 - \frac{V_{0,1}(t)}{C} - RV_{o,2}(t) - LV_{o,3}(t)$ (17) $V_{o,1}(t) = \frac{B_n \tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n+1)} + \frac{B_p \tau_r}{(n_p + 1)V_{dd}}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{(n_p+1)}$ (18) $V_{o,2}(t) = B_n(\frac{t}{\tau_r}V_{dd} - V_{TN})^{n_n} - B_p(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{n_p}$ (19) $V_{o,3}(t) = \frac{B_n n_n V_{dd}}{\tau_r}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n-1)} + \frac{B_p n_p V_{dd}}{\tau_r}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{(n_p-1)}$ (20) $V_1(t) = K_4 - \frac{V_{1,1}(t)}{C}$ (21) $V_{1,1}(t) = \frac{B_n \tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n+1)} + \frac{B_p \tau_r}{(n_p + 1)V_{dd}}(V_{dd} - \frac{t}{\tau_r}V_{dd} - V_{TP})^{(n_p+1)}$ (22)
$\tau_{poff} \leq t \leq \tau_r$	$V_o(t) = K_5 - \frac{V_{0,4}(t)}{C} - RV_{o,5}(t) - LV_{o,6}(t)$ (23) $V_{o,4}(t) = \frac{B_n \tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n+1)}$ (24) $V_{o,6}(t) = \frac{B_n n_n V_{dd}}{\tau_r}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n-1)}$ (25) $V_1(t) = K_6 - \frac{V_{1,2}(t)}{C}$ (26) $V_{1,2}(t) = \frac{B_n \tau_r}{(n_n + 1)V_{dd}}(\frac{t}{\tau_r}V_{dd} - V_{TN})^{(n_n+1)}$ (27)

TABLE III

PEAK SHORT-CIRCUIT CURRENT OF A CMOS INVERTER DRIVING AN RLC LOAD. THE ASTERISKS DENOTE THE USE OF (30) TO ANALYTICALLY DETERMINE THE PEAK CURRENT. ALL OTHER VALUES ARE DETERMINED FROM (31).

				I_{peak} (mA)		Error
τ_r (ps)	R (Ω)	L (nH)	C (pF)	SPICE	Analytic	%
150.0	20.0	10.0	1.0	2.04	1.92	5.89
100.0	30.0	10.0	1.0	2.70	2.62	2.96
100.0	20.0	10.0	1.0	2.70	2.68	0.74
100.0	10.0	10.0	1.0	2.70	2.56	5.19
100.0	20.0	10.0	2.0	2.62	2.59	1.15
50.0	10.0	5.0	1.0	3.38	3.20*	5.30
50.0	20.0	5.0	1.0	3.36	3.15*	6.25
40.0	5.0	1.0	1.0	4.2	4.01*	4.52
Maximum error						6.25
Average error						3.97

V. CONCLUSIONS

The effects of on-chip inductance on a CMOS inverter are discussed in terms of the output voltage, propagation delay, and short-circuit power. Fast transition times and large inductive loads increase the short-circuit current. A simple technique is presented to estimate the short-circuit power based on the peak short-circuit current. Analytic expressions for the output voltage are derived for a CMOS inverter driving an RLC load. The propagation delay based on these analytic equations is within 10% as compared to SPICE simulations. The error of the estimated peak short-circuit current is less than 7%.

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