Physical Design to Improve the Noise Immunity of Digital Circuits in a Mixed-Signal Smart-Power System

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Abstract— **Theoretical, simulation, and experimental analysis and data are presented, discussing physical design techniques which influence the noise behavior of digital circuits in a mixed-signal smart-power system. Several physical design strategies are presented to improve the noise immunity of digital circuits in smart-power systems.**

I. Introduction

Existing research in substrate coupling noise in mixed-signal circuits has concentrated on the problem of the high speed digital circuitry influencing the highly sensitive analog circuitry [1–6]. It has been demonstrated in the literature that physical design plays an important role in minimizing the influence of substrate noise generated by the digital circuitry, affecting the highly sensitive analog circuitry [1–6].

A number of articles [1–5] have reported experimentally observed noise waveforms caused by the high speed switching of the on-chip digital CMOS circuits in mixed-signal systems. A typical noise waveform, both experimentally observed and simulated, is shown in Fig. 1. Note that the noise spikes are generated during the digital signal transitions when the circuit dissipates transient power and a current path exists from V_{DD} to GND. No substrate noise is generated while the digital signal is high or low.

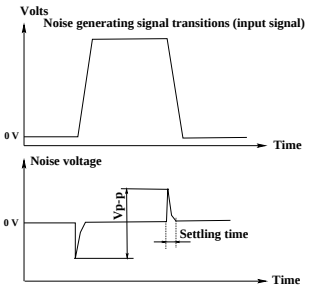

Fig. 1. A typical noise waveform caused by digital switching.

The presence and placement of substrate contacts have been shown to have a major influence on the magnitude and propagation characteristics of the substrate noise. The current flow lines for the generated noise for two typical substrates are shown in Fig. 2 [1]. An analysis of the placement of the substrate contacts has been performed in [4], and the results are shown in Fig. 3. Note that the noise level in the substrate increases as the distance between the noise source and the noise receptor d_{S-R} decreases, and as the distance between the substrate contacts or backside contact and the noise source d_{S-SB} and/or the noise receptor d_{R-SB} increases. The effect of the routing of the power supply lines has also been studied in [6, 7], permitting several rules to be developed. The orientation and placement of the noise sensitive blocks with respect to the noise source have been clearly shown to be significant [2].

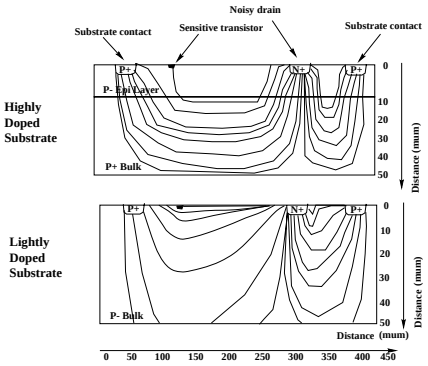

Fig. 2. The current flow lines for a highly doped and a lightly doped substrate

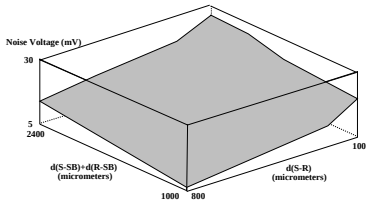

Fig. 3. Dependence of noise on the placement of the substrate contacts

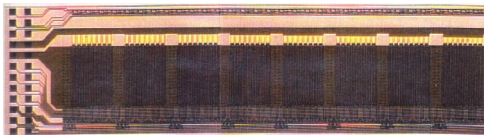

Fig. 4. Microphotograph of NMOS test circuit

The noise tolerance of digital circuits in a mixed-signal smart-power application has been analyzed in [8, 9]. A microphotograph of a test circuit is shown in Fig. 4. The following issues have been demonstrated to significantly influence the noise tolerance of digital circuits: 1) the noise transmission characteristics through the substrate, in particular the presence of a difference of phase and magnitude of the noise at different transistors, 2) the magnitude, sign (positive or negative), and duration of the noise spikes, 3) certain circuit aspects such as the logic family, transistor size, and load impedance, 4) the distance, placement, and orientation of the sensitive digital

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blocks with respect to the noise source and substrate contacts, and 5) the routing and connectivity of the ground lines of both the digital and high-power analog blocks. The primary objective of this paper is determining and interpreting the physical design issues that affect the operation of circuits, specifically the noise sensitivity of the digital circuits. A secondary objective is to develop physical design techniques to minimize this noise sensitivity.

Certain aspects of the design process as well as a description of the test circuits are described in Section II. Experimental results and discussions are presented in Section III. Physical design solutions to minimize the deleterious effects of noise are presented in Section IV. Some conclusions are offered in Section V.

II. The test circuits

The experimental results used to characterize the noise sensitivity of digital circuits in smart-power systems have been described in [8, 9] in terms of the *number of affected registers*. The experimental results described in this paper characterize the substrate noise waveforms under different test conditions, and correlate these waveforms with the results presented in [8, 9].

The floorplan of the test circuits is shown in Fig. 5a. These circuits have been designed and manufactured to determine the principal characteristics of the noise generation process. The difference in amplitude and phase of the substrate noise throughout the substrate has been investigated for different test conditions and physical design issues.

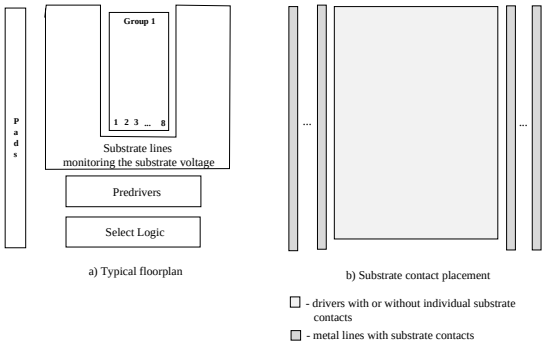

Fig. 5. Test circuits: a) the floorplan of the substrate voltage monitoring test circuits, and b) the placement of the substrate contacts within the test circuits

As described in [9], the substrate voltage required to induce a parasitic transition in a logic element is on the order of volts, permitting a simple approach to measure the substrate noise levels and the characteristic substrate waveforms. Fourteen metal lines connected to the substrate, *line1* to *line14*, surround a group of eight drivers. Each of the lines uses a dedicated pad to access the substrate voltage on that line. The noise distribution generated through the substrate by the switching of the drivers is determined from observing these 14 lines. The noise difference at a number of substrate points can also be determined. Each one of the eight drivers is individually selected so that up to all eight drivers can be selected at a given time in order to vary the noise magnitude [8]. As shown in Fig. 5b, the only substrate contacts in the circuit are placed near each of the power drivers and at the 14 metal lines. If any metal line is not connected externally to ground, the substrate contacts associated with that metal line are inactive from a noise point of view.

The nominal power supply for the power driver is 38 volts [10]. To efficiently drive the power transistor and to ensure a sufficient voltage swing at the gate of the power transistor, a 13 volt predriver is used to drive the power transistor. The predriver is controlled by 5 volt digital logic circuits. The circuit schematic depicting a power driver and the predriver that drives the power driver is shown in Fig. 6.

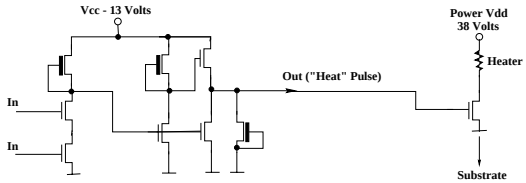

Fig. 6. The predriver-driver circuit

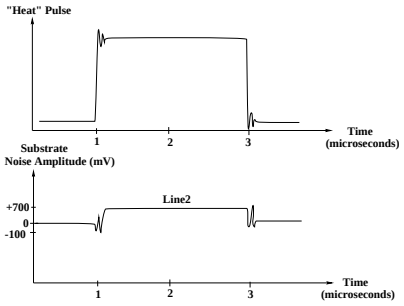

Fig. 7. The substrate bias generated by a power transistor operating in the linear region

The power transistors switch up to 38 volts and 100 mA. These transistors operate in the linear region when *on*, drawing about 100 mA with current peaks greater than 100 mA during the on/off transition cycles. Note that it is important to operate the power transistor in the linear region with a negligible V_{DS} so as to minimize the on-chip power dissipation. In the test circuits, V_{DS} across two out of the eight power drivers is monitored.

III. Experimental results and discussion

An experimentally observed effect is illustrated in Fig. 7. The power driver transistor operates in the linear region (the "Heat" pulse is high, see Figs. 6 and 7), generating an approximately constant substrate noise level that biases the substrate for the duration when the power driver is ON. The substrate bias level increases as the current through the power driver increases, and as the distance from the power driver to the line that monitors the substrate noise increases. The effect of a 6 mA current, corresponding to a power supply of 4 volts, is shown in Fig. 7. V_{DS} across the power transistor for this situation is ≈ 1.5 volts. The substrate noise voltage measured for line2 is ≈ 700 mV, while for line14, farther from the noise source, is ≈ 900 mV. These noise levels are obtained for the condition when eight power drivers are active.

For power supplies larger than six volts, the effect exemplified in Fig. 8 is noted. The substrate noise amplitude oscillates around the approximately constant noise level shown in Fig. 7. This oscillation is related to the V_{DS} variations across the power driver transistor as shown in Fig. 8. Consider the power supply voltage (or alternatively V_{DS}) of the power driver to be 34 V (the V level shown in Fig. 8). For this power supply, the substrate noise varies between $V_a = 4$ volts and $V_b = -3.2$ volts, while V_{DS} varies between $V_1 = 62$ volts and $V_2 = 12$ volts. Note that the overshoots in V_{DS} exceed levels greater than 60 volts. Undershoots of up to - 800 mV have also been observed. While these levels are for line 2, the same values are within 15% for each of the fourteen lines. A difference in phase of up to 80 ns is also noted between the noise waveforms of any two lines. Eight power drivers are active in this experiment.

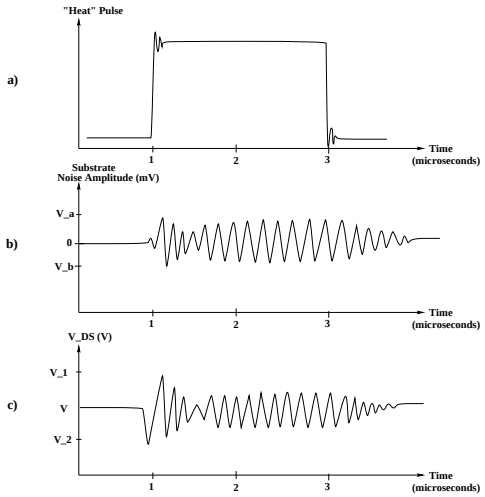

Fig. 8. Characteristic noise waveforms a) Input signal for the power transistor b) Substrate bias oscillation c) V_{DS} across the power transistor

Note that the substrate noise waveforms can be characterized by a steady state voltage superimposed over an oscillation. All of these waveforms are correlated with the saturation and linear regions of operation of the power transistor and with the V_{DS} variations of the power transistor. From Figs. 7 and 8 and the results presented in [9], it can be concluded that a linear transistor generates a constant substrate bias that does not affect the noise immunity of the digital circuits. It can also be concluded that noise spikes with large phase differences throughout the substrate are produced when the power transistor transitions from the linear region to the saturation region and from the saturation region to the linear region. Accordingly, these transitions of the power driver should be reduced to a minimum to improve the noise behavior of the digital circuits.

The oscillatory substrate noise waveform shown in Fig. 8 originates in the substrate-predriver-driver positive feedback loop. This loop is modeled by the circuit schematic shown in Fig. 9, where the V_{noise} voltage source models the induced substrate noise.

Using Fig. 9, the generation process of the oscillatory substrate waveform through the aforementioned positive feedback loop can be explained as:

- An initial positive substrate noise spike generated during the turn-on process of the power driver reaches the source of the power drivers. The predriver receives the noise attenuated and/or delayed by the parasitic RLC impedances of the ground lines.
- The initial V_{GS} at the input of a power driver transistor is reduced by the magnitude of the positive noise spike.
- A decrease in V_{GS} creates a decrease in I_{DS} and an increase in V_{DS}, which shifts the operating point of the power transistor from the linear region into the saturation region.
- Decreasing V_{GS} and increasing V_{DS} turns off the power transistor.
- Accordingly, the amount of generated noise decreases, decreasing V_{noise}, increasing I_{DS}, and returning the transistor to the linear region and to a small V_{DS}.
- This transition again produces a large amount of noise. This cycle, in which the power transistor switches from the linear region to the saturation region and back to the linear region, repeats until the predriver signal turns off and V_{GS} becomes zero.
- The oscillation remains while decreasing in amplitude once the predriver signal turns off. This behavior occurs since V_{noise} is sufficiently large to bias the power transistor when $V_{GS} = 0$. V_{noise} decreases in amplitude with each cycle until the oscillations disappear.

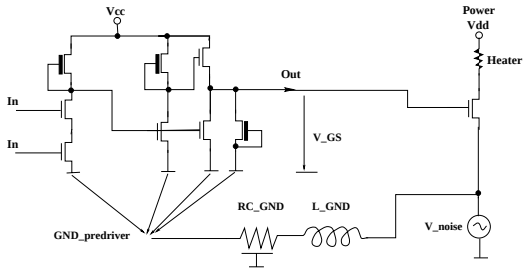

Fig. 9. The positive feedback loop responsible for the output oscillation

Note that these effects increase as the substrate voltage levels increase, and/or the voltage difference between the source of the power transistor and the GND of the predriver increases. All of these effects can be minimized by physical design techniques such as proper ground routing to minimize the voltage difference between certain sensitive ground nodes (such as the ground of the power driver and the ground of the corresponding predriver) and substrate contact placement to maintain a uniform and low amplitude noise distribution across the substrate.

The characteristics of the substrate noise waveform are experimentally shown to vary depending upon a variety of issues such as:

- By decreasing the power supply voltage from 34 volts to 4 volts, the frequency and amplitude of the oscillation, as shown in Fig. 8, also decreases. The same effects are obtained when the number of power drivers are decreased. For example, an oscillation is noted when the power supply reaches 6 volts with eight active drivers, 8 volts with

five active drivers, and 12 volts with three active drivers, while for one driver there are negligible oscillations even at 34 volts.

- Due to the high currents that are switched, any voltage drop on the metal lines can be significant, creating ground bounce and/or substrate voltage nonuniformities that are treated as V_{noise} voltages by the power drivers.
- The noise level is reduced by up to 400% if the line that monitors the noise is adjacent to a line at ground potential (17 μm is the distance used in the experiment).
- The noise reduction decreases in efficiency as the distance between the monitor line and the grounded line increases.
- If the distance between the monitor line and the grounded line is greater than 70 μm (four lines or 68 μm), almost no reduction in noise is noted.

As described in [9], a difference of phase and/or amplitude in the noise affecting two logic elements is the primary reason for a parasitic transition being induced. For an oscillatory noise waveform, each transition creates a situation where this difference of phase and/or amplitude may exist. Accordingly, an oscillatory noise waveform as shown in Fig. 8 has a greater effect on the noise sensitivity of a digital circuit than a waveform as shown in Fig. 1.

Several circuits have been designed to monitor the substrate noise waveforms at the same time as the number of affected registers are being monitored. Analyzing these circuits it has been experimentally demonstrated that the experimental results described in [8, 9] can be correlated with the existence, magnitude, and difference of phase of the oscillatory substrate noise waveform.

The different noise sensitivities of the digital circuits noted in [8] for both on-chip and off-chip connected grounds (the high power ground and the digital logic ground) can also be explained by an equivalent circuit schematic as shown in Fig. 9 with a V_{noise} voltage source. For the off-chip connected grounds, large RLC parasitic impedances (see Fig. 9) as compared to the on-chip connected grounds may exist, producing both IR and $L\frac{di}{dt}$ voltage drops and differences of phase between the two ground lines.

IV. Noise mitigation techniques

Based on the analysis and results presented here as well as in [8, 9], the noise sensitivity of digital circuits in a mixed-signal smart-power environment can be improved by employing several physical design techniques, such as:

- The ground routing should be implemented with thick and wide lines in low resistivity metal layers. This routing style will produce small RLC parasitic impedances which minimize ground biases and ground bounce effects. Special care in designing the ground distribution network should be given to minimize IR drops and $L\frac{di}{dt}$ effects.
- The grounds of the different circuit blocks, such as the ground of the drivers, predrivers, and logic blocks, should all be connected on-chip with minimal parasitic RLC impedances from one ground line to another ground line. The same routing style with a low resistivity metal is recommended in order to eliminate any effects associated with V_{noise} and the oscillatory substrate noise.
- Each transistor within a logic element should have a dedicated substrate contact in its vicinity, a standard analog design practice. These substrate contacts should be connected by a low resistivity metal layer. Significant beneficial effects are achieved with this technique, such as: 1) a reduction of the amplitude of the substrate noise, 2) a more uniform noise phase and amplitude for all of the relevant transistors, and 3) a reduction in V_{noise} effects and in the oscillatory noise waveforms.
- A compact layout is beneficial in improving the noise uniformity received by the different transistors since the RC substrate impedances among the transistors of each latch are minimized.
- If possible, it is recommended to place the noise sensitive digital circuitry as far from and/or as symmetric as possible with respect to the noise source. This floorplan will maintain a similar phase and magnitude of the noise for all of the transistors within the logic elements.

V. Conclusions

It is shown in this paper that physical design can play a significant role in managing the sensitivity of digital circuits to substrate noise in a mixed-signal smart-power environment. Several issues related to physical design that influence the operation of the circuits and which may generate large amounts of noise are theoretically and experimentally determined, modeled, and interpreted. Several noise mitigation techniques based on physical design strategies have also been suggested.

References

[1] D. K. Su and B. A. Wooley, "Experimental Results and Modeling Techniques for Substrate Noise in Mixed-Signal Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 28, No. 4, pp. 420–430, April 1993.

[2] X. Aragones and A. Rubio, "Analysis and Modelling of Parasitic Substrate Coupling in CMOS Circuits," *IEE Proceedings–Circuits, Devices and Systems*, Vol. 142, No. 5, pp. 307–312, October 1995.

[3] S. Masui, "Simulation of Substrate Coupling in Mixed-Signal MOS Circuits," *Proceedings of the IEEE International Symposium on VLSI Circuits*, pp. 42–43, June 1992.

[4] T. Blalack and B. A. Wooley, "Experimental Results and Modeling of Noise Coupling in a Lightly Doped Substrate," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 623–626, December 1996.

[5] K. M. Fukuda and M. Hotta, "Voltage-Comparator-Based Measurement of Equivalently Sampled Substrate Noise Waveforms in Mixed-Signal Integrated Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 31, No. 5, pp. 726–731, May 1996.

[6] B. R. Stanisic, N. K. Verghese, and D. J. Allstot, "Addressing Substrate Coupling in Mixed-Mode IC's: Simulation and Power Distribution Synthesis," *IEEE Journal of Solid-State Circuits*, Vol. 29, No. 3, pp. 226–238, March 1994.

[7] J. A. Olmstead and S. Vulih, "Noise Problems in Mixed Analog-Digital Integrated Circuits," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 659–662, May 1987.

[8] R. M. Secareanu, I. S. Kourtev, J. Becerra, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "Noise Immunity of Digital Circuits in Mixed-Signal Smart Power Systems," *Proceedings of the IEEE Great Lakes Symposium on VLSI* pp. 314–317, February 1999.

[9] R. M. Secareanu, I. S. Kourtev, J. Becerra, T. E. Watrobski, C. Morton, W. Staub, T. Tellier, and E. G. Friedman, "The Behavior of Digital Circuits under Substrate Noise in a Mixed-Signal Smart-Power Environment," *Proceedings of the IEEE International Symposium on Power Semiconductor Devices and ICs*, pp. 253–256, May 1999.

[10] E. Peeters and S. Verdonckt-Vandebroek, "Thermal Ink Jet Technology," *IEEE Circuits and Devices Magazine*, Vol. 13, No. 4, pp. 19–23, July 1997.