A CLOCK TREE TOPOLOGY EXTRACTION ALGORITHM FOR IMPROVING THE TOLERANCE OF CLOCK DISTRIBUTION NETWORKS TO DELAY UNCERTAINTY

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ABSTRACT

The design of clock distribution networks in synchronous systems presents enormous challenges. Control of the clock signal delay in the presence of various noise sources, process parameter variations, and environmental effects represents one of the fundamental problems in the design of high speed synchronous circuits. An algorithm that improves the tolerance of a clock distribution network to process and environmental variations is presented in this paper. The algorithm generates a clock tree topology that minimizes the uncertainty of the clock signal delay in the most critical data paths. Details of the algorithm and preliminary results on benchmark circuits are presented.

1. INTRODUCTION

The primary characteristic of the microelectronics revolution is the rapid decrease in device size, producing phenomenal increases in circuit density, functionality, and operational clock frequency [1, 2]. Scaling of the device geometries supports the system-on-a-chip integration of multiple subsystems [3, 4], greatly increasing the number of on-chip clocked elements. These effects have resulted in hundreds of thousands of elementary operations being executed in sequences specified by application-specific algorithms and controlled by a clock signal, operating within time periods of less than a nanosecond [5]. These constraints demonstrate the tight timing control of the arrival times of the clock signal at the many registers throughout the integrated circuit. Deviations of the clock signal from the target delay can cause incorrect data to be latched within a register, resulting in the system malfunctioning. Uncertainty of the clock signal delay is introduced by a number of factors that affect the clock distribution network, examples of which include process and environmental parameter variations [6, 7] and interconnect noise [8]. The sensitivity of a clock distribution network to these effects has therefore become an issue of fundamental importance to the synchronous design problem [9, 10].

There are a variety of sources of delay uncertainty in high speed integrated circuits [11]. Effects such as the nonuniformity of the interconnect lines and interlevel dielectric variations introduce uncertainty in the delay of the clock signal arriving at different registers. Environmentally induced parameter variations caused by changes in the ambient temperature and external radiation also produce delay uncertainty. On-chip noise due to inductance effects and coupling among interconnects introduces additional clock signal delay uncertainty as the clock frequency increases well beyond the one gigahertz frequency range.

In this paper, an algorithm that improves the tolerance of a clock distribution network to delay uncertainty is presented. The algorithm focuses on the topological design of a clock distribution network and the manner in which the topology affects the sensitivity of the network to delay uncertainty. The algorithm extracts the clock tree topology based on the temporal criticality of the data paths. The concept of the algorithm is summarized in Section 2. The algorithmic approach is described in Section 3. Preliminary results of the algorithm on benchmark circuits are presented in Section 4. Finally, some conclusions are presented in Section 5.

2. CONCEPT OF THE ALGORITHM

The issue of delay uncertainty in clock distribution networks is the uncertainty between the delay of the different clock paths that drive sequentially-adjacent registers connected by a combinational path. Intuitively, the effects of process and environmental parameter variations (PEPV) on the common portion of the clock tree introduce identical delays to the clock signals driving the sequentially-adjacent registers of a

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data path [10]. Alternatively, PEPV may introduce different clock delays on the portion of the clock tree that is not common. This concept is illustrated in Fig 1.

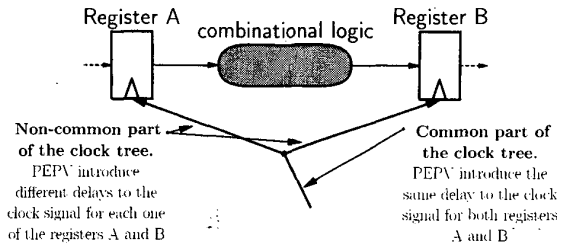


Figure 1: Introduction of different clock signal delays to non-common portions of the clock tree.

The more strict the setup and hold time constraints of a combinational data path, the more sensitive a data path is to delay uncertainty. A small difference in the clock signal delay can violate these constraints and cause a circuit to malfunction. The topology of the clock tree can also greatly affect the delay uncertainty [12]. In particular, when the common portion of two paths in a clock tree increases, the delay uncertainty at the leaves of these paths is likely to decrease. The algorithm presented in this paper relies on this principle to generate a clock tree topology with improved tolerance to PEPV. The objective of the algorithm is to minimize the delay uncertainty of these critical paths.

A synchronous digital circuit is represented in the algorithm as an edge-weighted graph G, which is called an *uncertainty graph*. An example of an uncertainty graph representation is shown in Fig. 2. Each node u in the graph G denotes a register in the circuit. Each edge $u \rightarrow v$ in G denotes a combinational path between the registers corresponding to u and v in the original circuit. The weight $w(u, v)$ of each edge represents the tolerance of the corresponding data path to PEPV and imposes a constraint on the delay uncertainty of the clock signals driving the registers u and v. In particular, for the circuit to function correctly, this uncertainty must not exceed $w(u, v)$. For example, the path corresponding to the edge 3→4 is critical, since the path can tolerate zero uncertainty in the clock delays of these bounding registers. Alternatively, the path 4→5 can tolerate up to 3 time units (tu) of delay uncertainty.

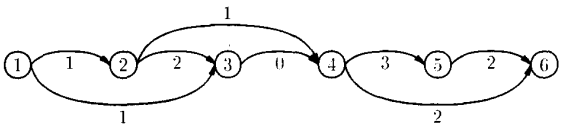


Figure 2: Graph representation of a circuit.

The algorithm relies on a topological delay uncertainty metric to generate clock trees that satisfy targeted uncertainty constraints. Specifically, given two paths, the delay uncertainty between the clock signals at the corresponding leaf nodes is assumed to be equal to the number of internal tree nodes (branch nodes) in the non-common portions of the paths. The basic assumption underlying this metric is that as the number of common tree nodes between two paths decreases, the delay uncertainty of these leaves increases.

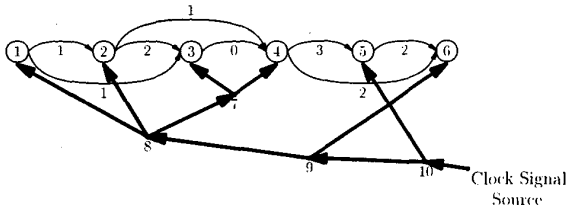


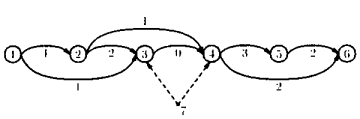
Figure 3: Clock tree topology for the circuit shown in Fig 2.

A clock tree topology that satisfies the delay uncertainty constraints of the graph shown in Fig. 2 is illustrated in Fig. 3. For example, consider the pair 2→4. The uncertainty constraints of this pair should not exceed one. The paths leading from the clock signal source to the two leaf nodes split at the internal node 8. The number of non-common branch nodes of the two paths is one (node 7). For the pair 4→6, the paths from the source split at node 9, and the number of non-common branch nodes is two (nodes 7 and 8), which is equal to the edge weight $w(4, 6)$. For the critical pair 3→4, the common paths split at node 7 and, as required, the number of non-common branch nodes is zero.

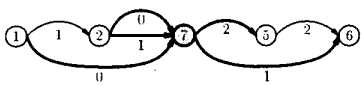
3. DESCRIPTION OF THE ALGORITHM

The algorithm presented in this section extracts the clock tree topology (CTT) by determining the hierarchy of the branch points of the tree such that the clocked elements of the most critical data paths share the greatest portion of the clock tree. The algorithm proceeds by iteratively selecting from the uncertainty graph those data paths with the minimum tolerance to PEPV. These paths correspond to the edges with the minimum edge weight. In each iteration, a new branch node is introduced, and the clock signals are distributed from that node to the selected registers. These branch nodes replace the selected register nodes. The edges entering or leaving the replaced nodes are redirected to the newly introduced node, and the edge weights are adjusted to reflect the new tolerance of these edges. The algorithm continues until only one node remains in the graph. The clock tree topology that satisfies all of the uncertainty constraints is obtained by unfolding the computation to establish the connections among the hierarchically introduced branch nodes.

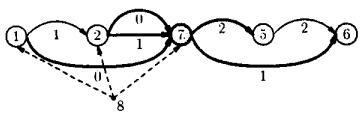
The execution of the proposed algorithm on the uncertainty graph shown in Fig. 2 is illustrated in Fig. 4. The algorithm starts with the graph shown in Fig. 4(a). The minimum-weight edge in this graph is between nodes 3 and



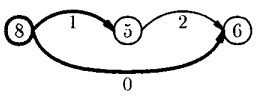
(a) **1st Iteration:** The clock signal is distributed to the registers of the most critical data path 3→4 from branch point 7.



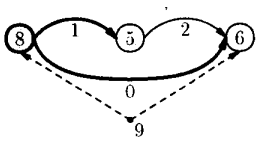
(b) Branch point 7 replaces the nodes that it drives within the graph. The weights of the redirected arches (**bold**) are reduced by one.



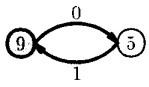
(c) **2nd Iteration:** The clock signal is distributed to the registers of the most critical data paths 1→7 and 2→7 from branch point 8.



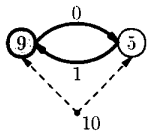
(d) Branch point 8 replaces the nodes that it drives within the graph. The weights of the redirected arches (**bold**) are reduced by one.



(e) **3rd Iteration:** The clock signal is distributed to the registers of the most critical data path 8→6 from branch point 9.



(f) Branch point 9 replaces the nodes that it drives within the graph. The weights of the redirected arches (**bold**) are reduced by one.



(g) **4th Iteration:** Only one node (10) is inserted in the graph. The algorithm terminates.

Figure 4: Iterations of the algorithm to reduce the input graph to a single node.

4. The clock signal is therefore distributed to these nodes from the new branch node 7. Node 7 is inserted in the uncertainty graph as shown in Fig. 4(b), replacing nodes 3 and 4. The edges leaving or entering nodes 3 and 4 are redirected to node 7. The weights of these edges are reduced by 1 tu, the amount of uncertainty introduced by the branch node 7. The iterative application of this basic procedure continues until only one node remains in the graph (node 10) as shown in Figs. 4(c) through 4(g). At this point, the algorithm extracts the final clock tree topology, which is shown in Fig. 3. Note that nodes 3 and 4 (corresponding to the most critical data path with zero tolerance to PEPV) share the greatest portion of the clock tree from the clock signal source to branch node 7. In the case of a less critical data path such as the path between nodes 4 and 6, the clock paths to the registers have in common a smaller portion of the clock tree.

The correctness of the CTT generation algorithm can be proved by an inductive argument showing that after each iteration, the portion of the clock tree that has been generated satisfies all relevant uncertainty constraints. The algorithm has polynomial complexity, terminating in $O(n^2)$ steps, where n is the number of nodes in the uncertainty graph. The number of iterations is n, and within each iteration, the number of updates is proportional to n.

4. PRELIMINARY RESULTS

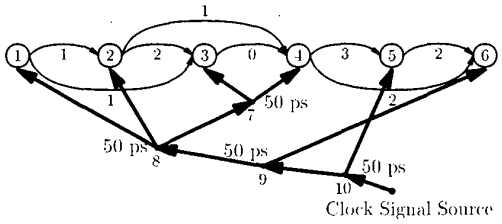
The capability of the proposed algorithm to reduce the non-common portion of the clock tree that drives the most critical data paths of a circuit is illustrated in Fig. 5. The topology generated by the proposed algorithm is compared with a binary tree topology under the assumption that the range of delay uncertainty of the clock signal on the branches immediately following a branch point is 50 ps. In this case, for the example shown in Fig. 5(a), the maximum range of clock delay uncertainty for the data paths, 1→3, 2→4, and 4→6, is reduced by 50 ps as compared with the binary tree topology shown in Fig. 5(b). This result produces a 33% reduction of the maximum delay uncertainty for the data paths, 1→3 and 2→4, and a 25% reduction for data path 4→6. The timing margins for those data paths can therefore be less strict for the circuit shown in Fig. 5(a). In this example, the clock period is not decreased due to the reduced delay uncertainty since the delay uncertainty for the most critical data path 3→4 is the same for both clock tree topologies.

The proposed algorithm has also been tested on a number of benchmark circuits. In these tests, the average reduction of the range of delay uncertainty for the most critical data paths is estimated for different levels of PEPV tolerance assigned to the circuit data paths. Additionally, the improvement in the delay uncertainty of the most critical data path is determined. This delay uncertainty can be excluded from the time budget required to ensure correct timing of the most critical data paths.

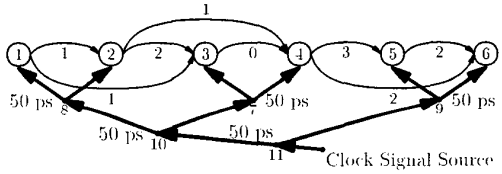
In evaluating the benchmark circuits it is assumed that the original clock tree topology for the benchmark circuits is a balanced tree and that there are up to four branches leaving each branch point within the clock tree. The results of this analysis are listed in Table 1. It is shown that the delay uncertainty of the most critical data paths can be reduced by up to 75%. The levels of tolerance to PEPV assigned to the

Table 1: Reduction in delay uncertainty for different PEPV tolerance levels

Benchmark Files	Number of Registers	Total number of nodes	Average reduction of delay uncertainty for the most critical paths (%)			Delay uncertainty improvement for the most critical data path
			PEPV=3	PEPV=5	PEPV=7	
Multi 16b	31	48	61.4%	60.9%	57.7%	0%
S27cp	3	8	41.6%	50.0%	50.0%	50%
S386	6	20	0%	28.5%	12.5%	0%
S641	19	77	23.5%	24.3%	16.6%	66%
S838_1	32	67	19.2%	17.6%	21.4%	0%
S838	32	69	26.4%	26.4%	33.3%	75%



(a) Algorithmically extracted clock tree topology for an arbitrary circuit



(b) Clock tree topology for the same circuit assuming a binary tree

Figure 5: Comparison between the algorithmically extracted CTT and a binary tree.

data paths are shown for each of the test cases. Note in Table 1 that as the complexity of the circuits increases, the per cent reduction in delay uncertainty decreases. This behavior is caused by the increased depth of the clock tree which increases the delay uncertainty among the clock branches.

5. CONCLUSIONS

An algorithm that generates a clock distribution network with high tolerance to process and environmental variations is presented. The algorithm extracts the clock tree topology in order to minimize the delay uncertainty of the clock signals that drive the most critical data paths. The hierarchy of the branch points of the clock tree is determined such that the clocked elements of the most critical data paths share the greatest portion of the clock tree. Preliminary results from the application of the algorithm to benchmark circuits demonstrate significant improvements in the tolerance of a circuit to process and environmental variations.

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