# LARGE SCALE CLOCK SKEW SCHEDULING TECHNIQUES FOR IMPROVED RELIABILITY OF DIGITAL SYNCHRONOUS VLSI CIRCUITS

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*Abstract*—This paper compares several methods for determining an optimal non-zero clock skew schedule for synchronous digital VLSI circuits. The optimality of a given clock skew schedule which satisfies the circuit timing constraints is defined from the perspective of circuit timing reliability. This optimality is characterized by the deviation of the computed clock schedule from an 'ideal' objective clock schedule. Both *linear* and *quadratic* programming (LP and QP) formulations of the clock skew scheduling problem are analyzed and a novel LP formulation is introduced. These formulations are compared using the ISCAS'89 suite of benchmark circuits. Mathematical optimization results are calculated using the large scale optimization package Lancelot.

## 1. INTRODUCTION

The work presented in this paper focuses on increasing the timing reliability of synchronous VLSI circuits by determining a feasible non-zero clock skew schedule. One such *ideal* non-zero clock skew schedule may be chosen by noting that there is an interval of feasible skew values—called the *permissible range*—for each data path [1]. The boundaries of a permissible range are determined by circuit structure but are affected because of process parameter variations and operating conditions such as temperature and supply voltage. The ideal clock skew schedule for reliability is considered to be the one in which the clock skew for a local data path is at the middle of the permissible range for this specific data path. Since the circuit timing constraints depend on the circuit topology, however, this ideal schedule is unlikely to also be feasible (that is, to satisfy all timing constraints). Various *linear programming* (LP) or *quadratic programming* (QP) formulations may be used to find a feasible non-zero clock skew schedule which is as close as possible to the ideal (and likely unfeasible) schedule.

This paper starts by presenting background information in Section 2 to highlight the relevant timing properties of synchronous circuits and the graph model used to represent these circuits. Following in Section 3 are descriptions of the mathematical formulations to be compared including the formal definitions of the LP and QP problems in Section 3.1 and Section 3.2, respectively. The C++ software implementation and analytic results from the ISCAS'89 suite of benchmark circuits are presented in Section 4. This paper concludes with some final remarks in Section 5.

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## 2. BACKGROUND

Background information is presented in this section by describing the timing properties of fully synchronous digital systems and the model used to represent these systems in Section 2.1 and 2.2, respectively.

### 2.1. Timing properties of a synchronous system

The properties of fully synchronous systems are well known and a detailed description can be found in [2, 3]. An example of a *local data path* [2, 3] (a *sequentially-adjacent pair of registers*) delimited by the registers $R_i$ and $R_f$ is shown in Figure 1. Such local data paths are characterized by a minimum and a maximum signal propagation delay from $Q_i$ to $D_f$. The clock signals $C_i$ and $C_f$ are delivered to $R_i$ and $R_f$ with delays $t_d^i$ and $t_d^f$, respectively, whereas the algebraic difference, $s_{i,j} = t_d^i - t_d^f$, is known as the *clock skew* [2–4]. Note that the clock skew $s_{i,j}$ as defined above may be negative, zero, or positive [2–4].

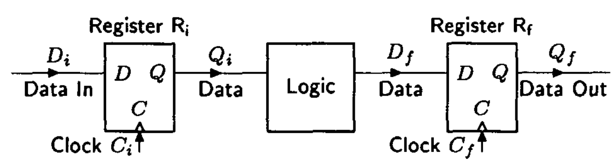


**Fig. 1.** A local data path

The exact temporal relationships among the $C$, $D$, and $Q$ signals in a local data path depend on many factors, including the particular types of registers employed (an in-depth treatment may be found in [2, 3, 5]). In the majority of cases, however, these timing relationships may be translated into an interval of values which the clock skew may assume [3,4]. A *permissible range* [1] is associated with each local data path—a clock skew schedule is *feasible* if each local clock skew is within the path specific permissible range. Note that under certain conditions [2], the permissible range of each local data path is guaranteed to include the zero clock skew value. Thus, most synchronous circuits are designed to satisfy global zero clock skew.

### 2.2. Circuit model

The work described in this paper is based upon a *connected undirected graph* [2] model of a synchronous circuit. A graph is constructed from a circuit in a natural way by adding a vertex for each register and a properly labeled edge for each local data path. Multiple edges between vertices are easily eliminated by using the graph transformations described in [2,3]. A simple example of the graph $\mathcal{G}$ of a circuit with $r = 5$ registers and $p = 6$ local data paths is shown in Figure 2—note the permissible range $[l, u]$ labeled on each edge. Each edge is also labeled with an arrow indicating the direction of signal propagation from the initial to the final register of the corresponding local data path [6].

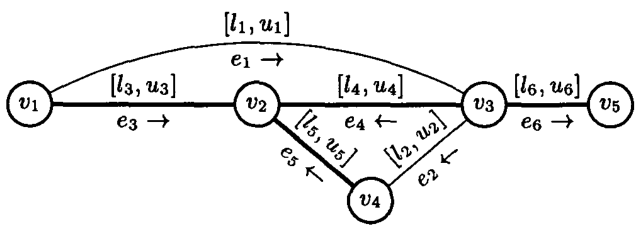


**Fig. 2.** A circuit graph—edges from the spanning tree are thicker.

## 3. THE CLOCK SKEW SCHEDULING PROBLEM

Two distinct approaches to the mathematical problem of clock skew scheduling are presented in this section. The clock period $T_{cp}$ of the circuit is *not* minimized in either approach. Rather, a feasible clock skew schedule is computed that maximizes the circuit timing reliability according to a previously specified reliability criteria. Linear and quadratic programming formulations are described in Sections 3.1 and 3.2, respectively.

### 3.1. Linear Programming Models

The LP formulation of the clock skew scheduling algorithm addresses the problem of determining a clock skew schedule that maximizes the circuits reliability for a specified target clock period $T_{cp}$. Recall that for each local data path $i$, the lower and upper bounds of the permissible range are $l_i$ and $u_i$, respectively, and the clock skew $s_{i,j}$ must satisfy [2] the inequality:

$$l_i \leq s_{i,j} \leq u_i. \tag{1}$$

Fishburn first demonstrated in [4] how to define an optimization problem to determine a clock skew schedule that improves the circuit timing reliability. In [4], a minimum safety factor $M$—the closest distance between a clock skew and the ends of the corresponding permissible range—is *maximized*. In other words, the minimum amount of *slack* (that is, the amount by which an inequality exceeds the limit), is maximized over all local data paths in a circuit. Formally, this problem is defined as Problem LP1:

Problem LP1

$$\begin{aligned} \max \quad & M \\ \text{subject to:} \quad & s_{i,j} \leq T_{CP} - \hat{D}^{i,j}_{PM} - M \\ & s_{i,j} \geq -\hat{D}^{i,j}_{Pm} + M \\ & M \geq 0. \end{aligned} \tag{2}$$

Note that in Eq. (2) above $\hat{D}^{i,j}_{Pm}$ and $\hat{D}^{i,j}_{PM}$ are the minimum and maximum signal propagation delays along the local data path from $R_i$ to $R_j$, respectively, while $-\hat{D}^{i,j}_{Pm} + M$ and $T_{CP} - \hat{D}^{i,j}_{PM} - M$ are the lower and upper bounds of the permissible range for the clock skew $s_{i,j}$ between $R_i$ and $R_j$.

An alternative linear programming formulation is proposed in this paper. In the following Problem LP2a, rather than maximizing the slack of the inequality (1) the objective is to minimize the maximum 'deviation' from the ideal clock skew over all local data paths:

Problem LP2a

$$\begin{aligned} \min \quad & M \\ \text{subject to:} \quad & s_{i,j} \leq T_{CP} - \hat{D}^{i,j}_{PM} \\ & s_{i,j} \geq -\hat{D}^{i,j}_{Pm} \\ & |s_{i,j} - g_{i,j}| \leq M, \end{aligned} \tag{3}$$

Note that $g_{ij}$ in Eq. (3) is the 'ideal' objective value of the clock skew for the local data path between $R_i$ and $R_j$. Also, note that $g_{ij}$ may have any desired value (within the permissible range) which satisfies certain design criteria. For the purpose of this work, however, the value of $g_{ij}$ is chosen to be the middle of the permissible range $(l + u)/2$. Furthermore, the absolute value function in Eq. (3) cannot be easily handled by the LP solver and is replaced with two inequalities as follows:

Problem LP2b

$$\begin{aligned} \min \quad & M \\ \text{subject to:} \quad & s_{i,j} \leq T_{CP} - \hat{D}_{PM}^{i,j} \\ & s_{i,j} \geq -\hat{D}_{Pm}^{i,j} \\ & s_{i,j} \leq g_{i,j} + M \\ & s_{i,j} \geq g_{i,j} - M \\ & M \geq 0 \end{aligned} \tag{4}$$

Finally, an alternative to problems LP1 and LP2b is introduced in this paper by redefining the safety factor $M$ as a relative rather than absolute value. Specifically, the value of $M$ is taken to represent a percentage of the permissible range of a local data path. Formally, the lower bound and upper bound clock skew constraints in Eq. (2) become

$$\begin{aligned} s_{i,j} &\geq -\hat{D}_{Pm}^{i,j}(1-M) + M(T_{CP} - \hat{D}_{PM}^{i,j}) \\ s_{i,j} &\leq (1-M)(T_{CP} - \hat{D}_{PM}^{i,j}) - M\hat{D}_{Pm}^{i,j}, \end{aligned} \tag{5}$$

and Problem LP2b becomes

Problem LP3

$$\begin{aligned} & \max \quad M \quad \text{subject to:} \\ & s_{i,j} \leq T_{CP} - \hat{D}_{PM}^{i,j} - M[T_{CP} - (\hat{D}_{PM}^{i,j} - \hat{D}_{Pm}^{i,j})] \\ & s_{i,j} \geq -\hat{D}_{Pm}^{i,j} + M[T_{CP} - (\hat{D}_{PM}^{i,j} - \hat{D}_{Pm}^{i,j})] \\ & 0 \leq M \leq 0.5. \end{aligned} \tag{6}$$

## 3.2. Quadratic Programming Models

The formulation of clock skew scheduling as a *quadratic programming (QP)* problem is described in this section. The linear dependencies among the clock skews and the kernel of cycles are introduced in Section 3.2.1. The QP problem is formulated and solved in Section 3.2.2.

### 3.2.1. Linear dependence of clock skews

A *kernel* of $\mathcal{G}$ is a minimal set of cycles such that (a) the cycles are linearly independent, and (b) every cycle in $\mathcal{G}$ is a linear combination of cycles from the set. The kernel can be summarized in a compact way by the *circuit kernel* equation, $\mathbf{B}\mathbf{s} = \mathbf{0}$, where $\mathbf{s}$ is an $n_c + n_m = p'$-element vector of all but the isolated skews, and, each row of the $n_c \times p'$ matrix $\mathbf{B}$ corresponds to a cycle. $\mathbf{B}$ can be derived from inspection by choosing a traversal direction of each cycle and including skews along the cycle with a sign depending upon the edge direction labeling (note the similarity with Kirchoff's Voltage Law loop equations for electrical networks [7]). Assume that the edges/skews are enumerated as in Figure 2 such that the chords $\mathbf{s}^c$ are first (indices 1 through $n_c$), followed by the main basis $\mathbf{s}^b$ (indices $n_c + 1$ through $p'$), and the isolated basis. If the cycles are permuted so as to appear in the order of the chords (*i.e.*, the first row of $\mathbf{B}$ corresponds to $e_1/s_1$, and so on), the kernel equation is $\mathbf{B}\mathbf{s} = [\mathbf{I}_{n_c} \;\; \mathbf{C}_{n_c \times n_m}] \left[\begin{smallmatrix}\mathbf{s}^c \\ \mathbf{s}^b\end{smallmatrix}\right] = \mathbf{s}^c + \mathbf{C}\mathbf{s}^b = \mathbf{0}$, where $\mathbf{I}_{n_c}$ is an identity matrix of dimension $n_c$. The solutions of this equation comprise the *kernel* or *null space* $\ker(\mathbf{B})$ of the linear mapping $\mathbf{B} : \mathbb{R}^{p'} \mapsto \mathbb{R}^{n_c}$ and $\mathbf{s}$ is called *consistent* if $\mathbf{s} \in \ker(\mathbf{B})$ [8].

### 3.2.2. QP clock skew scheduling problem formulation and solution

Let an *objective* clock schedule $\mathbf{g}$ be chosen according to certain design criteria ($\mathbf{g}$ has $p'$ elements). From a reliability perspective, for example, an ideal, although most likely *not* consistent, choice of $\mathbf{g}$ is $g_i = (l_i + u_i)/2$. The optimization goal is to determine a feasible and consistent schedule $\mathbf{s}$ such that the least square error $\varepsilon = (\mathbf{s} - \mathbf{g})^2$ is minimized:

Problem QP

$$\begin{aligned} \min \quad & \varepsilon = (\mathbf{s} - \mathbf{g})^2 = \sum_{k=1}^{p'} (s_k - g_k)^2 \\ \text{subject to} \quad & \mathbf{B}\mathbf{s} = \mathbf{0} \\ & \text{and } l_k \leq s_k \leq u_k \text{ for } k \in \{1 \ldots p'\}. \end{aligned} \tag{7}$$

This problem had previously been solved using an iterative two stage approach [6] that avoids much of the analytic and numeric difficulty associated with solving a constrained QP problem with bounded variables. The work described in this paper include a full implementation of the original algorithm in C++ code using LANCELOT to solve the final equations. New analytic results have been obtained and are presented in Section 4.

## 4. RESULTS

The algorithm described in Section 3.2.2 has been implemented as a C++ program and applied to both the ISCAS'89 benchmark circuits. We use our own LP and QP solvers (described in [2]) and the Lancelot package [9] for large scale optimization problems. The results of running the algorithms on the ISCAS '89 suite of benchmark circuits is summarized in Table 1.

## 5. CONCLUSIONS

The problem of clock skew scheduling for improved tolerance to process parameter variations is examined in this paper. The mathematical problem is formulated as both a

QP problem and as three LP problems. Two new LP formulations of the optimal scheduling problem from a reliability perspective are presented. The full source code (and executables) related to the work presented here is available at `http://www.sonic1.ee.pitt.edu:8080/GSRC`.

The new LP formulations are both shown to give improved results compared to the original LP problem (Eq. (2)) suggested in [4]. LP2b provides the best results (among the LP formulations) 55% of the time. LP3 gives the optimal solution 32% of the time, and LP1 gives the best results 13% of the time. The QP formulation provides the overall best result in 87% of the circuits. The availability of an efficient LP solver may make the LP problem formulations more desirable. In conclusion, the QP problem is the overall best approach while among the LP problems the new formulation presented in this paper (Problem LP2b) is superior.

## 6. REFERENCES


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**Table 1.** For each circuit the following data is listed: circuit name in column 1, number of disjoint subgraphs in column 2, and numbers of vertices, edges and target clock period in columns 3 through 5 respectively. The remaining columns list the average value of $\varepsilon$ in Eq. (7), that is, $\sqrt{\varepsilon/p}$.

| Circuit | subcircuits | $r$ | $p$ | $T_{CP}$ | $LP1$ | $LP2b$ | $LP3$ | $QP$ |
|---|---|---|---|---|---|---|---|---|
| **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** |
| s1196 | 7 | 18 | 20 | 20.8 | 3.71 | 3.44 | 3.69 | 3.29 |
| s1238 | 7 | 18 | 20 | 20.8 | 3.71 | 3.44 | 3.69 | 3.29 |
| s13207 | 49 | 669 | 3068 | 85.6 | 23.88 | 23.72 | 23.73 | 13.14 |
| s1423 | 2 | 74 | 1471 | 92.2 | 28.69 | 28.01 | 28.58 | 20.27 |
| s1488 | 1 | 6 | 15 | 32.2 | 7.85 | 4.81 | 6.17 | 5.10 |
| s1494 | 1 | 6 | 15 | 32.8 | 7.95 | 4.83 | 6.15 | 5.08 |
| s208.1 | 1 | 8 | 28 | 12.4 | 1.46 | 1.47 | 1.49 | 1.71 |
| s27 | 1 | 3 | 3 | 6.6 | 0.54 | 0.43 | 0.44 | 0.43 |
| s298 | 1 | 14 | 54 | 13 | 2.16 | 1.83 | 1.72 | 1.56 |
| s344 | 1 | 15 | 68 | 27 | 4.91 | 4.59 | 4.90 | 3.71 |
| s349 | 1 | 15 | 68 | 27 | 4.83 | 4.77 | 4.97 | 3.68 |
| s382 | 1 | 21 | 113 | 14.2 | 3.15 | 3.04 | 2.84 | 2.63 |
| s386 | 1 | 6 | 15 | 17.8 | 3.87 | 2.28 | 2.24 | 1.99 |
| s400 | 1 | 21 | 113 | 14.2 | 3.14 | 3.04 | 2.84 | 2.63 |
| s420.1 | 1 | 16 | 120 | 16.4 | 2.08 | 2.07 | 2.09 | 1.86 |
| s444 | 1 | 21 | 113 | 16.8 | 3.53 | 3.58 | 3.40 | 3.10 |
| s510 | 1 | 6 | 15 | 16.8 | 4.49 | 3.76 | 4.35 | 4.03 |
| s526 | 1 | 21 | 117 | 13 | 2.03 | 2.46 | 2.09 | 1.71 |
| s526n | 1 | 21 | 117 | 13 | 2.03 | 2.46 | 2.09 | 1.71 |
| s5378 | 1 | 179 | 1147 | 28.4 | 5.99 | 5.56 | 5.66 | 3.77 |
| s641 | 1 | 19 | 81 | 83.6 | 23.60 | 18.48 | 20.04 | 15.89 |
| s713 | 1 | 19 | 81 | 89.2 | 25.35 | 20.33 | 22.05 | 17.13 |
| s820 | 1 | 5 | 10 | 18.6 | 6.28 | 6.04 | 6.34 | 4.22 |
| s832 | 1 | 5 | 10 | 19 | 6.36 | 6.15 | 6.44 | 4.20 |
| s838.1 | 1 | 32 | 496 | 24.4 | 3.48 | 3.50 | 3.48 | 2.90 |
| s9234 | 3 | 228 | 2476 | 75.8 | 18.64 | 19.11 | 18.62 | 12.27 |
| s9234.1 | 2 | 211 | 2342 | 75.8 | 18.78 | 18.05 | 18.72 | 12.54 |
| s953 | 4 | 29 | 135 | 23.2 | 3.01 | 3.66 | 2.87 | 2.46 |
| s1269 | 1 | 37 | 251 | 51.2 | 12.15 | 13.10 | 11.70 | 9.54 |
| s1512 | 1 | 57 | 405 | 39.6 | 7.93 | 7.57 | 7.87 | 5.94 |
| s3271 | 1 | 116 | 789 | 40.4 | 6.53 | 4.65 | 4.45 | 3.69 |
| s3330 | 1 | 132 | 514 | 34.8 | 5.29 | 6.99 | 5.75 | 3.69 |
| s3384 | 25 | 183 | 1759 | 85.2 | 21.49 | 20.43 | 21.43 | 11.43 |
| s4863 | 1 | 104 | 620 | 81.2 | 22.39 | 22.78 | 22.37 | 15.25 |
| s6669 | 20 | 239 | 2138 | 128.6 | 34.14 | 30.26 | 31.73 | 17.92 |
| s938 | 1 | 32 | 496 | 24.4 | 3.48 | 3.49 | 3.49 | 2.89 |
| s967 | 4 | 29 | 135 | 20.6 | 2.99 | 3.34 | 2.91 | 2.21 |
| s991 | 1 | 19 | 51 | 96.4 | 18.00 | 15.08 | 16.89 | 9.95 |