Inductance/Area/Resistance Tradeoffs in High Performance Power Distribution Grids

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Abstract— **The design of high integrity, area efficient power distribution grids is of immediate practical importance as the portion of on-chip interconnect resources dedicated to power distribution networks in high performance integrated circuits has greatly increased. To optimize the process of allocating on-chip metal resources, inductance/area/-resistance tradeoffs in high speed power distribution grids are explored in this paper. Two tradeoff scenarios in power grids with alternating power and ground rails are considered. In the first scenario, the area occupied by the grid lines is maintained constant and the grid inductance versus grid resistance tradeoff is evaluated as the width of the grid lines varies. In the second scenario, the metal area of the grid is maintained constant and the grid inductance versus grid area tradeoff is investigated. In both cases, the grid inductance increases almost linearly with line width, rising more then eightfold for a tenfold increase in line width. The grid resistance and grid area, however, decrease relatively slowly with line width. This decrease in grid resistance and area is limited to a factor of two under assumed interconnect characteristics.**

I. Introduction

With each technology generation, the requirements placed on the on-chip power and ground distribution networks increase. The stricter specifications are due to shorter rise times, smaller noise margins, higher currents, and increased current densities. The higher speed switching of smaller transistors produces faster current transients in the power distribution network. The higher currents cause large ohmic IR voltage drops while fast current transients cause large inductive $L\frac{di}{dt}$ voltage drops (ΔI noise). The power distribution networks are typically designed to minimize these current transients, maintaining the local supply voltage within specified design margins.

To satisfy these tight specifications, the $R + j\omega L$ impedance of the on-chip power distribution networks should be sufficiently low as seen from the power terminals of the circuit elements. With transistor switching times as low as a few picoseconds, the on-chip signals typically contain significant harmonics at frequencies as high as ~ 100 GHz. For on-chip wires, the inductive reactance ωL dominates the overall wire impedance beyond ~ 10 GHz.

The process of designing the global on-chip power distribution network, however, is affected by the characteristic that these networks are typically designed at the early stages of the design process, when little is known about the power demands at specific locations on the integrated circuit (IC). Furthermore, redesigning the global power distribution at the later stages of the design process can be prohibitively expensive. Power distribution networks, therefore, tend to be conservatively designed [1], sometimes using more than a third of the on-chip metal resources [2].

Performance goals in power distribution networks, such as low impedance (low inductance and resistance), small area, and low current densities are typically in conflict. Increasing the line width to increase the conductance and improve the electromigration reliability also increases the grid area. Replacing wide metal lines with narrow interdigitated power/-ground (P/G) lines increases the line resistance if the grid area is maintained constant or increases the area if the net cross section of the lines is maintained constant. It is therefore important to make a balanced choice under these conditions. A quantitative model of the inductance/area/resistance tradeoff in high performance power distribution networks is therefore needed to achieve an efficient power distribution network. The primary goal of this research is to provide guidelines and intuition for the design of high performance power distribution networks.

This paper is organized as follows. Existing work on the design of power distribution networks in high complexity digital circuits is surveyed in Section II. A description of the power grid structures and a brief summary of the inductive properties of these networks are presented in Section III. Inductance/area/resistance tradeoffs in high performance power distribution grids are analyzed in Section IV. Specific conclusions characterizing the results described in this paper are summarized in Section V.

II. Background

The problem of optimizing on-chip multilevel power distribution grids has been considered by Song and Glasser [3]. In their early work published in 1986, a simple model is presented to estimate the maximum on-chip IR drop as a function of the number of metal layers and the metal layer thickness. The optimal thickness of each metal layer to produce minimum IR drops is determined. Design guidelines are provided to maximize signal wiring area while maintaining a constant IR drop. Application of these results to current high complexity integrated circuits is, however, limited.

An alternative approach for on-chip power distribution called a "cascaded power/ground ring" has been proposed by Cao and Krusius [4]. This approach focuses on maximizing the amount of wiring resources available for signal routing.

The inductance of on-chip power distribution networks has traditionally been neglected because the network inductance has been dominated by the parasitic inductance of the package pins, traces, and bond wires. This situation is changing rapidly due to increasing die size (and length of the on-chip power rails) and the lower inductance of flip chip packaging. Priore noted in [5] that replacing very wide power and ground lines with narrower interdigitated power and ground lines re-

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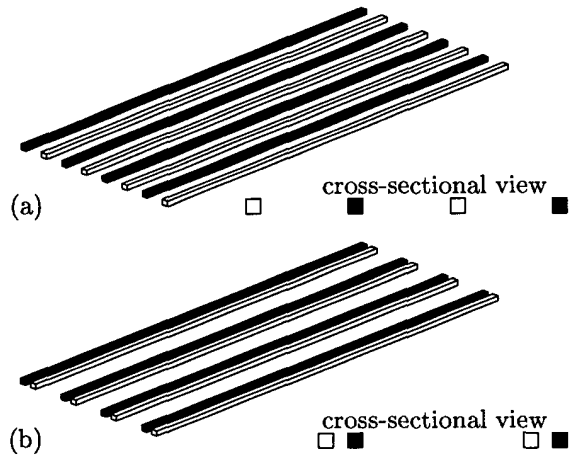

Fig. 1. General and cross-sectional view of the power/ground grid structures with alternating power and ground rails; (a) an interdigitated grid, where the lines are equidistantly spaced, (b) a paired grid, where the power and ground lines are placed in equidistantly spaced close pairs. The power lines are grey colored, the ground lines are white colored.

duces the self inductance of the supply network. He also suggested an approximate expression for the time constant of the response of a power supply network to a voltage step input signal. Zheng and Tenhunen [6] proposed replacing the wide power and ground lines with an array of interdigitated narrow power and ground lines with the purpose of reducing the switching voltage transients on the power bus by decreasing the characteristic impedance of the power network.

The inductance extraction program FastHenry [7] is used in this work to explore the inductive properties of these interconnect structures. A conductivity of 58 S/μm $\simeq$ (1.72 $\mu\Omega \cdot cm)^{-1}$ is assumed for the interconnect material.

III. Inductive properties of power distribution grids

Power grids with alternating power and ground lines are the focus of this analysis. Two types of such structures are illustrated in Fig. 1. In the grid type shown in Fig. 1a, the lines are equidistantly spaced; such grids are called *interdigitated*. In the second grid type, the lines are placed in equidistantly spaced pairs of adjacent power and ground lines, as shown in Fig. 1b. These grids are henceforth called *paired grids*.

As described in [8], the following inductive characteristics of high performance power grids have been established. Paired grids have lower inductance as compared to interdigitated grids with the same line width and number of lines. The grid inductance increases linearly with the grid length. The grid inductance decreases inversely linearly with the number of lines in a grid. The grid inductance is also relatively constant with frequency; a drop in inductance of less than 10% for most practical dimensions and structures occurs over a frequency range from 1 GHz to 100 GHz. These properties are due to the regularity of the grid structure. Alternating power and ground lines of the grid carry currents flowing in opposite directions. This arrangement cancels out the inductive coupling between distant lines, turning the inductive coupling into, effectively, a short range phenomenon.

These properties of the grid inductance greatly simplify the procedure for evaluating tradeoffs in power distribution grids. The resistance of the grid increases linearly with grid length and decreases inversely linearly with grid width (*i.e.*, the number of parallel lines). Therefore, the resistive properties of the grid can be conveniently described in a dimension independent grid sheet resistance $R_\square$. The linear dependence of the grid inductance on the grid dimensions is similar to that of the grid resistance. As with resistance, it is convenient to express the inductance of a power grid in a dimension independent *grid sheet inductance* $L_\square$ (*i.e.*, Henrys per square), rather than to characterize the grid inductance for a particular grid with specific dimentions. This approach is analogous to the *plane* sheet inductance of two parallel power and ground planes (*e.g.*, in a PCB stack), which depends only on the separation between the planes, not on the specific dimensions of the planes. Similarly, the grid sheet inductance reflects the routing characteristics of the grid (*i.e.*, the line width and pitch) and is independent of the dimensions of a specific structure (*i.e.*, the grid length and the number of lines in the grid).

To investigate inductance tradeoffs in power distribution grids, the dependence of the grid inductance on line width is evaluated using FastHenry. Paired and interdigitated grids consisting of ten P/G rails are investigated. A line length of 1000 μm and a line thickness of 1 μm are assumed. The minimum spacing between the lines S_0 is 0.5 μm. The line width W is varied from 0.5 μm to 5 μm.

IV. Inductance/Area/Resistance tradeoffs

Two tradeoff scenarios are considered in this paper. The inductance versus resistance tradeoff under a constant grid area constraint in high performance power distribution grids is analyzed in Section IV-A. The inductance versus area tradeoff under a constant grid resistance constraint is analyzed in Section IV-B.

A. Inductance vs. resistance tradeoff under a constant grid area constraint

In the first scenario, the fraction of the metal layer dedicated to the power grid, called the grid area ratio and denoted as A, is assumed fixed and the objective is to explore the tradeoff between the grid inductance and resistance under the constraint of a constant area. The area dedicated to the grid includes both the wire width W and the minimum spacing S_0 necessary to isolate the power line from any neighboring lines.

The inductance of paired grids is virtually independent of the separation between the P/G line pairs because the current loop area is mainly determined by the line spacing within each P/G pair where this spacing is much smaller than the separation between P/G pairs [8]. Therefore, only paired grids with an area ratio of 0.2 are considered here; the properties of paired grids with a different area ratio A (*i.e.*, different P/G separation) can be linearly extrapolated. In contrast, the dependence of the inductance of the interdigitated grids on the grid line pitch is substantial, since the effective current loop area is strongly dependent upon the line pitch. Interdigitated grids with area ratios of 0.2 and 0.33 are analyzed here. With increasing line width, the grid line pitch P (and, consequently, the grid width) increases accordingly so as to maintain the desired grid area ratio $A = \frac{W+S_0}{P}$.

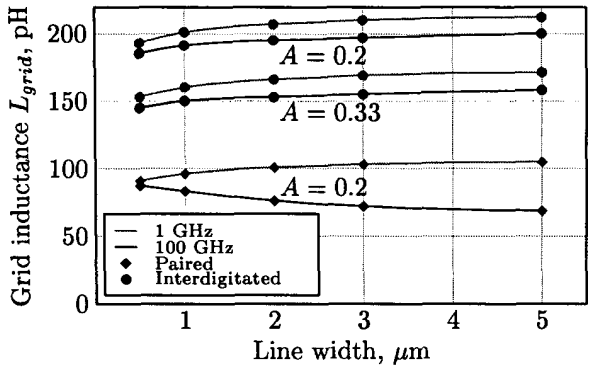

Fig. 2. The grid inductance versus line width under a constant grid area constraint for paired and interdigitated grids with ten P/G lines.

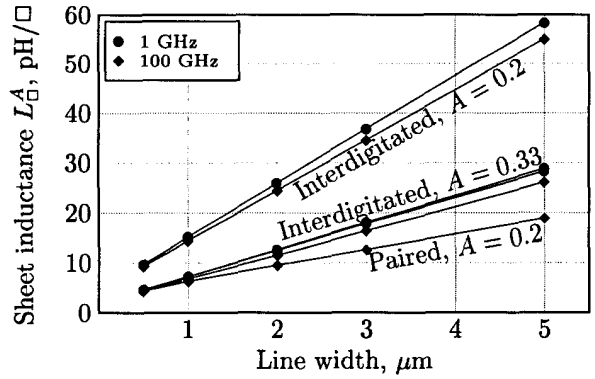

Fig. 3. The sheet inductance L_{grid}^{A} versus line width under a constant grid area constraint.

The grid inductance L_{grid} versus line width is shown in Fig. 2 for two signal frequencies: 1 GHz (the low frequency case) and 100 GHz (the high frequency case). The high frequency inductance is within 10% of the low frequency inductance for interdigitated grids, as mentioned previously. The large change in inductance for paired grids is due to the proximity effect in closely spaced, relatively wide lines.

The sheet inductance of a grid with a fixed area ratio A, $L_{\square}^{A}$, can be determined from L_{grid} through the following relationship,

$$L_{\square}^{A}(W) = L_{grid}\frac{NP}{D} = L_{grid}\frac{N}{D}\frac{W+S_0}{A}, \qquad (1)$$

where N is the number of lines (line pairs) and P is the line (line pair) pitch in an interdigitated (paired) grid (see Fig. 1). The grid length is denoted D. For each of the six L_{grid} data sets shown in Fig. 2 a correspondent $L_{\square}^{A}$ versus line width data set is plotted in Fig. 3. As illustrated in Fig. 3, the sheet inductance $L_{\square}^{A}$ increases with line width; this increase with line width can be approximated as a linear dependence with high accuracy.

The low frequency sheet resistance of a grid is $R_{\square} = \rho_{\square}\frac{P}{W}$. The grid resistance under a constant area ratio constraint, $A = \frac{W+S_0}{P} = \text{const}$, can be expressed as a function of only the line width W,

$$R_{\square}^{A} = \frac{\rho_{\square}}{A}\frac{W+S_0}{W}. \qquad (2)$$

This expression shows that as the line width W increases from the minimum line width $W_{min} = S_0$ ($\frac{W+S_0}{W} = 2$) to a large width ($W \gg S_0$, $\frac{W+S_0}{W} \simeq 1$), the resistance decreases twofold. An intuitive explanation of this result is that at the minimum line width $W_{min} = S_0$, only half of the grid area used for power routing is filled with metal (the other half is used for line spacing) while for large widths $W \gg S_0$, almost all of the grid area is metal.

In order to better observe the relative dependence of the grid sheet inductance and resistance on the line width, $L_{\square}^{A}$ and $R_{\square}^{A}$ are plotted in Fig. 4 normalized to their respective values at a minimum wire width of 0.5 μm (such that $L_{\square}^{A}$ and $R_{\square}^{A}$ are equal to one normalized unit at 0.5 μm). As shown in Fig. 4, five out of six $L_{\square}^{A}$ lines have a similar slope. These lines depict the inductance of a paired grid at 1 GHz and the inductance of two interdigitated grids ($A = 0.2$ and $A = 0.33$) at 1 GHz and 100 GHz. The line with a lower slope represents a paired grid at 100 GHz. This different behavior is due to pronounced proximity effects in closely placed wide lines with very high frequency signals.

The dependence of the grid sheet inductance on line width is virtually linear and can be accurately approximated by

$$L_{\square}^{A}(W) = L_{\square}^{A}(W_{min}) \cdot \{1 + K \cdot (W - W_{min})\}, \qquad (3)$$

where $L_{\square}^{A}(W_{min})$ is the sheet inductance of the grid with minimum line width and K is the slope of the lines shown in Fig. 4. Note that while $L_{\square}^{A}(W_{min})$ depends on the grid type and area ratio (as illustrated in Fig. 3), the coefficient K is virtually independent of these parameters (with the exception of the special case of paired grids at 100 GHz).

The grid inductance increases with line width, as shown in Fig. 4. The inductance increases eightfold (sixfold for the special case of a paired grid at 100 GHz) for a tenfold increase in line width. The grid resistance decreases nonlinearly with line width. This decrease in resistance is limited to a factor of two as mentioned previously.

As the line width decreases, the inductive $L\frac{dI}{dt}$ noise becomes smaller due to the lower grid inductance L while the resistive IR noise increases due to the greater grid resistance R, as shown in Fig. 4. Therefore, a minimum total power supply noise, $IR + L\frac{dI}{dt}$, exists at some target line width. The line width that produces the minimum noise depends upon the ratio and relative timing of the peak current demand I and the peak transient current demand $\frac{dI}{dt}$. The optimal line width is, therefore, application dependent. This tradeoff provides guidelines for choosing the width of the power grid lines that produces the minimum noise.

B. Inductance vs. area tradeoff under a constant grid resistance constraint

In the second scenario, the resistance of the power distribution grid is fixed (for example, by IR drop or electromigration constraints). The grid sheet resistance is

$$R_{\square} = \rho_{\square}\frac{P}{W} = \frac{\rho_{\square}}{M} = \text{const}, \qquad (4)$$

where $\rho_{\square}$ is the sheet resistivity of the metal layer and $M = \frac{W}{P}$ is the fraction of the area filled with power grid metal, hence-

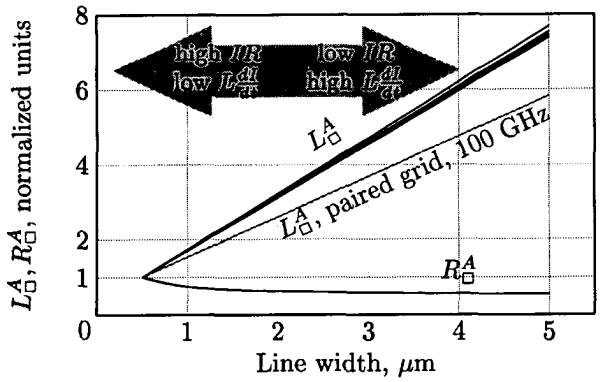

Fig. 4. Normalized sheet inductance and sheet resistance versus the width of the P/G line under a constant grid area constraint.

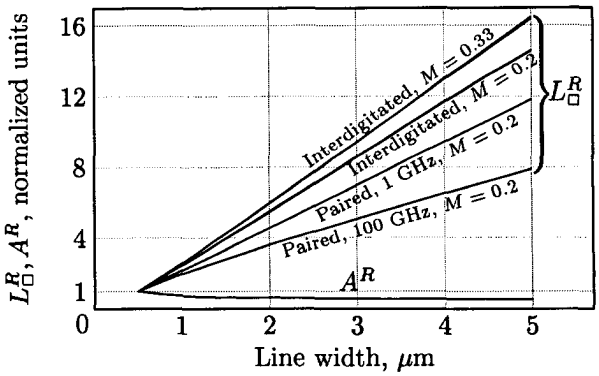

Fig. 5. Normalized sheet inductance $L^R_\square$ and the grid area ratio A^R versus the width of the P/G line under a constant grid resistance (*i.e.*, constant grid metal ratio M) constraint.

forth called the metal ratio of the grid. The constant resistance $R_\square$ infers a constant grid metal ratio M. The constraint of a constant grid resistance is similar to that of a constant grid area except that the line spacings are not considered to be a part of the grid area. The objective is to explore tradeoffs between the grid inductance and area under the constraint of a constant grid resistance. This analysis is conducted similarly to the analysis described in the previous section. Therefore, only the normalized data, analogous to the data shown in Fig. 4, is depicted in Fig. 5.

As shown in Fig. 5, under a constant resistance constraint the grid inductance increases linearly with line width. Unlike in the first scenario, the slope of the inductance increase with line width varies with grid type and grid metal ratio. Paired grids have the lowest slope and interdigitated grids with a metal ratio of 0.33 have the highest slope. The lower slope of the inductance increase with line width is preferable, as, under a target resistance constraint, a smaller area and/or inductance implementation can be realized. The slope of the inductance increase with line width is independent of frequency in interdigitated grids (the lines for 1 GHz and 100 GHz coincide and are not discernible in the figure), while in paired grids the slope decreases significantly at high frequencies (100 GHz). The inductance increase varies from eight to sixteen fold, depending on grid type and grid resistance (*i.e.*, grid metal ratio), for a tenfold increase in the wire width. A reduction in the grid area is limited by a factor of two, similar to the decrease in resistance in the first scenario.

V. Conclusions

The inductance/area/resistance tradeoff in high performance power distribution grids is explored in this paper. Two types of grids with alternating power and ground rails are investigated for two different tradeoff scenarios. In the first scenario, the inductance versus resistance tradeoff is investigated as the width of the grid lines is varied under a constant grid area constraint (including the necessary minimum spacing). In the second scenario, the inductance versus grid area tradeoff is investigated as the width of the grid lines is varied under a constant grid resistance constraint (*i.e.*, constant metal area of the grid). The line width increases tenfold starting from a minimum width equal to the minimum line spacing. In both scenarios, the grid inductance increases linearly with line width, rising from eight to sixteen times for a tenfold increase in the line width. The grid resistance in the first scenario and the grid area in the second scenario decrease relatively slowly with line width. The decrease in the grid resistance and grid area is limited to a factor of two in these two tradeoff scenarios.

This investigation provides guidelines for evaluating the interdependence of the inductance, area, and resistance in high performance power grids. The inductance versus resistance tradeoff provides a basis for choosing the width of the power line that minimizes the noise based on application-specific current requirements. These guidelines and criteria can be used to explore the design of high performance power distribution grids based upon application-specific slew rate, current, and power supply noise requirements.

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