CMOS VOLTAGE INTERFACE CIRCUIT FOR LOW POWER SYSTEMS

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ABSTRACT

A bi-directional CMOS voltage interface circuit is proposed for applications that require signal transfer between two circuits operating at different voltage levels. The circuit can also be used as a level converter at the driver and receiver ends of long interconnect lines for low swing applications. The operation of the voltage interface circuit is verified by both simulation and experimental test circuits. The proposed voltage interface circuit operates at high speed while offering significant power savings of up to 95% as compared to existing schemes.

1. INTRODUCTION

The dominant component of power consumption in CMOS circuits is dynamic power [1]. The most effective way of reducing dynamic power consumption is to reduce the supply voltage. Since lowering the supply voltage also degrades the speed of a circuit, different blocks are often operated at different voltages in high complexity integrated circuits [2], [3], [4], [7], [8]. Blocks that must operate at high speed utilize a higher voltage while those blocks for which speed is less critical operate at a lower voltage. In order to transfer signals among these regions operating at different voltage levels, specialized voltage interface circuits are required.

Another issue in modern integrated systems is the significant amount of on-chip interconnect [4]-[6]. At each new IC generation, the relative amount of interconnect increases due to the greater number of transistors and the larger die size. In many recent systems, charging and discharging these interconnect lines can require more than 50% of the total power consumed on-chip [5], [6]. In certain programmable logic devices, more than 90% of the total power consumption is due to the interconnect wires [5].

As described in [4]-[6], decreasing the signal voltage swing on the interconnect can significantly decrease the power consumption. A low swing interconnect architecture [6] is shown in Fig. 1. In this scheme, the circuit blocks operate at a high voltage for high throughput, while a low voltage swing signal is transmitted on the interconnect to decrease the power consumption. Voltage level converters are placed at the driver and receiver ends of this low swing interconnect architecture to change the voltage swing.

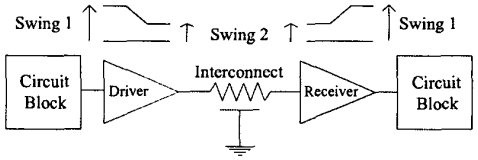

Fig. 1. Circuit architecture for low swing interconnect.

A level converter circuit must consume very low power in order to fully exploit the reduced power attained by lowering the voltage. In order not to degrade the circuit operating speed, the voltage interface circuit must convert the input signal swing to the desired output signal swing with minimum delay [2], [4]. A simple CMOS interface circuit composed of two cascaded inverters is a standard circuit approach for converting voltage levels [2]-[7]. This circuit suffers from static power consumption and a non-full rail output voltage swing when converting a low voltage swing input to a high voltage swing output (such as the receiver end shown in Fig. 1) [2], [3], [6], [7]. Specialized circuits are therefore required to efficiently convert voltage levels.

A bi-directional CMOS voltage interface circuit that drives high capacitive loads to full swing at high speed while consuming no static power is presented in this pa-

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per. The propagation delay, power consumption, and power efficiency characteristics of the proposed voltage interface circuit are compared to other interface circuits described in the literature [2], [3], [5], [6]. The proposed voltage interface circuit offers significant power savings and lower propagation delay as compared to these circuits.

The paper is organized as follows. Operation of the proposed interface circuit is described in Section 2, simulation results and a comparison with other converter circuits are presented in Section 3, and results from experimental test circuits are presented in Section 4. Finally, some conclusions are provided in Section 5.

2. CIRCUIT OPERATION

The interface circuit proposed here is shown in Fig. 2. The circuit provides bi-directional voltage level conversion. Therefore, without any change in circuit configuration, the interface circuit can be used at both the driver and receiver ends of a low voltage swing circuit architecture (see Fig. 1) to convert voltage levels from high to low and low to high.

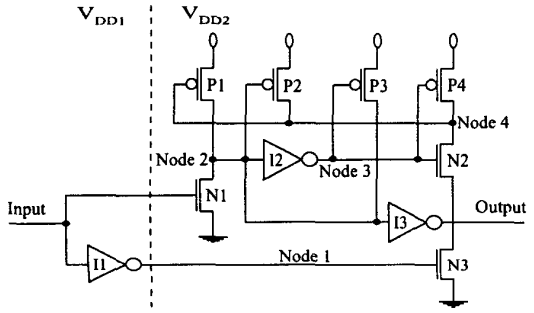

Fig. 2. The proposed voltage interface circuit.

In the proposed interface circuit, P1 is isolated from the input to minimize both the static power consumption and the propagation delay. As the pull-up and pull-down networks are never simultaneously on, the proposed voltage interface circuit consumes no static power while driving high capacitive loads to full swing (V_{DD2}) at high speed.

In this circuit, only I1 is supplied by V_{DD1}. The rest of the circuit (to the right of the demarcation line) is supplied by V_{DD2}. The circuit operates in the following manner. With a $0 \rightarrow 1$ transition at the input, node 2 is discharged through N1. P2 ensures that P1 is cut-off, and I2 ensures that P3 is cut-off during the output transition, so that the short-circuit power consumption and output transition time are minimized. When node 2 becomes sufficiently low, the output transitions high. With a $1 \rightarrow 0$ transition at the input, node 1 goes high. Node 4 is pulled down to ground through N2 and N3 (N2 is on before the input signal changes). As node 4 is discharged to ground, P1 turns on, charging node 2. When node 2 is sufficiently high, the output signal transitions low. There is a negative feedback path from node 3 to node 4 to node 2 through I2, P4, and P1. P3 preserves the output state after P1 is cut-off through the feedback path.

3. CIRCUIT SIMULATION RESULTS

The voltage interface circuit proposed here is compared to selected voltage interface circuits published in the literature [2], [3], [5], [6]. These circuits are referred to by acronyms derived from the first letters of the last names of the authors who proposed the circuits. The circuit proposed in [2] (SF), the circuit proposed in [3] (CQ), and the circuit proposed here (KSF) are non-inverting while the asymmetric level converter circuit introduced in [5] (ZGR), and the symmetric level converter circuit introduced in [6] (NIITA) are inverting. To produce a fair comparison, an inverter is added to the output stages of ZGR and NIITA. The output stage inverter of each voltage interface circuit is sized the same.

Simulations are performed for a 0.18 μm CMOS technology. The two voltage levels are 1.8 volts and 3.3 volts. The simulations have only been carried out for level conversion from low to high since CQ, ZGR, and NIITA have been designed specifically for low swing-to-high swing conversion. The input signal applied to each interface circuit is a 1 MHz square wave signal with a 1.8 volt swing and a 50% duty cycle. The input to output propagation delay is calculated from 50% of the input swing to 50% of the output swing. The average delay is the arithmetic mean of the high-to-low and low-to-high propagation delays. The average power consumption is calculated for a full cycle of the input waveform.

Each circuit is optimized to drive a 15 pF load. The load at the output of each interface circuit is swept from 1 pF to 15 pF in order to evaluate the delay and power characteristics. The propagation delay versus load capacitance characteristics for each of the circuits are shown in Fig. 3. The average power consumption versus load capacitance are shown in Fig. 4.

The voltage interface circuit proposed here exhibits the minimum conversion delay among the target interface circuits. As shown in Fig. 3, KSF is 3.6 times faster than CQ, 1.9 times faster than SF, 1.2 times faster than ZGR, and 1.9 times faster than NIITA for a 1 pF load capacitance. The propagation delay of ZGR approaches the propagation delay of KSF with increasing load capacitance. However, ZGR displays poor power characteristics as compared to KSF.

The high speed operation of KSF produces no power penalty. Rather, as shown in Fig. 4, the proposed voltage interface circuit offers a significant power savings. KSF reduces the average power consumption by up to 57% as compared to CQ, by up to 24% as compared to SF, by up

to 95% as compared to ZGR, and by up to 12% as compared to NIITA.

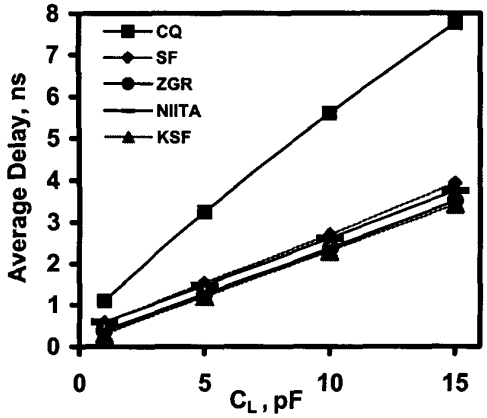

Fig. 3. Average delay versus load capacitance.

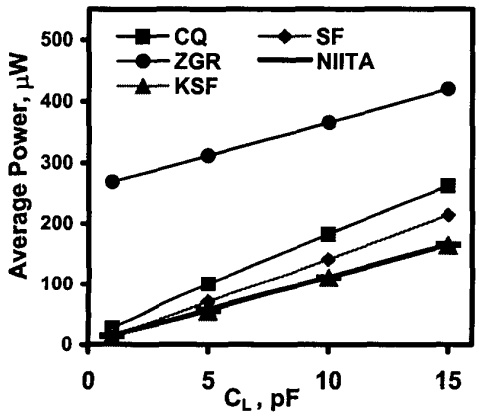

Fig. 4. Average power versus load capacitance.

To better understand the power characteristics of these voltage interface circuits, the power efficiency (defined as the ratio of the power delivered to the load to the total power consumed by the circuit) characteristics are shown in Fig. 5. The normalized area, maximum frequency of full swing operation (MFSO), and internal power consumption (excluding the power delivered to the load, C_L = 1 pF) of each target circuit are listed in Table 1. The circuit area is evaluated assuming the area is proportional to the total transistor width. The area of each circuit is normalized with respect to the smallest circuit (NIITA). MFSO is defined as the maximum input signal frequency at which a full swing signal is observable at the output for a 1 pF load capacitance.

As shown in Fig. 5, the internal losses of the KSF circuit are quite small. The power efficiency of KSF ranges from 89.3% to 99.4% as the load is increased from 1 pF to 15 pF. The power efficiency of KSF is 10.3% higher than the power efficiency of NIITA for a 1 pF load. As the load capacitance is increased, the power efficiency of KSF and NIITA both improve and approach each other (~1% difference) since the internal losses of both circuits become negligible as compared to the power delivered to the load. However, the internal power loss of KSF is significantly lower than the internal power loss of NIITA over the entire range of load capacitances (55% lower for C_L = 1 pF and 47% lower for C_L = 15 pF).

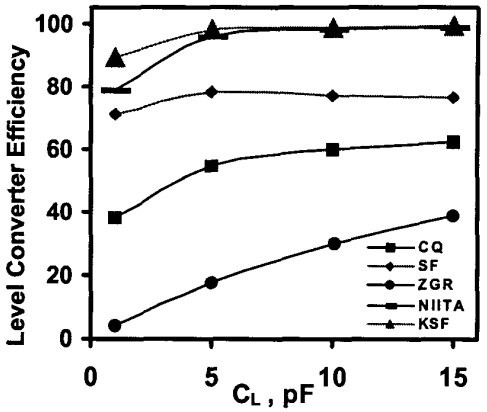

Fig. 5. Power efficiency versus load capacitance.

The power consumed by each circuit increases linearly with the load capacitance (see Fig. 4). The internal losses of CQ and SF are primarily due to the short-circuit current at the output stage during the output signal transition. As the load capacitance increases, the output transition requires additional time, increasing the short-circuit current. Therefore, the slopes of the CQ and SF power curves are higher as compared to the other circuits. The worsening short-circuit power loss of SF degrades the efficiency as the load increases above 5 pF (see Fig. 5). ZGR suffers from significant static power loss when the input signal is high, therefore ZGR has the lowest power efficiency (the highest internal power loss).

Table 1. The normalized area, MFSO, and average internal power consumption of each voltage interface circuit (C_L = 1 pF).

Circuit	Area (normalized)	MFSO (MHz)	Power (µW)
SF [2]	2.8	240	4.5
CQ [3]	2.1	200	17.8
ZGR [5]	1.6	590	257.1
NIITA [6]	1.0	380	2.9
KSF	1.3	610	1.3

As listed in Table 1, the proposed voltage interface circuit KSF occupies a small amount of area (second smallest) and offers the highest operating frequency range. KSF is operational up to an input frequency of 610 MHz (when driving a 1 pF output load). The MFSO is not

directly related to the average delay shown in Fig. 3 since the MFSO is determined by the longest input to output full rail delay (rising or falling) of each circuit.

4. EXPERIMENTAL RESULTS

The interface circuit has been fabricated in a 3 μm CMOS technology. A microphotograph of the circuit is shown in Fig. 6.

Fig. 6. Microphotograph of the interface circuit.

The circuit has been experimentally evaluated with 5 volt and 10 volt power supplies. To verify the bi-directional operation of the circuit, the circuit has been evaluated for both low-to-high and high-to-low voltage interfaces. The experimental results are listed in Table 2. The waveforms obtained from the circuit tests are shown in Fig. 7 (the time axis is 500 ns/division, and the voltage axis is 5 volts/division).

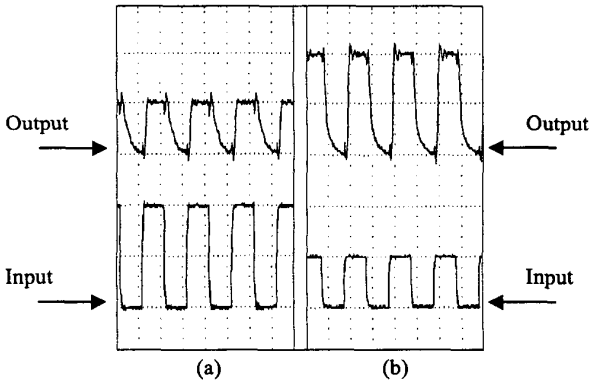

Fig. 7. Experimentally derived input and output voltage waveforms of the proposed voltage interface circuit. (a) 10 V → 5 V interface. (b) 5 V → 10 V interface.

The functional operation of the proposed interface circuit has also been experimentally verified. The propagation delays listed in Table 2 are higher than the simulation results (see Fig. 3) due to the voltage level (1.8/3.3 volts vs. 5/10 volts) and feature size (3 μm vs. 0.18 μm) differences.

As listed in Table 2, the high-to-low propagation delay is longer than the low-to-high propagation delay for both the 5 V → 10 V and 10 V → 5 V interfaces. The critical node that determines the output transition time is node 2. After a 0 → 1 transition at the input, the time to discharge node 2 only depends upon the response time of N1. Alternatively, after a 1 → 0 transition at the input, the time to charge node 2 depends upon the delay along the path I1, N3, N2, and P1.

Table 2. Experimentally measured test results.

Voltage Levels	Output 1 → 0 (ns)	Output 0 → 1 (ns)
10 V → 5 V	190	80
5 V → 10 V	120	70

5. CONCLUSIONS

A bi-directional CMOS voltage interface circuit for signal transfer between circuits operating at different voltage levels is presented in this paper. The circuit can also be used at the driving and receiving ends of long interconnect lines so as to lower the power consumption by propagating a smaller voltage swing signal along the line. Up to a 3.6 times delay improvement and up to a 95% power reduction are observed as compared to previously published schemes. The proposed voltage interface circuit operates at high speed while consuming no static power.

6. REFERENCES

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