An Substrate Noise Circuit for Accurately Testing Mixed-Signal ICs

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Abstract — A substrate coupling noise measurement technique is presented in this paper. The proposed on-chip test circuit can accurately and efficiently measure substrate coupling noise in any type of semiconductor substrate. The measured substrate coupling voltage is converted to a digital code by a simple on-chip analog-to-digital converter. The I/O pads, bounding wires, package frame, external cables, and test fixture/circuit do not affect the accuracy of the measurement. On-chip calibration is also included to further extend the test accuracy. The circuit provides an effective substrate coupling noise test technique for evaluating a variety of existing substrate coupling noise models. Less than 0.4% error as compared to SPICE is achieved.

I. Introduction

The push for reduced cost, more compact circuit boards, and added customer features has provided incentives for including analog functions with primarily digital MOS integrated circuits (IC). Complex high speed digital circuits together with high performance analog circuits are therefore commonly integrated on the same IC substrate. In such mixed-signal systems, fast switching transients produced by the digital circuits can couple into sensitive analog components, thereby limiting analog precision. Performance degradation caused by substrate noise has become difficult to control and even more difficult to predict. The capability of accurately measuring substrate noise to identify and avoid these problems has therefore become increasingly important.

Substrate noise was first reported in the 80's [1], followed by significant research in the 1990's [2]-[4]. In order to evaluate substrate noise, on-chip test circuits are required to accurately and efficiently measure the substrate current [4], [5]-[9]. These measurements, however, are based on simple single MOS transistor test structures [2], [8], voltage comparator structures [6], [7], or single stage MOS different amplifier structures [9]. A common problem in these measurements is the difficulty of acquiring output signals without other noise signals mixed in the measured signal. Due to the small peak-to-peak voltage, an accurate substrate noise test is difficult to achieve. Noise from the test board, power supply, and integrated circuit package adds noise to the substrate coupling current sensed by the on-chip test circuitry (see Fig. 1). The parasitic components of the pads, bonding wires, package frame, external circuitry, and the cable affect the analog output signal, severely decreasing the accuracy of the measurement. Expensive equipment is also typically required to test these circuits. In order to produce accurate test results and to simplify the measurement process, dedicated data sensing and analog-to-digital conversion circuitry must also be included on-chip.

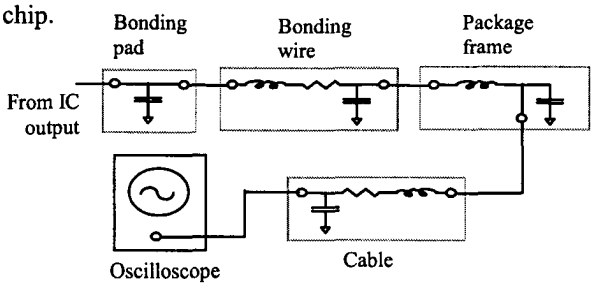

Fig. 1: Parasitic impedances along an IC test path

In this paper, an accurate substrate noise test circuit is presented. The proposed test circuit rejects other types of noise such as common-mode noise, power/ground noise, *1/f* noise, and any random noise while only collecting the substrate coupling noise. The circuit output is in the form of a digital code so that the noise from the pads, bonding wires, package frame, and external test circuit does not affect the accuracy of the test result. Simple test equipment is required for reading out the measured data.

This paper is organized as follow. The substrate noise mechanism is reviewed in Section II. In Section III, the principle used in the on-chip substrate noise test circuitry is described. Design details of the circuit are presented in Section IV. The error of the test circuit is considered in Section V. Analytic and SPICE simulation results are presented and compared in Section VI. Finally, some conclusions are provided in Section VII.

II. Substrate Coupling Noise

When current is injected into the substrate, a local fluctuation in the substrate voltage will occur. This voltage fluctuation is the substrate noise. In mixed-signal integrated circuits, the injected current can be caused by power busses coupling noise into the substrate through ohmic contacts [5], [10], the wells capacitively coupling noise through the reverse biased bulk/well junctions, and/or the transistors capacitively coupling noise through

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the source/drain diffusions. When the drain of an MOS transistor switches, the switching voltage is coupled through the drain junction capacitor into the substrate (see Fig. 2). Due to the change in the substrate voltage, a substrate pulse current flows into the substrate. The induced switching current flow causes the substrate potential to change. Due to the body effect and the junction capacitance of a sensitive transistor, changes in the backgate voltage induce noise spikes in the drain current and, consequently, the drain voltage. The substrate noise coupling produces different effects for different types of substrates. For low resistance, heavily doped, and thick substrates, the injected noise current flows directly through the epitaxial layer into the bulk and up through the epi layer to the substrate contact on the surface [5]. The voltage induced by the current flow within the substrate is small, decreasing the substrate coupling. These substrate coupling noise sources are shown in Fig. 2 below.

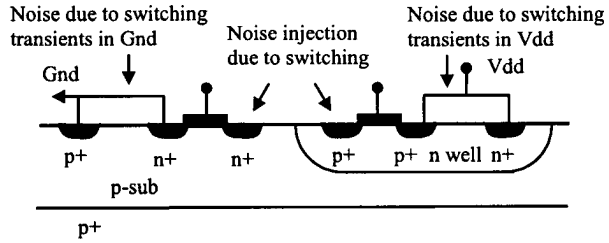

Fig. 2: Sources of noise coupling within the substrate

Masui reported in [2] that the noise voltage decreases with increasing spacing in lightly doped substrates; however, in heavily doped substrates, the substrate coupling noise depends little on the spacing. The experimental results described in [9] also show that the peak-to-peak noise amplitude is independent of the distance between the current source and the noise source; increasing the separation from 40 μm to 850 μm does not reduce the measured noise. Additionally, physical separation has no observable effect on the noise settling time.

The current flow in the substrate also affects the MOS transistors by changing the effective threshold voltage. Substrate noise reduction techniques include separate analog and digital power/ground lines, physical separation between the analog and digital circuits, guard rings, a low inductance bias path for the substrate, and the application of additional substrate contacts as reported in [5].

III. Circuit Design Principles

The proposed substrate noise test circuit has a differential structure and consists of a substrate coupling noise sensing circuit, an integrator, a comparator, a counter, and a digital timing circuit (see Fig. 3). The differential operation removes the common-mode noise from the power distribution network, thereby producing a more accurate capacitive coupling voltage. The substrate noise sensing part of the test circuit is shown in Fig. 4.

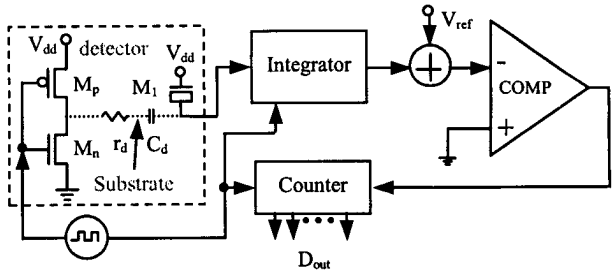

Fig. 3: Substrate coupling noise test circuit

Circuit operation

The circuit is composed of a differential integrator, a comparator, a digital control block, and some switches and capacitors (see Fig. 3). The gate of M_1 is connected to the power supply V_{dd}; the source and drain are tied together. The depletion capacitor C_d of the PN junction between the S/D and the substrate is formed as shown in Fig. 4.

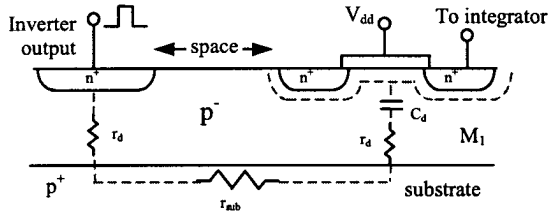

Fig. 4: The sensing part of the substrate noise test circuit

When a clock is applied to the input of the inverter, the output switches from V_{dd} to ground. Current is injected into the substrate through the drain capacitance. In order to increase the injection current, a large drain area for both the PMOS and NMOS transistors is selected for the inverter. This injected current causes a voltage change along the path which is sensed by a MOS transistor capacitor (M_1 in Fig. 4).

The substrate coupling noise is stored in the form of charge on the MOS sensing capacitor C_d. An integrator processes the sensed substrate coupling noise voltage for N clock cycles once the next stage comparator changes state. The comparator compares the integrated substrate coupling voltage with a reference voltage V_{ref} every clock cycle.

After N clock cycles, the output of the integrator is equal to the reference voltage, and the output state of the comparator changes. The updated comparator output terminates the counter that sums the number of digital cycles that have been applied to the noise source (the inverter) before the counter is terminated. The output of the counter is stored in an output buffer-register and passed from the test circuit. The sensing MOS capacitor C_d is small and is quickly charged/discharged. The substrate coupling noise over a wide range of frequency can therefore be measured with this sensing circuit. The substrate coupling noise per switching event is

$$V_{sub} = \frac{C_f}{NC_d} V_{ref} \quad , \qquad (1)$$

where C_f is the feedback capacitance in the integrator (see Fig. 5), C_d is the sensing capacitance of transistor M_1, N is a number converted from the output digital code, and V_{ref} is the reference voltage.

The change in the MOS capacitance C_d with the substrate voltage is small. In (1), C_f and C_d are design variables which are fixed by the circuit. N is the decimal value of the output digital code. The measured result is not affected by the parasitic impedances along the substrate coupling path and the external test path. Note in (1) that a precise reference voltage V_{ref} is required to achieve an accurate measurement. The substrate coupling voltage can be measured independent of the type of substrate. This substrate coupling noise test technique is therefore an effective tool for evaluating different substrate coupling noise models.

IV. Detailed Circuit Characteristics

A schematic of the substrate coupling noise integrator circuit is shown in Fig. 5. It is a fully symmetric differential switched capacitor circuit. An on-chip calibration process is used in this test circuit to remove the integrator offset and other noise voltages.

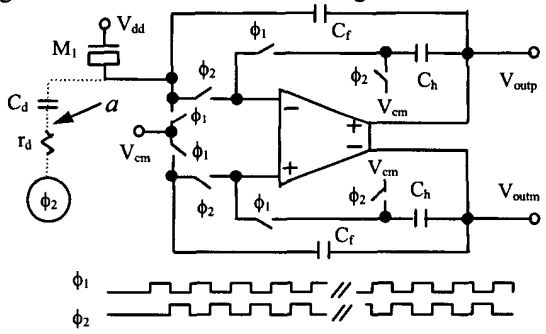

Fig. 5: Substrate coupling voltage integrator circuit

After N clock cycles, the differential voltage at the integrator output is

$$\Delta V_o[N] = \frac{C_d}{C_f} \sum_{k=1}^{N} V_{in}[k] + 2N\Delta - \frac{NC_d}{2C_f}\Delta + \delta[N], \qquad (2)$$

where $V_{in}[k]$ is the k_{th} sample voltage at node a during ϕ_1 and Δ is the integrator offset voltage. $\delta[N]$ is the lumped noise voltage at the output of the integrator. The first term in (2) is the total substrate noise components after N clock injections. The remaining terms are noise components unrelated to substrate coupling.

Calibration process

The coupling capacitor C_d is typically much smaller than the integrator feedback capacitor C_f. The third term in (2) is small, thereby making the second term dominant. For the circuit shown in Fig. 5, the amplifier offset voltage error and other noise sources can be removed by a calibration cycle. The operation of the calibration process proceeds as follow: by applying a power supply voltage at the inverter input during the calibration period and operating the circuit shown in Fig. 5, another digital code N_c is generated by the circuit. The new digital code is the error (including the amplifier offset voltage error) code. From (2), the total noise voltage is

$$\Delta V_n[N] = 2N\Delta - \frac{NC_d}{2C_f}\Delta + \delta[N] = \frac{N}{N_c} V_{ref} . \qquad (3)$$

The calibrated substrate coupling noise per switching event is

$$\Delta V_{noise} = \left(\frac{1}{N} + \frac{1}{N_c}\right) \cdot V_{ref} \quad , \qquad (4)$$

and the corrected digital code is

$$N_{corrected} = \frac{V_{ref}}{\Delta V_{noise}} = \frac{N_c \cdot N}{N_c + N} . \qquad (5)$$

In (4) and (5), N is the decimal value of the raw substrate coupling noise code, N_c is the decimal value of the calibration code, and V_{ref} is a DC reference voltage. The corrected noise code is given by (5). The noise in the reference voltage is the only source of error in the measured result. As in (2), the non-substrate related noise components of the measured results can be larger than the substrate noise voltage. The substrate noise cannot be measured without removing these non-substrate related noise components. With the use of an offset cancellation technique, the measured substrate noise is significantly more accurate and reliable. Furthermore, all of the noise acquisition processes including the A/D conversion are accomplished on-chip, therefore, complicated external test circuitry is not needed for this proposed substrate noise test circuit. The accuracy and error characteristics of this circuit are analyzed in the following section.

V. Accuracy and Error Analysis

Most of the offset voltage of an integrator is removed by the calibration technique [see (3), (4), and (5)]. However, due to the randomness of many noise sources such as power/ground noise, 1/f noise, and thermal noise at the integrator output, the noise can only be completely removed if N and $N_c \rightarrow \infty$. The remaining error after the calibration process is

$$\Delta V_n = \sum_{k=0}^{N-1} \delta_k(t) - \frac{N}{N_c} \sum_{k=0}^{N_c-1} \zeta_k(t) \quad , \qquad (6)$$

where δ_k is the noise voltage per clock cycle during sampling, and ζ_k is the noise voltage per clock cycle generated during the calibration process.

Based on this analysis, a smaller measurement error is achieved if the reference voltage is large (large N). Since the substrate coupling voltage is usually small, the sensing

capacitance cannot be excessively small. Increasing the size of the sensing transistor M_1 also reduces the error and improves the linearity of C_d. In the integrator circuit shown in Fig. 5, the ratio of C_d to C_f is 0.1. As long as the OPAMP operates in the linear range, a larger reference voltage is preferable to enhance measurement accuracy.

VI. Simulation Results

The proposed test circuit including the integrator, comparator, counter, and the on-chip timing circuit has been simulated using SPICE. The sensing MOS capacitor has a width of 15 μm and a length of 1.8 μm. The total capacitance of C_d is about 89 fF. The voltage at the C_d input node is set at 30 mV and 0 mV for generating the raw and calibration codes, respectively.

Two codes, the raw code and the calibration code, are also generated from SPICE. The SPICE simulation of the comparator output is shown in Fig. 6. As shown in Fig. 6, the comparator changes from 0 to 1 when the integrator output reaches 600 mV (the reference voltage V_{ref}). The calculated code from (1) is 178 and the simulated raw code is 235. A calibration code of 720 is obtained after the calibration process. From (5), the calibrated code is 177, which is quite close to the actual (calculated) code of 178. The same procedures have been applied to various substrate noise voltages. These results are shown in Fig. 7. The raw simulation results are different as compared to the calculated (actual) values caused by the OPAMP offset and other noise components. The SPICE simulation produces a calibration code N_c of 720. From (5), the raw codes are calibrated and are depicted in Fig. 7. As shown in Fig. 7, the calibrated codes are close to the calculated codes. The difference between the calibrated code and the calculated (raw) code is less than 0.4%.

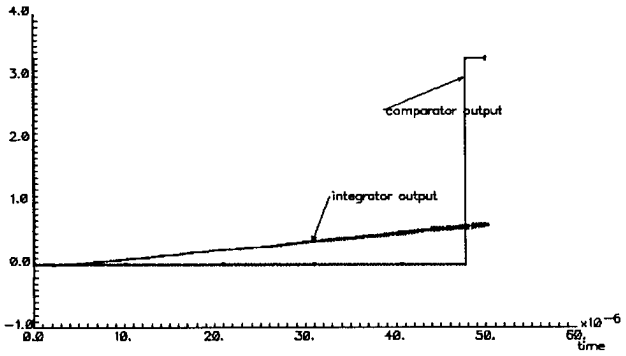

Fig. 6: SPICE derived waveforms of the integrator and comparator outputs. V_{ref} = 800 mV, f = 5 MHz, and the output is 235.

VII. Conclusions

The proposed test circuit can accurately measure substrate coupling noise. The measurement technique can be used to analyze different types of substrates. With this test circuit, different substrate coupling models can be evaluated.

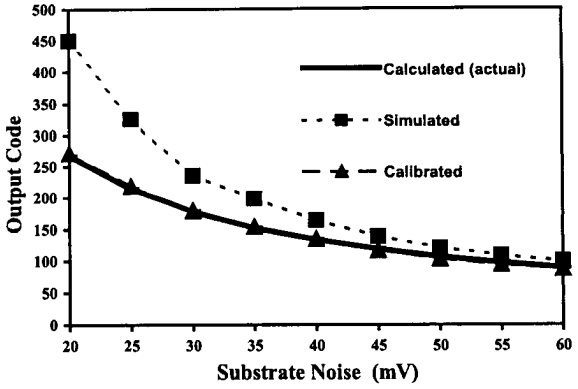

Fig. 7: Comparison of calculated, simulated, and calibrated output digital codes

The proposed substrate noise test circuit has an on-chip calibration function to remove extraneous noise sources from the test results. With this calibration step, only the substrate coupling noise is included in the digital output code. Less than 0.4% error from the actual value is achieved. This test circuit includes a simple on-chip analog-to-digital converter so that the measured substrate coupling noise is in the form of a digital code. With this proposed circuit, the noise voltages from the pads, bounding wires, package frame, and external cables/fixture do not affect the accuracy of the measurement. The only noise source that can affect the accuracy of the measurement is from the reference voltage. In order to enhance the measurement accuracy, a low noise reference voltage is therefore preferable.

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