INDUCTIVE INTERCONNECT WIDTH OPTIMIZATION FOR LOW POWER

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ABSTRACT

The width of an interconnect line affects the total power consumed by a circuit. A tradeoff exists, however, between the dynamic power and the short-circuit power in determining the width of inductive interconnect. The optimum line width that minimizes the total transient power dissipation is determined in this paper. A closed form solution for the optimum width with an error of less than 6% is presented. For a specific set of line parameters and resistivities, the power is reduced by almost 80% as compared to a minimum wire width. Considering the driver size in the design process, the optimum wire and driver size that minimizes the total transient power is also determined.

1. INTRODUCTION

With decreasing feature size in CMOS circuits, interconnect design has become an important issue in high speed, high complexity integrated circuits (IC). With the increase in signal frequencies and the corresponding decrease in signal transition times, the interconnect impedance can behave inductively, producing on-chip noise. Inductive behavior can, however, be exploited. As shown in [1], a properly designed inductive line can reduce the total power dissipated by long interconnect such as high speed clock distribution networks or data busses. Clock networks can dissipate a large portion of the total power consumed by a synchronous IC, ranging from 25% to as high as 70% [2]. The technique proposed here can be used to reduce the overall power being dissipated by a high speed clock distribution network.

Many algorithms have been proposed to determine the optimum wire size that minimizes a cost function such as delay [3]. As the inductance becomes important, certain algorithms have been enhanced to consider an *RLC* model [4]. Previous studies in wire and driver sizing do not consider the change in signal characteristics accompanied with a change in the line inductive impedance characteristics. The criteria that minimize delay are based on an unrealistic inductance model and, furthermore, do not consider power dissipation. The work described in [5] minimizes power dissipation while ignoring the effect of line inductance on the power characteristics.

In this paper, the tradeoff between short-circuit and dynamic power in inductive interconnect is introduced. The optimum line width that minimizes the total power dissipation is determined. As the line driver has an important effect on the signal and power dissipation characteristics, a closed form solution for the simultaneous driver and wire sizing problem that minimizes the total transient power dissipation is presented.

The paper is organized as follows. In section 2, the transient power characteristics of inductive interconnect are discussed. A power optimization criterion is formulated in section 3. Some simulation results are presented in section 4. In section 5, the effects of line material and length on the optimum interconnect width is exemplified. Some conclusions are discussed in section 6.

2. POWER CHARACTERISTICS OF INDUCTIVE INTERCONNECT

The transient power characteristics of inductive interconnect are presented in this section. The research described in [1] uses wire sizing techniques to reduce the total transient power dissipated by a clock distribution network; however, a closed form solution to determine the optimum interconnect width is not provided. This model also ignores the change in circuit behavior that occurs when the width of the line is increased. The matching response between the line and the driver plays an important role in the transient power dissipation. In [1], the driver size is also not considered as a design variable.

The dependence of the power dissipation on the interconnect width is illustrated in Fig. 1. As the line inductance increases, the short-circuit power decreases for wider interconnect.

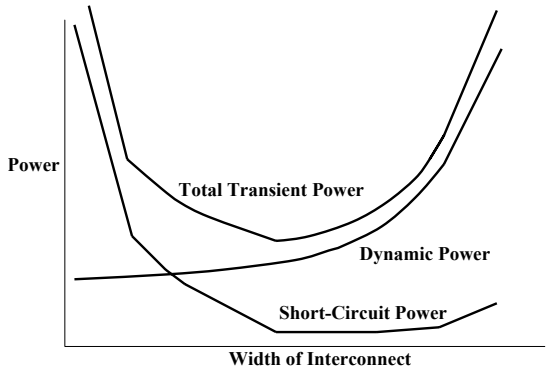

Figure 1: Short-circuit, dynamic, and total transient power dissipation as a function of the width of the interconnect line

If the interconnect exceeds a certain width, the short-circuit power begins to increase. The dynamic power increases with line width as the line capacitance increases. As

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shown in Fig. 1, a tradeoff exists between dynamic and short-circuit power in sizing inductive interconnect.

For the circuit shown in Fig. 2, a long interconnect line connecting two CMOS inverters can be modeled as a lossy transmission line. A change in the line width primarily affects the dynamic power of Inv_1 P_{1d}, and the short-circuit power of Inv_2 P_{2sc}. The dynamic power of Inv_2 depends on the load capacitance, and is not affected by the wire size. The change in the short-circuit power of Inv_1 is negligible, assuming a fixed signal transition time at the input of Inv_1. P_{1d} is given by $P_{1d} = f {V_{dd}}^2 C_1$, where f is the operating frequency, C_1 is the total capacitance driven by Inv_1, and V_{dd} is the supply voltage. The short-circuit power dissipation within the load gate P_{2sc} is directly proportional to the input signal transition time, which is the signal transition time at the far end of an interconnect line. P_{2sc} can be represented as

$$P_{2sc} = G(V_{dd}, V_t, K, C_L)\ \tau_0\ f, \tag{1}$$

where τ_0 is the transition time of the input signal at the load gate, and $G(V_{dd}, V_t, K, C_L)$ is a function of V_{dd}, threshold voltage V_t, transconductance K of the load gate, and capacitive load C_L. The general form of (1) is valid whether the load is modeled as a capacitive load, a lossless transmission line, or a lossy transmission line. G is also a function of τ_0; however, the dependence of G on τ_0 is small.

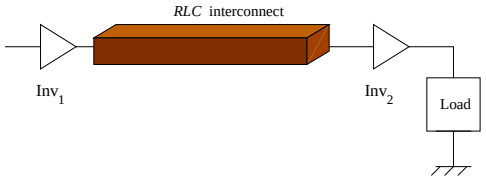

Figure 2: CMOS gates connected by an RLC interconnect

At small interconnect widths, the characteristic line impedance Z_{lossy} is large as compared to the equivalent output resistance of the transistor R_{tr}. Thus, the line is overdriven (the underdamped condition). Z_{lossy} decreases with increasing line width. The line remains underdamped until Z_{lossy} equals R_{tr}. A further increase in the line width underdrives the line as Z_{lossy} becomes less than R_{tr}. As the line width is increased, the line driving condition changes from overdriven to matched to underdriven [6].

For an overdriven line, the short-circuit power dissipation changes with line width as shown in Fig. 3. For an underdriven line, however, an increase in the line width increases the short-circuit power. To characterize this behavior, a closed form expression for the signal transition time is presented in section 3.

3. OPTIMUM INTERCONNECT WIDTH FOR MINIMUM POWER

An optimization criterion for wire sizing is presented in this section. The total transient power is expressed in terms of two design parameters, the interconnect width and the driver size.

Previous research in wire sizing has not considered the change in the line inductive impedance characteristics with a change in the line width. As described in section 2, a change

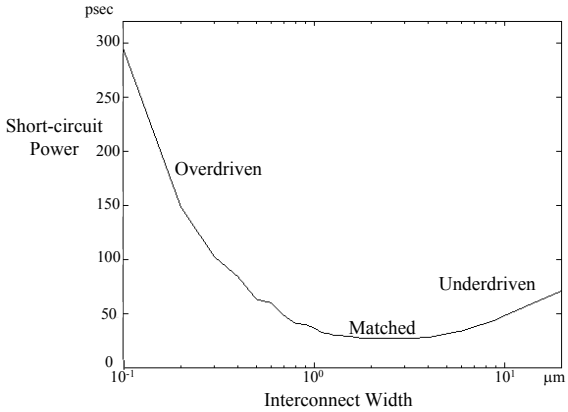

Figure 3: Short-circuit power of the load gate

in the line impedance characteristics affects the power dissipation characteristics. Specifically, in previous research the behavior of the short-circuit power has not been included as a part of the optimization process. Ignoring the interconnect matching characteristics between the driver and load may also lead to a non-optimal solution.

From the discussion presented in section 2, the geometric width (the effective impedance) of the driver also plays an important role in the matching response and the total transient power dissipation. Two complementary effects occur. As the driver size increases, the transition time of the output signal decreases and, consequently, the short-circuit power of the load gate decreases. Simultaneously, the gate input capacitance of the driver increases as the width of the driver becomes larger, increasing the power required to charge the gate capacitance.

For an inverter driving N gates, as shown in Fig. 4, the total transient power dissipation $P_{tdrive}(W_{INT}, W_n)$ is a function of two design parameters. W_{INT} is the line width and W_n is the NMOS transistor width of the driver (a symmetric driver is assumed).

$$\begin{aligned} P_{tdrive}(W_{INT}, W_n) &= P_{1d}(W_{INT}) \\ &+ N\,P_{2sc}(W_{INT}, W_n) + P_{drive}(W_n), \end{aligned} \tag{2}$$

where $P_{drive}(W_n)$ is the dynamic power required to charge the driver gate capacitance.

$$P_{driver}(W_n) = f {V_{dd}}^2 C_{driver}(W_n), \tag{3}$$

$$C_{drive}(W_n) = \alpha W_n (1 + \frac{\mu_n}{\mu_p}) L_n C_{ox}, \tag{4}$$

where $\frac{\mu_n}{\mu_p}$ is the the electron-to-hole mobility ratio, L_n is the feature size, C_{ox} is the gate oxide capacitance per unit area, and α is a constant characterizing the effective gate capacitance during different regions of operation.

The dynamic power of the driving inverter $P_{1d}(W_{INT})$ is a function of the interconnect width,

$$P_{1d}(W_{INT}) = f {V_{dd}}^2 C_1(W_{INT}), \tag{5}$$

$$C_1(W_{INT}) = NC_{2g} + C_{INT}(W_{INT}), \tag{6}$$

where C_{2g} is the gate capacitance of the load inverter, and $C_{INT}(W_{INT})$ is the total interconnect capacitance as a function of the interconnect width.

A closed form solution for the signal transition time at the far end of an inductive interconnect is determined. The

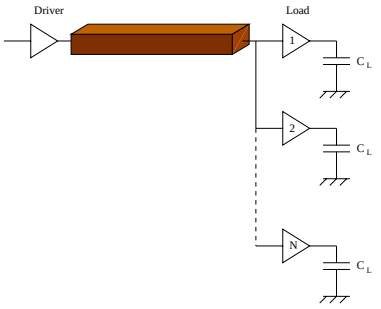

Figure 4: Inverter driving N logic gates

signal transition time is described in terms of the per unit length line impedance parameters. For a low-to-high input transition, an analytical expression for the signal at the far end of a line is

$$V(t) = V_c(\tau_{pOFF})\, e^{-\alpha_n (t-\tau_{pOFF})}, \qquad (7)$$

where τ_{pOFF} is the time at which the PMOS transistor of the driver turns off, $V_c(\tau_{pOFF})$ is the voltage of the load capacitance at τ_{pOFF}, and

$$\alpha_n = \frac{\frac{1+R_{INT}\gamma_n}{L_{INT}\gamma_n} + \sqrt{\left(\frac{1+R_{INT}\gamma_n}{L_{INT}\gamma_n}\right)^2 - \frac{4}{L_{INT}C_1}}}{2}, \qquad (8)$$

where $\gamma_n(W_n) = 1/R_n(W_n)$, R_n is the NMOS transistor equivalent resistance, and R_{INT} and L_{INT} are the total line resistance and inductance, respectively.

The transition time is expressed by $\tau_0 = \frac{t_{10\%} - t_{90\%}}{0.8}$, where $t_{10\%}$ and $t_{90\%}$ are the times at which the signal reaches 10% and 90% of the final value, respectively. Using closed form expressions for the line impedance parameters in terms of the line width, the transition time $\tau_0(W_{INT}, W_n)$ as a function of W_n and W_{INT} is obtained. The short-circuit power of the load inverter $P_{2sc}(W_{INT}, W_n)$ is used to obtain a closed form solution for the minimum power.

To obtain a closed form solution for the optimum width, expressions are presented for the line impedances that model the interconnect. R_{INT} is given by the well known formula $\frac{\rho}{W_{INT}\, T}$, where ρ and T are the line resistivity and thickness, respectively. C_{INT} is expressed in terms of the line dimensions for different line structures as described in [7].

An expression for the line inductance requires information describing the current return path. For an interconnect shielded by two ground lines, a closed form expression is obtained for the line inductance in terms of the line dimensions and the separation between the signal line and the ground lines. A shielded structure is commonly used in clock distribution networks [8].

Equation (2) is a nonlinear equation in two variables. Differentiating (2) with respect to W_{INT} and W_n and equating both expressions to zero, two nonlinear equations in W_{INT} and W_n are obtained. Numerical methods are used to solve these two expressions.

$$\frac{dP_{tdrive}}{dW_{INT}} = 0, \frac{dP_{tdrive}}{dW_n} = 0. \qquad (9)$$

4. SIMULATION RESULTS

For a specific driver size, the total transient power dissipation is a function of the line width. Given a set of line parameters, the optimum line width can be obtained by determining the interconnect width that minimizes P_{tdrive}. Values of R_{INT}, C_{INT}, and L_{INT} are determined based on the following physical parameters, $\rho = 2.5\,\mu\Omega cm$ and $l = 5\,mm$, where l is the interconnect length. A $0.24\,\mu m$ CMOS driver inverter with $W_n = 15\,\mu m$ and $W_p = 30\,\mu m$ is also assumed.

A comparison between the analytic solution and circuit simulation for different loads is listed in Table 1. The error between the analytic solution and SPICE for the chosen range of values is less than 6%.

The optimum width for minimum power is compared with the optimum width for minimum delay. Listed in the last column in Table 1 is the per cent increase in signal propagation delay when the optimum line width for minimum power is considered rather than the optimum width for minimum delay. Note that the maximum increase in delay is about 20%.

Table 1: Simulation and analytical results of the optimum width for different loads

Number of Loads N	$W_{INT_{optimum}}(\mu m)$		Error (%)	Increase in delay (%)
	Analytical	SPICE		
1	0.51	0.50	+2.0	21.0
2	0.72	0.70	+2.0	10.8
5	1.06	1.00	+6.0	5.2
10	1.34	1.30	+3.1	4.2

For $N = 10$, the total transient power dissipation of a symmetric driver is illustrated in Fig. 5. Considering the driver size as a design variable, a different local minimum for the transient power dissipation exists for each driver size.

Furthermore, for each line width, a minimum transient power dissipation exists for each driver size. A global minimum for the transient power is obtained by determining the optimum value of each design variable. Considering the driver size as a design parameter, (2) is a function of two variables, permitting the global minimum for the power dissipation to be determined. For the example circuit shown in Fig. 4, the global minimum power is achieved at $W_{INT} = 2.8\,\mu m$ and $W_n = 57\,\mu m$. Rather than minimizing the total transient power, a closed form expression of the propagation delay is used to minimize the overall power-delay product. The global minimum power-delay product is achieved for this example at $W_{INT} = 2.0\,\mu m$ and $W_n = 54\,\mu m$.

5. EFFECTS OF INTERCONNECT RESISTIVITY AND LENGTH ON POWER DISSIPATION

The proposed criteria for interconnect width optimization are applied to different target circuits. The total transient power dissipation is obtained using three different interconnect widths; thin, optimum, and wide. Different case studies demonstrate the importance of the optimization process in reducing power. The optimum width is obtained for two line lengths, $l = 1$ mm (more resistive) and 5 mm (more inductive). For short (resistive) lines, the signal characteristics are not particularly sensitive to the line width. The optimum solution achieves a greater power reduction in more inductive lines.

Using the optimum width rather than the minimum width, the total power dissipation is decreased by reducing the

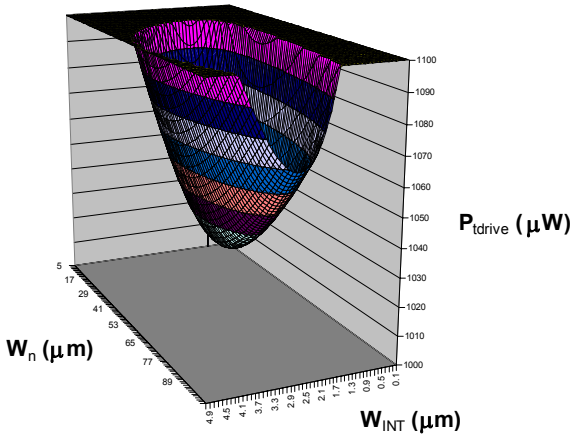

Figure 5: Total power dissipation with different wire and driver sizes for $N = 10$.

short-circuit power. As listed in Table 2, the optimum width of a copper line ($\rho = 1.7\,\mu\Omega cm$) reduces the total transient power by 68.5% for $l = 5$ mm as compared to 28.6% for $l = 1$ mm. For an aluminum line ($\rho = 2.5\,\mu\Omega cm$), a reduction of 77.9% is achieved as compared to 37.8%. The more inductive the interconnect, the more sensitive the power dissipation is to a change in the line width (and a change in the signal characteristics). Wire width optimization is, therefore, more effective for longer, more inductive lines.

A ten times wide line is used rather than the optimum line. Using the optimum width reduces the total power dissipation as compared to a wider line. The power reduction in this case is caused by a reduction in both power components (short-circuit and dynamic). The per cent reduction in power is listed in the final column of Table 2. For both line lengths, the power reduction in copper is higher than the power reduction in aluminum. For $l = 5$ mm, the per cent reduction in power is 27.8% for copper as compared to 25.4% for aluminum. A reduction in copper of 41.9% is obtained versus 37.4% in aluminum for $l = 1$ mm. This behavior is nonintuitive as the line resistance is higher for aluminum and both lines have the same capacitance and inductance. The power dissipation is actually higher for aluminum than for copper. The inductance-to-resistance ratio $\frac{L}{R}$ of copper is higher than in aluminum, increasing the importance of using the optimum width for less resistive (highly inductive) lines. Alternatively, for thin lines, the line resistance has a greater effect on the signal characteristics. The reduction in power is higher for aluminum than copper (compare, for example, the reduction in power in copper versus aluminum in the fourth and last columns).

6. CONCLUSIONS

It is shown in this paper that a tradeoff exists between dynamic and short-circuit power in determining the width of inductive interconnect. This tradeoff is not significant in resistive lines as the signal characteristics are less sensitive to the line dimensions. The short-circuit power of an overdriven interconnect line decreases with line width, while the dynamic power increases. When the line exceeds the matched condition, not only the dynamic power but also the short-circuit power increase with increasing line width.

Table 2: Power reduction for different metal line resistivities and dimensions

	Total Transient Power Dissipation (μW)				
	Resistive Line (l = 1 mm)				
ρ ($\mu\Omega\,cm$)	Optimum	Thin	Improve	Wide	Improve
Cu (1.7)	583	817	28.6 %	808	27.8 %
Al (2.5)	606	976	37.8 %	813	25.4 %
	Inductive Line (l = 5 mm)				
Cu (1.7)	1121	3563	68.5 %	1931	41.9 %
Al (2.5)	1236	5592	77.9 %	1973	37.4 %

For a long inductive interconnect line, an optimum interconnect width exists that minimizes the total transient power dissipation. A closed form solution is presented for determining this optimum width. This solution has high accuracy, producing an error of less than 6%. The optimum line width is shown to be more effective in reducing the total transient power as the line becomes longer. With aluminum interconnect, a reduction in power of about 78% and 37% is obtained as compared to thin and wide wires, respectively. For copper interconnect, a reduction in power of 68% and 42% is obtained for the same conditions. The optimum interconnect width depends upon both the driver size and the number of load gates. With this solution, the optimum driver and wire size can be simultaneously determined.

7. REFERENCES

[1] Y. I. Ismail, E. G. Friedman, and J. L. Neves, "Exploiting On-Chip Inductance in High Speed Clock Distribution Networks," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 9, No. 6, pp. 963 - 973, December 2001.

[2] C. J. Anderson *et al.*, "Physical Design of a Fourth-Generation POWER GHz Microprocessor," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 232-233, February 2001.

[3] J. J. Cong, K. Leung, and D. Zhou, "Performance-Driven Interconnect Design Based on Distributed *RC* Delay Model," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 14, No. 3, pp. 321-336, March 1995.

[4] Q. Zhu and W. M. Dai, "High-Speed Clock Network Sizing Optimization Based on Distributed *RC* and Lossy *RLC* Interconnect Models," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 15, No. 9, pp. 1106-1118, September 1996.

[5] J. Lillis, C. Cheng, and T. Y. Lin, "Optimal Wire Sizing and Buffer Insertion for Low Power and a Generalized Delay Model," *IEEE Journal of Solid State Circuits*, Vol. 31, No. 3, pp. 437-447, March 1996.

[6] M. A. El-Moursy and E. G. Friedman, "Optimizing Inductive Interconnect for Low Power," *Proceedings of the International Workshop on System-on-Chip for Real-Time Applications*, pp. 206-216, July 2002.

[7] N. Delorme, M. Belleville, and J. Chilo, "Inductance and Capacitance Analytic Formulas for VLSI Interconnects," *Electronics Letters*, Vol. 32, No. 11, pp. 996-997, May 1996.

[8] Y. Lu, K. Banerjee, M. Celik and R. W. Dutton, "A Fast Analytical Technique for Estimating the Bounds of On-Chip Clock Wire Inductance," *Proceedings of the IEEE Custom Integrated Circuits Conference*, pp. 241-244, May 2001.