Electrical Characteristics of Multi-Layer Power Distribution Grids

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Abstract— The design of robust and area efficient power distribution networks for high speed, high complexity integrated circuits has become a challenging task. The integrity of the high frequency signals depends upon the impedance characteristics of the on-chip power distribution networks. The electrical characteristics of these multi-layer power distribution grids and the relevant design implications are the subject of this paper. Each grid layer within a multi-layer power distribution grid typically has significantly different electrical properties. Unlike single layer grids, the electrical characteristics of a multi-layer grid can vary significantly with frequency. As the frequency increases, a large share of the current flow is transfered from the low resistance upper layers to the low inductance lower layers. The inductance of a multi-layer grid therefore decreases with frequency, while the resistance increases with frequency. Therefore, as compared to power distribution grids built exclusively in the upper, low resistance metal layers, a multi-layer power distribution grid extending to the lower interconnect layers exhibits superior high frequency impedance characteristics. An analytic model is also presented to determine the impedance characteristics of a multi-layer grid from the inductive and resistive properties of the comprising individual grid layers.

I. Introduction

The design of on-chip multi-layer power distribution grids in high speed integrated circuits (ICs) has become a challenging problem. The increase in die size, the larger number of interconnect layers, and the decreasing line pitch have all increased the physical complexity of the power grid structure. Furthermore, inductive effects in on-chip interconnect have become more significant with increasing circuit speed. Robust and area efficient design of multi-layer power distribution grids therefore requires a thorough understanding of the electrical properties of these interconnect structures.

The on-going miniaturization of integrated circuit (IC) feature size has increased the average current per circuit area as well as the slew rate of the current transients with each technology generation, placing strict requirements on the on-chip power distribution network. The high currents cause large ohmic IR voltage drops and the fast current transients cause large inductive $L\frac{di}{dt}$ voltage drops (ΔI noise) in power distribution networks. To maintain the local supply voltage within specified design margins, power distribution networks should be low impedance as seen from the power terminals of the circuit elements.

The use of decoupling capacitors is an effective technique to reduce the inductance of the power distribution networks at high frequencies. The efficacy of decoupling capacitors depends on the impedance of the conductors connecting the capacitors to the power load and source. Optimal allocation of on-chip decoupling capacitance depends upon the impedance characteristics of the interconnect. Robust and area efficient design of multi-layer power distribution grids therefore requires a thorough understanding of the impedance properties of the power distributing interconnect structures.

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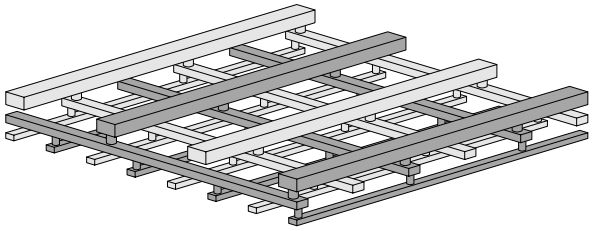

Fig. 1. A multi-layer power distribution grid. The ground lines are light grey, the power lines are dark grey.

Power distribution networks in high performance digital ICs are commonly structured as a multi-layer grid, as shown in Fig. 1. The electrical properties of these multi-layer grids are the subject of this paper.

The paper is organized as follows. Existing work on the electrical properties of power distribution grids is reviewed in Section II. The electrical properties of multi-layer power distribution grids are discussed in Section III. A case study of a two layer power grid is presented in Section IV. The design implications of the impedance properties of a multi-layer grid are discussed in Section V. The conclusions are summarized in Section VI.

II. Background

On-chip power distribution grids have traditionally been considered as resistive networks [1]. The inductance of the on-chip power distribution networks has been neglected because the network inductance has been dominated by the parasitic inductance of the package pins, traces, and bond wires. This situation is changing due to the higher switching speeds of integrated circuits [2] and the lower inductance of advanced flip chip packaging. Priore noted in [3] that replacing wide power and ground lines with narrower interdigitated power and ground lines reduces the self inductance of the supply network. Zheng and Tenhunen [4] proposed replacing the wide power and ground lines with an array of interdigitated narrow power and ground lines, decreasing the characteristic impedance of the power grid.

The inductive properties of single layer power grids have been described by the authors in [5]. In grid layers with alternating power and ground lines, long distance inductive coupling is greatly diminished due to cancellation, turning the inductive coupling into, effectively, a local phenomenon. The grid inductance, therefore, behaves similarly to the grid resistance: increases linearly with grid length and decreases inversely linearly with grid width (*i.e.*, the number of lines in the grid). The electrical properties of power distribution grids can therefore be conveniently expressed by a dimension-independent sheet resistance $R_\square$ and sheet inductance $L_\square$ [6]. The inductance of the power grid layers can be efficiently estimated using simple models comprised of a few interconnect lines.

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Area/inductance/resistance tradeoffs in power distribution grids have also been investigated [6]. The sheet inductance of power distribution grids is shown to increase linearly with line width under two different tradeoff scenarios. Under the constraint of constant grid area, a tradeoff exists between the grid inductance and resistance. The variation of inductance with frequency in single layer power grids has been characterized in [7]. This variation is relatively moderate, typically less than 10% of the low frequency inductance.

Power distribution grids in modern integrated circuits typically consist of many grid layers, spanning an entire stack of interconnect layers. The objective of the present investigation is to characterize the electrical properties of these multi-layer grids, advancing the existing work beyond individual grid layers.

III. Electrical properties of multi-layer grids

The power and ground lines within each layer of a multi-layer power distribution grids are orthogonal to the lines in the adjacent layers. Orthogonal lines have zero mutual partial inductance as there is no magnetic linkage [8]. Orthogonal grid layers can therefore be evaluated independently. A multi-layer grid can be considered to consist of two stacks of layers, with all of the lines in each stack parallel to each other, as shown in Fig. 2. Grid lines in one stack are orthogonal to the lines in the other stack. Grid layers in each stack only affect the grid inductance in the direction of the lines in the stack. This behavior is analogous to the properties of grid resistance.

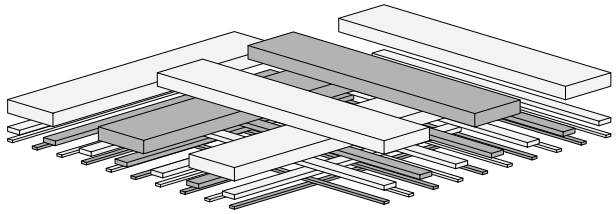

Fig. 2. A multi-layer grid consists of two stacks of layers. The lines in each stack are parallel to each other. The layers in one stack determine the resistive and inductive characteristics of the multi-layer grid in the direction of the lines in that stack, while the layers in the other stack determine the characteristics in the orthogonal direction.

To characterize a multi-layer grid, the electrical properties of the two stacks of single layer grids, as shown in Fig. 2, need to be determined. The problem is thereby reduced to determining the impedance characteristics of a stack of several individual grid layers with lines in the same direction.

The layers of a typical multi-layer power distribution grid have significantly different electrical properties. Lines in the upper layers tend to be thick and wide, forming a low resistance global power distribution grid. Lines in the lower layers tend to be thinner, narrower, and have a smaller pitch. The lower the metal layer, the smaller the metal thickness, width, and pitch. The upper grid layers therefore have a relatively high inductance and low resistance, whereas the lower layers have a relatively low inductance and high resistance [6]. The lower the layer, the higher the resistance and the lower the inductance of that layer.

The variation with frequency of the impedance of each layer in a grid stack comprised of N grid layers is schematically shown in Fig. 3. The layers are numbered from 1 (the uppermost layer) to N (the lowest layer). The grid layer resistance increases with layer number, $R_1 < R_2 < \ldots < R_N$, and the inductance decreases with layer number, $L_1 > L_2 > \cdots > L_N$. At low frequencies, the uppermost layer has the lowest impedance as the layer with the lowest resistance. This layer, however, has the highest inductance and, consequently, the lowest transition frequency $f_1 = \frac{1}{2\pi}\frac{R_1}{L_1}$, as compared to other layers (see Fig. 3). The transition frequency is the

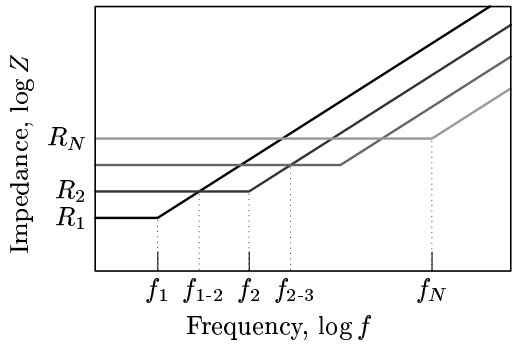

Fig. 3. Impedance of the individual grid layers comprising a multi-layer grid.

frequency at which the impedance of a specific grid layer changes in character from resistive to inductive. At this frequency, the inductive impedance of a grid layer is equal to the resistive impedance (neglecting skin and proximity effects), *i.e.*, $R_1 = \omega L_1$. The grid impedance increases linearly with frequency above f_1. The lowest grid layer has the highest resistance and the lowest inductance; therefore, this layer has the highest transition frequency f_N. As the inductance of the upper layers is higher than the lower layers, the impedance of an upper layer exceeds the impedance of any lower layer above a certain frequency. For example, the impedance of the first layer $R_1 + \omega L_1 \approx \omega L_1$ equals the magnitude of the second layer impedance $R_2 + \omega L_2 \approx R_2$ and exceeds the impedance of this layer above frequency $f_{1\text{-}2} = \frac{1}{2\pi}\frac{R_2}{L_1}$, as shown in Fig. 3. Similarly, the impedance of layer k exceeds the impedance of layer l, $k < l$, at $f_{k-l} = \frac{1}{2\pi}\frac{R_l}{L_k}$.

An entire stack of grid layers cannot be accurately described by a single RL circuit due to the aforementioned differences among the electrical properties of the individual grid layers. A stack of multiple grid layers can, however, be modeled by several parallel RL branches, each branch characterizing the electrical properties of one of the comprising grid layers, as shown in Fig. 4. Note that this model disregards magnetic coupling among the grid layers. Magnetic coupling between two grid layers is significant only where the line pitch in both layers is the same and the separation between the two layers is smaller than the line pitch. This configuration is uncommon; therefore, magnetic coupling among grid layers can be generally neglected.

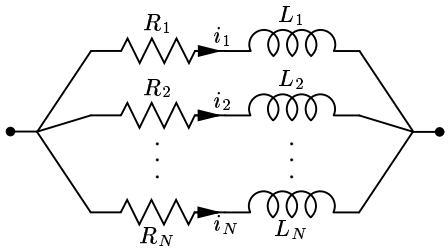

Fig. 4. Equivalent circuit of a stack of N grid layers.

Due to the difference in the electrical properties of the individual layers, the magnitude of the current in each grid layer varies significantly with frequency. At low frequencies, the low resistance uppermost layer is the path of lowest impedance, as shown in Fig. 3. The uppermost layer has the greatest effect on the overall low frequency resistance and inductance of the grid stack, as the largest share of the overall current flows through this layer. As the frequency increases to $f_{1\text{-}2} = \frac{1}{2\pi}\frac{R_2}{L_1}$ and higher, the impedance of the uppermost layer ωL_1 exceeds the impedance of the second uppermost layer R_2, as

shown in Fig. 3. The second uppermost layer, therefore, carries the largest share of the overall current and most affects the overall inductance and resistance within this frequency range. As the frequency exceeds $f_{2\text{-}3} = \frac{1}{2\pi}\frac{R_3}{L_2}$, the next layer in the stack becomes the path of least impedance and so on. The process continues until at very high frequencies the lowest layer carries most of the overall current.

As the frequencies increase, the majority of the overall current is progressively transfered from the layers of low resistance and high inductance to the layers of high resistance and low inductance. Therefore, the overall grid inductance decreases with frequency and the overall grid resistance increases with frequency. A qualitative plot of the variation of inductance with frequency is shown in Fig. 5. At low frequency, all of the layers exhibit a purely resistive behavior and the current is partitioned among the layers according to the resistance of each layer. The share of the overall current flowing through layer n is

$$i_n = \frac{I_n}{\sum_{k=1}^{N} I_k} = \frac{\prod_{k\neq n} R_k}{\sum_{l=1}^{N}\prod_{k\neq l} R_k}. \qquad (1)$$

Note that $i_1 > i_2 > \ldots > i_N$ as $R_1 < R_2 < \ldots < R_N$. The overall resistance of a multi-layer grid R_0^{LF} at low frequency is therefore determined by a parallel connection of all of the individual layer resistances,

$$R_0^{LF} = R_1 \| R_2 \| \ldots \| R_N = \frac{\prod_{k=1}^{N} R_k}{\sum_{l=1}^{N}\prod_{k\neq l} R_k}. \qquad (2)$$

The low frequency inductance of a multi-layer grid L_0^{LF} is, however,

$$L_0^{LF} = L_1 i_1^2 + L_2 i_2^2 + \ldots + L_N i_N^2 \approx L_1, \qquad (3)$$

due to $L_1 > L_k$ and $i_1 > i_k$ for any $k \neq 1$.

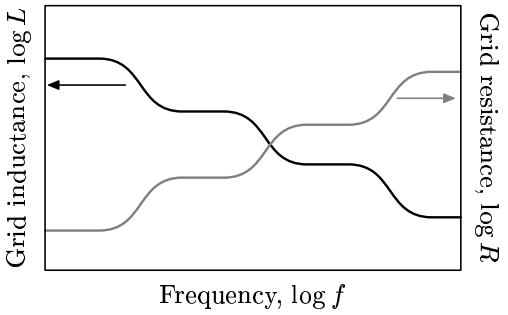

Fig. 5. Variation of inductance and resistance of a multi-layer stack with frequency. As the signal frequency increases, the current flow shifts to the high resistance, low inductance layers, decreasing the overall inductance of the grid and increasing the overall resistance.

At very high frequencies, the resistance and inductance exchange roles. All grid layers exhibit a purely inductive behavior and the current is partitioned among the layers according to the inductance of each layer. The share of the overall current flowing through layer n is

$$i_n = \frac{I_n}{\sum_{k=1}^{N} I_k} = \frac{\prod_{k\neq n} L_k}{\sum_{l=1}^{N}\prod_{k\neq l} L_k}. \qquad (4)$$

The relation among the currents of each layer is reversed as compared to the low frequency case: $i_1 < i_2 < \ldots < i_N$. The overall inductance of the multi-layer grid at high frequency L_0^{HF} is therefore determined by a parallel connection of the individual layer inductances,

$$L_0^{HF} = L_1 \| L_2 \| \ldots \| L_N = \frac{\prod_{k=1}^{N} L_k}{\sum_{l=1}^{N}\prod_{k\neq l} L_k}. \qquad (5)$$

The high frequency resistance of a multi-layer grid R_0^{HF} is

$$R_0^{HF} = R_1 i_1^2 + R_2 i_2^2 + \ldots + R_N i_N^2 \sim R_N, \qquad (6)$$

due to $R_N > R_k$ and $i_N > i_k$ for any $k \neq N$.

The grid resistance and inductance vary with frequency between these limiting low and high frequency cases. If the difference in the electrical properties of the layers is sufficiently high, the variation of the inductance and resistance with frequency has a staircase-like shape, as shown in Fig. 5. As the frequency increases, the grid layers consecutively serve as primary current paths, dominating the overall grid impedance within a specific frequency range.

IV. Case study of a two layer grid

The electrical properties of a two layer stack are evaluated in this section to quantitatively illustrate the concepts described in Section III. The parameters of the grid layers are described in Fig. 6. The inductance extraction program FastHenry [9] is used to explore the inductive properties of grid structures. A resistivity of 1.72 $\mu\Omega \cdot$ cm is used in the analysis, where an advanced process with copper interconnect is assumed [10].

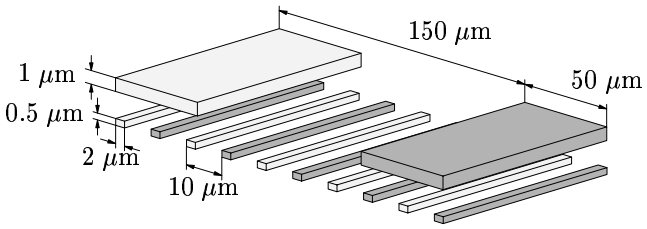

Fig. 6. General view of a two layer stack. The ground lines are white colored, the power lines are grey colored.

The FastHenry-extracted sheet inductance and sheet resistance of the two layer stack is shown in Figs. 7 and 8. Note that the inductance and resistance of the individual grid layers, also shown in Figs. 7 and 7, vary little with frequency. The inductance and resistance of the two layer stack, however, vary significantly with signal frequency due to current redistribution, as discussed in Section III.

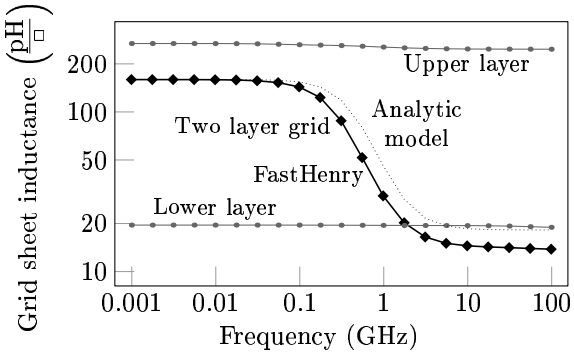

Fig. 7. Inductance of a two layer stack versus signal frequency. Both FastHenry data (solid line) and analytic model data (dotted line) are shown. The individual inductance of the two comprising grid layers is shown for comparison (FastHenry data).

The inductive and resistive characteristics of a two layer stack can also be analytically determined using the circuit model as shown in Fig. 4. Assuming $L_{12} = 0$ as discussed in Section III, the loop inductance and resistance of a two layer stack are, respectively,

$$L_0 = \frac{L_1(R_2^2 + \omega^2 L_1 L_2) + L_2(R_1^2 + \omega^2 L_1 L_2)}{(R_1 + R_2)^2 + \omega^2 (L_1 + L_2)^2}, \qquad (7)$$

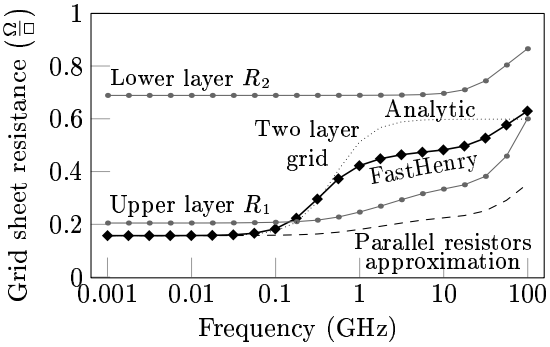

Fig. 8. Resistance of a two layer stack versus signal frequency. The individual resistance of the two comprising grid layers and the parallel resistance of the individual layer resistances are shown for comparison.

$$R_0 = \frac{R_1(R_1R_2 + \omega^2 L_2^2) + R_2(R_1R_2 + \omega^2 L_1^2)}{(R_1 + R_2)^2 + \omega^2(L_1 + L_2)^2} . \qquad (8)$$

The variation of the grid inductance and resistance with frequency according to the analytic models described by (7) and (8) is also illustrated in Figs. 7 and 8 by the dotted lines. The analytic model satisfactorily describes the variation of grid inductance and resistance with frequency. The discrepancy between the analytic and FastHenry data at high frequencies is due to proximity effects which are not captured by the model shown in Fig. 4.

Having determined the variation with frequency of the resistance and inductance in the previous sections, it is possible to characterize the frequency dependent impedance characteristics of a two layer stack. The impedance magnitude determined according to the analytic models (7) and (8) is shown in Fig. 9 by the dotted line. The low frequency values of the individual layer inductance, L_1 and L_2, and resistance, R_1 and R_2, are used in the analytic model. The impedance magnitude based on FastHenry extracted data is shown by the solid line. The extracted impedance of the individual grid layers is also shown for comparison. Note that the impedance characteristics of the individual layers shown in Fig. 9 bear close resemblance to the schematic graph shown in Fig. 3. As discussed in Section III, the low resistance upper grid layer dominates the impedance characteristics at low frequencies, while the low inductance lower grid layer determines the impedance characteristics at high frequencies.

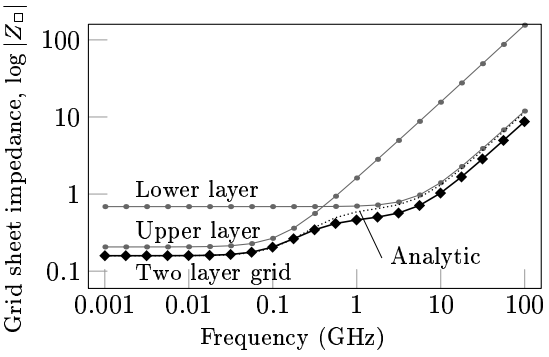

Fig. 9. Impedance magnitude of a two layer stack versus signal frequency. Both the extracted (solid line) and analytic (dotted line) data are shown. The impedance of the two comprising grid layers is also shown.

V. Design implications

Current redistribution among layers of a multi-layer grid has several beneficial effects. The impedance of a power distribution grid is minimized across an entire frequency spectrum, as shown in Fig. 3. The lower impedance of the current path between the power load and surrounding decoupling capacitors reduces the on-chip power supply noise. Relatively low inductance and high resistance at high frequencies increase the damping factor of the power distribution grid (proportional to $R/\sqrt{L}$), thereby preventing resonant oscillations in power distribution networks operating at high frequencies. Conversely, resonant oscillations are more likely at lower frequencies, where the inductance is relatively high and the resistance is low.

Redistribution of the grid current toward the lower layers at high frequencies increases the current density in the power and ground lines in these lower grid layers, degrading the electromigration reliability of the power distribution grid. The significance of these effects will increase as the frequency of the current delivered through the on-chip power distribution grid increases with higher operating speeds. An analysis of these effects is therefore necessary to ensure the design quality of high speed circuits.

VI. Conclusions

The electrical characteristics of multi-layer power distribution grids are investigated in this paper. The grid layers of a multi-layer power distribution grid typically have significantly different electrical properties. The upper metal layers comprised of thicker and wider lines are low resistance and high inductance; the lower metal layers comprised of thinner and narrower lines are relatively high resistance and low inductance. Due to this difference in layer properties, the electrical characteristics of multi-layer grids can vary significantly with frequency. As signal frequencies increase, the majority of the current flow shifts from the lower resistance upper layers to the lower inductance lower layers. The inductance of a multi-layer grid therefore decreases with frequency, while the resistance increases with frequency. A method to analytically determine the electrical properties of a multi-layer grid from the inductive and resistive properties of the comprising grid layers is described. The implications of these electrical characteristics on the design of high performance power distribution grids are also discussed. The electromigration reliability of the power and ground lines in the lower grid layers will degrade due to the increase in current density at high frequencies.

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