FORWARD BODY BIASED KEEPER FOR ENHANCED NOISE IMMUNITY IN DOMINO LOGIC CIRCUITS

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ABSTRACT

A forward body biased keeper circuit technique is proposed in this paper for enhancing the robustness of dynamic circuits. The proposed circuit technique is evaluated as an alternative to the standard approach of increasing the physical size of a keeper transistor for enhanced noise immunity. The forward body biased keeper circuit technique has a lower speed penalty under the same noise immunity conditions as compared to a standard keeper sizing technique. The effectiveness of the proposed circuit technique can be further increased provided that the junction temperature is reduced using active cooling and refrigeration.

1. INTRODUCTION

Domino logic circuit techniques are extensively applied in high performance microprocessors due to the superior speed and area characteristics of domino CMOS circuits as compared to static CMOS circuits [1]-[3]. High speed operation of domino logic circuits is primarily due to the lower noise margin of domino circuits as compared to static gates. This desirable property of a lower noise margin, however, makes domino logic circuits highly sensitive to noise as compared to static gates. Aggressive scaling of the threshold voltages to enhance speed further degrades the noise immunity of domino logic gates [1]. Moreover, exponentially increasing subthreshold leakage currents with reduced threshold voltages degrade the reliability of dynamic circuits fabricated in deep submicrometer CMOS technologies. As on-chip noise becomes more severe with technology scaling and higher operating frequencies, error free operation of domino logic circuits has become a major challenge [1]-[3].

In a standard domino logic gate, a feedback keeper is employed to maintain the state of the dynamic node against coupling noise, charge sharing, and subthreshold leakage current. The keeper transistor is fully turned on at the beginning of the evaluation phase. Provided that the necessary input combination to discharge the dynamic node is applied, the keeper and pulldown network transistors compete to determine the logical state of the dynamic node. This contention between the keeper and the pulldown network transistors degrades the circuit speed and power characteristics [1]. The keeper transistor is typically sized smaller than the pulldown network transistors in order to minimize the delay and power degradation caused by the keeper contention current. A small keeper, however, cannot provide the necessary noise immunity for reliable operation in an increasingly noisy and noise sensitive on-chip environment [1], [3]. There is, therefore, a tradeoff between reliability and high speed/energy efficient operation in domino logic circuits.

The forward body bias circuit technique is typically employed for reducing power consumption, enhancing speed, or compensating for die-to-die and within-die parameter variations [4], [5]. The forward body bias circuit technique is often seen as an alternative to the reverse body bias circuit technique due to the preferable scaling characteristics of the forward body bias technique. Contrary to the reverse body bias technique, forward body biasing a MOSFET enhances the body effect while reducing short-channel effects [4], [5].

A new use of the forward body bias technique is proposed in this paper for enhancing the noise immunity of dynamic circuits. Forward body biasing a keeper transistor is evaluated as an alternative to the standard approach of increasing the keeper size for enhanced robustness. The current drive of a keeper transistor is increased with the proposed circuit technique without modifying the physical dimensions of the keeper. By applying a forward body bias voltage of 550 mV to a keeper transistor at a worst case temperature of 120^{o}C, the noise immunity of an 8-bit multiplexer is enhanced by up to 7.5% while reducing the delay penalty by 4.1% as compared to the standard approach of increasing the keeper width.

The beneficial effect of reducing the die temperature on the forward body bias circuit technique is also evaluated. At room temperature, the enhancement in noise immunity based on the proposed circuit technique increases to 8.7% by increasing the forward body bias voltage to 700 mV. The delay penalty is 3.3% smaller as compared to the stan-

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dard approach of increasing the keeper size in order to achieve the same enhancement in noise immunity.

The operation of the proposed domino logic with forward body biased keeper (FBBK) circuit technique is described in Section 2. The speed and power overhead of the FBBK circuit technique is described in Section 3. Some conclusions are offered in Section 4.

2. FORWARD BODY BIASED KEEPER

Forward body biasing a keeper transistor is proposed to improve the noise immunity characteristics as compared to a standard domino logic circuit. The threshold voltage of a forward body biased MOSFET is reduced, increasing the conduction current as compared to a zero body biased transistor with the same physical dimensions. Forward body biasing the keeper, therefore, improves the noise immunity characteristics as compared to a standard domino logic circuit with the same keeper physical size. A K-bit domino multiplexer with a forward body biased keeper transistor is shown in Fig. 1.

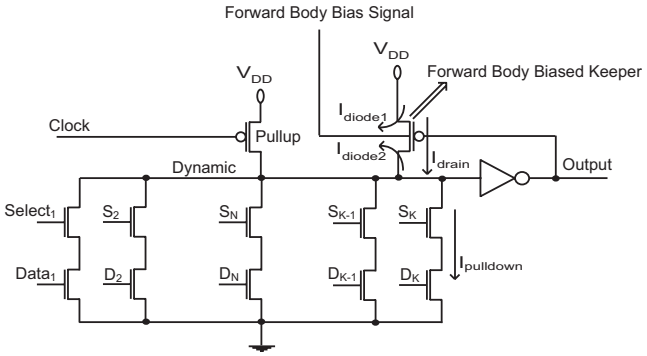


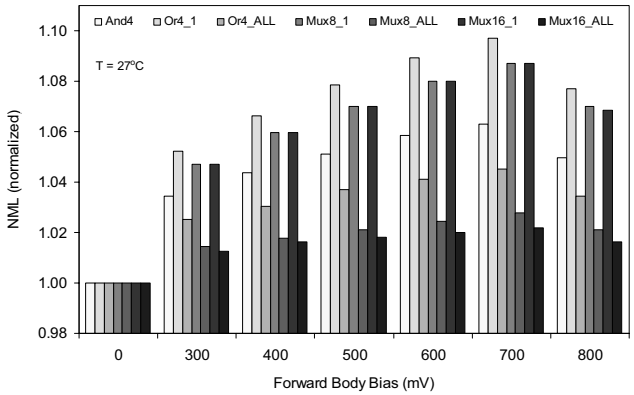
Fig. 1. A K-bit domino multiplexer based on the forward body biased keeper circuit technique.

When a keeper transistor is forward body biased, the source-to-body and drain-to-body p-n junctions produce diode currents as illustrated in Fig. 1. The forward body bias voltage that can be applied to a MOSFET is limited due to these diode currents [1], [4], [5]. The diode current through the drain-to-body p-n junction (I_{diode2}) opposes the drain current of a keeper transistor. For strongly forward body biased keepers, I_{diode2} can lower (clamp) the voltage of the dynamic node. The noise immunity can thereby be reduced, provided that the drain-to-body diode is strongly turned on.

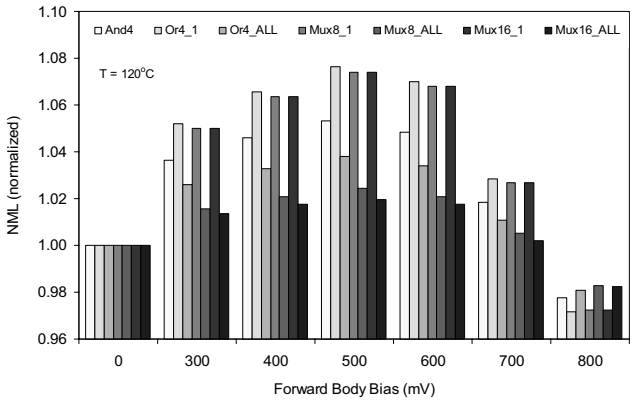
The low noise margin (NML) is the noise immunity metric used in this paper. The NML is

$$NML = V_{IL} - V_{OL}, \quad (1)$$

where V_{IL} is the input low voltage defined as the smaller of the DC input voltages on the voltage transfer characteristic (VTC) at which the rate of change of the output node voltage with respect to the input voltage is equal to one (the unity gain point on the VTC). V_{OL} is the output low voltage. The variation of the noise immunity of various domino logic circuits is evaluated by varying the forward body bias voltage, assuming a 0.18 μm CMOS technology, as shown in Fig. 2. The keeper to pulldown network equivalent transistor width ratio is two for all of the circuits.



(a)



(b)

Fig. 2. Variation of the noise immunity of four input And and Or gates and 8 bit and 16 bit multiplexers with the forward body bias voltage applied to a keeper transistor at two different junction temperatures. And4, Or4_ALL, Mux8_ALL, and Mux16_ALL: noise couples to all of the inputs. Or4_1, Mux8_1, and Mux16_1: noise couples to one input while all of the other inputs are grounded. (a) T = 27°C. (b) T = 120°C.

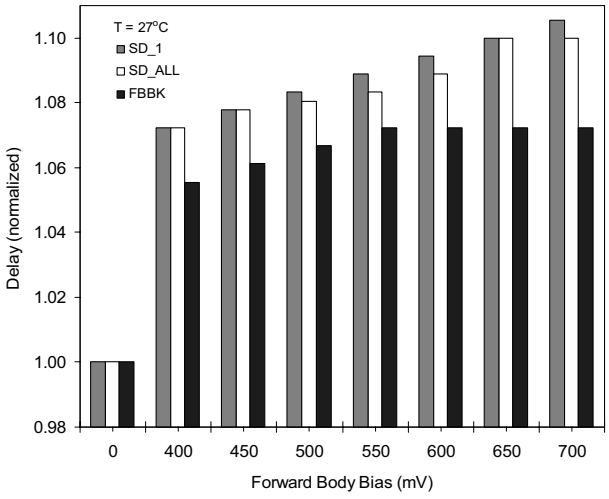
As shown in Fig. 2a, at room temperature, increasing the forward body bias voltage towards 700 mV enhances the noise margins of all of the domino logic circuits. For a forward body bias voltage of 700 mV, the enhancement in noise immunity varies between 2.2% (for a 16 bit multiplexer with noise coupling to all of the inputs, *Mux16_ALL*) and 9.7% (for a 4 input Or gate with noise coupling to only one input while the other inputs are grounded, *Or4_1*) for different types of circuits and noise coupling scenarios. As the forward body bias voltage is increased beyond 700 mV, the body diodes strongly turn on, degrading the noise immunity of the gates.

The current through a forward biased p-n junction is strongly dependent on the junction temperature [4], [5]. I_{diode2} exponentially increases as the die temperature is increased. Therefore, as shown in Fig. 2b, both the maximum achievable enhancement in noise immunity and the maximum forward body bias voltage that can be applied to a keeper transistor are reduced when the junction temperature is increased. For a worst case junction temperature of 120°C, the noise immunity is enhanced for forward body bias voltages up to 550 mV (for all circuits evaluated). As the forward body bias voltage is increased beyond 550 mV, the noise immunity degrades primarily due to the diode current through the forward biased drain-to-body p-n junction. For a forward body bias voltage of 500 mV, the enhancement in noise immunity varies between 2.0% (for *Mux16_ALL*) and 7.6% (for *Or4_1*) for different types of circuits and noise coupling scenarios.

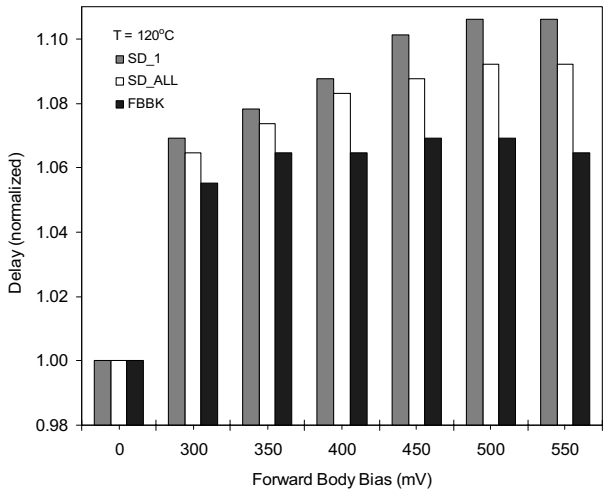
3. SPEED AND POWER OVERHEAD

The speed and power overhead of the proposed circuit technique is evaluated in this section. Similar to increasing the physical size of a keeper transistor, forward body biasing a keeper increases the contention current; thereby, degrading the evaluation speed and increasing the power consumption of a domino logic circuit. Since the standard approach for enhancing noise immunity is to increase the width of a keeper transistor, the proposed forward body biased keeper circuit technique is compared to standard domino logic circuits with increased keeper sizes while providing the same noise immunity characteristics. A comparison of the delay of an 8 bit domino multiplexer based on the standard domino (SD) circuit technique and the proposed forward body biased keeper circuit technique for different noise coupling scenarios is shown in Fig. 3. For each forward body bias voltage, the width of the keeper transistor of a standard domino multiplexer is increased to maintain the same noise immunity (assuming two different noise coupling scenarios) as compared to an FBBK multiplexer.

As described in Section 2, the diode currents increase with greater forward body bias (FBB) voltage; thereby degrading the voltage level of a dynamic node and reducing the effective current supplied by a keeper to support the state of the dynamic node. For a moderate FBB, the increased drain current due to the reduced threshold voltage dominates I_{diode2}. As shown in Fig. 3, the evaluation delay increases for FBB voltages up to a specific value (dependent on the junction temperature). Increasing the FBB voltage beyond this specific value (beyond 550 mV and 450 mV at 27°C and 120°C, respectively) enhances the evaluation speed due to the supporting role of I_{diode2} in the evaluation process. Alternatively, for a standard domino logic circuit, increasing the keeper size increases the contention current; thereby degrading the evaluation speed. The speed advantage of the proposed forward body biased keeper technique as compared to a standard domino logic circuit with the same noise immunity characteristics, therefore, increases as the forward body bias voltage is increased.



(a)



(b)

Fig. 3. Comparison of the delay overhead of an 8 bit domino multiplexer based on the FBBK technique as compared to the standard keeper sizing technique for two different junction temperatures. At each FBB voltage, the keeper size of a standard domino multiplexer is increased to maintain the same noise immunity as compared to a FBBK multiplexer. SD_1: noise couples to one input while the other inputs are grounded. SD_ALL: noise couples to all of the inputs. All of the values are normalized to the delay of the SD multiplexer with the same keeper size as compared to the FBBK multiplexer. (a) T = 27°C. (b) T = 120°C.

At room temperature, the delay penalty for increasing the noise immunity by 8.7% (V_{FBB} = 700 mV) is 3.3% smaller as compared to a standard domino logic circuit based on keeper sizing (assuming the noise couples to only one input). Similarly, at 120°C, the delay penalty for achieving a 7.5% higher noise immunity (V_{FBB} = 550 mV) is 4.1% smaller as compared to the delay penalty of the standard technique of increasing the keeper size.

Short-circuit current within the output inverter increases due to a degradation in the voltage of the dynamic node as the forward body bias voltage is increased. Due to increasing contention, diode, and short-circuit currents and increasing junction capacitances, the power consumption increases with the proposed FBBK circuit technique as compared to a standard domino logic circuit with the same size keeper. A comparison of the power consumption of an 8 bit domino multiplexer based on the SD circuit technique and the proposed FBBK circuit technique for different noise coupling scenarios is shown in Fig. 4.

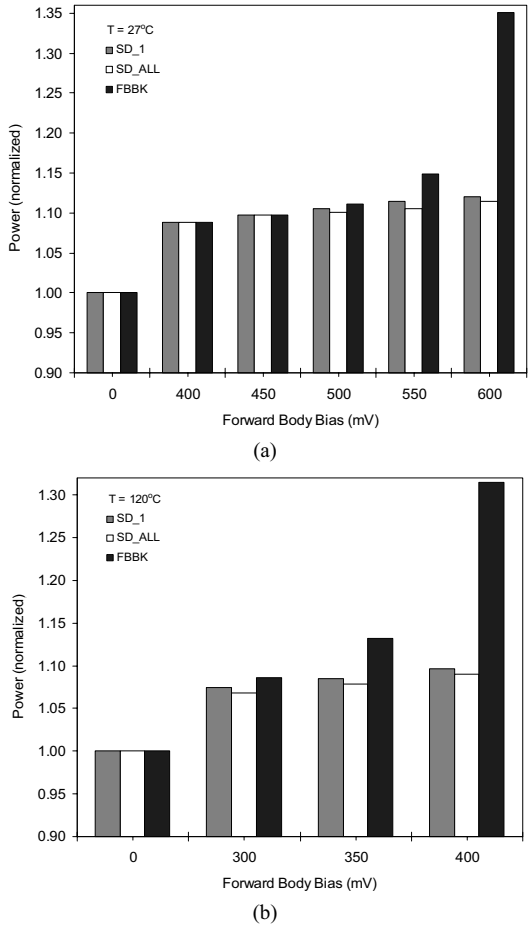


Fig. 4. Comparison of the power overhead of an 8 bit domino multiplexer based on the FBBK technique as compared to the standard keeper sizing technique for two different junction temperatures. All of the values are normalized to the power consumed by the SD multiplexer with the same keeper size as compared to the FBBK multiplexer. Simulation conditions are as described in the caption of Fig. 3. (a) T = 27°C. (b) T = 120°C.

As shown in Fig. 4, the rate of increase in power consumption with the forward body bias voltage is relatively small for moderate FBB voltages (below 550 mV and 350 mV for 27°C and 120°C, respectively). As the FBB is increased beyond these voltages, the power consumption rapidly increases due to the significantly higher diode currents. At room temperature, the power overhead of the FBBK and standard keeper sizing circuit techniques is similar for FBB voltages up to 500 mV. The FBBK circuit technique increases the power consumption by up to 3.9% and 21.3% for FBB voltages of 550 mV and 600 mV, respectively, as compared to the standard keeper sizing technique while maintaining the same noise immunity. Similarly, at 120°C, the power overhead of the FBBK and standard keeper sizing techniques is similar for FBB voltages up to 300 mV. The FBBK circuit technique increases the power consumption by up to 4.9% and 20.6% for FBB voltages of 350 mV and 400 mV, respectively, as compared to the standard domino logic circuit technique based on increasing the keeper size while providing the same noise immunity.

4. CONCLUSIONS

A forward body biased keeper circuit technique is proposed in this paper for enhanced noise immunity in domino logic circuits. Various domino logic circuits are evaluated based on the proposed circuit technique. The achievable enhancement in noise immunity based on the forward body biased keeper circuit technique is strongly dependent on the junction temperature. Up to a 7.6% enhancement in noise immunity is achieved by applying a 500 mV forward body bias to a keeper transistor at a worst case temperature of 120°C, assuming a 0.18 μm CMOS technology. The effectiveness of the proposed forward body biased keeper technique increases provided that the junction temperature is reduced via active cooling and refrigeration. The enhancement in noise immunity increases to 9.7% for a forward body bias voltage of 700 mV at 27°C.

At room temperature, the power overhead of the forward body biased keeper circuit technique as compared to the standard keeper sizing technique is less than 3.9% for body bias voltages below 550 mV. By applying a forward body bias voltage of 550 mV, the noise immunity of an 8 bit multiplexer is enhanced by up to 7.6% with a 1.7% smaller speed penalty as compared to the standard keeper sizing technique.

5. REFERENCES

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