EXPONENTIALLY TAPERED H-TREE CLOCK DISTRIBUTION NETWORKS

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Abstract—**Exponentially tapered interconnect can reduce the dynamic power dissipation of clock distribution networks. A criterion for sizing H-tree clock networks is proposed. The technique reduces the power dissipated by an example clock network by up to 12% while preserving the signal transition times and propagation delays. Furthermore, the inductive behavior of the interconnects is reduced, decreasing the inductive noise. Exponentially tapered interconnects reduce by approximately 20% the difference between the overshoots in the signal at the input of a tree as compared to a uniform tree with the same area overhead.**

1. Introduction

With the decrease in feature size of CMOS integrated circuits (IC), interconnect design has become a primary issue in high speed ICs. Interconnect design is most often used to increase circuit speed; however, the interconnect also affects the power dissipated by a circuit [1]. Clock networks can dissipate a large portion of the total power dissipated within a synchronous IC. In this paper, an interconnect shaping technique is proposed to reduce the power dissipated by an H-tree structured clock distribution network without degrading the signal characteristics.

For global clock networks, H-trees are highly efficient in reducing clock skew [2]. With increasing signal frequencies and a corresponding decrease in signal transition times, the interconnect impedance can behave inductively [3]. The line widths within an H-tree are typically divided by two at the branch points to reduce reflections. The proposed criterion does not maintain a tapering factor of two in sizing the interconnects in H-trees. Exponentially tapered interconnects, as shown in Fig. 1, are proposed. The proposed design methodology not only decreases the transient power dissipation but also reduces the inductive behavior of the interconnects.

The paper is organized as follows. In section 2, the proposed criterion for tapering an H-tree network is presented. Different issues that affect the proposed technique are discussed in section 3. In section 4, simulation results are presented. Some conclusions are provided in section 5.

2. Tapered H-Tree For Minimum Power

Exponential tapering has been shown to be the optimum shape function to produce the minimum signal propagation

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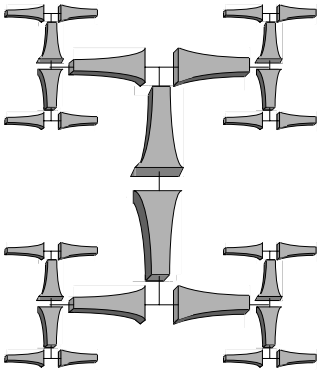

Figure 1: Exponentially tapered H-tree

delay in RLC lines [1]. A tapered line, shown in Fig. 2a, can achieve the same signal characteristics (signal delay and transition time) of the uniform line shown in Fig. 2b with a smaller total line capacitance. Tapering a line reduces the coupling capacitance between the signal line and the adjacent ground lines, and, consequently, the total capacitance of the signal line. Although the line capacitance is reduced, the line resistance is greater, thereby maintaining approximately the same signal characteristics. A reduction in the line capacitance decreases the dynamic power while an increase in the line resistance decreases the inductive behavior of the interconnect.

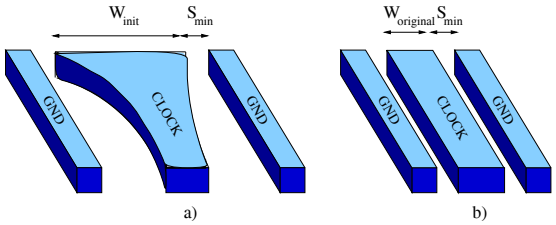

Figure 2: Coplanar clock line a) exponential tapering b) uniform (no tapering)

An exponentially tapered RLC interconnect line is described in [1]. Due to practical limitations, the line is divided into equal length sections. A first order approximation of the transfer function of each line section is used to characterize the signal. As described in section 3, the line becomes less inductive with tapering, since the line resistance increases. A first order approximation is adequate to characterize the time constant of each line section. Additional savings in power can be achieved with the cost of greater computational com-

plexity if a higher order approximation is used. If the RC time constants are maintained in both shaping techniques (exponential and uniform), the signal characteristics (propagation delay and transition time) remain the same. In order to maintain the same signal characteristics with exponential tapering, the summation of the RC time constants of all of the sections along each branch of an H-tree is the same in both tapered and uniform lines.

The optimum tapering factor for minimum power satisfies

$$\sum_{i=1}^{N} R_{i-T}C_{i-T} \leq \sum_{i=1}^{N} R_{i-U}C_{i-U}, \qquad (1)$$

and consequently, achieves the minimum line capacitance, where R_{i-T} and R_{i-U} are the resistance of each section in a tapered and uniform line, respectively, C_{i-T} and C_{i-U} are the capacitance of each section in a tapered and uniform line, respectively, and N is the number of sections in each branch.

Two practical constraints limit the choice of the largest line width W_{init} and the optimum tapering factor p. These practical limits can be represented by

1. $W_{init} \leq W_{max}$, where W_{max} is the maximum wire width of a target technology.
2. $p \leq \frac{N}{l(N-1)} ln(\frac{W_{init}}{W_{min}})$, where W_{min} is the minimum wire width of a target technology and l is the length of the line segment.

These two constraints should be satisfied for a tapered line segment. W_{init} cannot be greater than the maximum wire width permitted by the technology. Alternatively, increasing p may result in a width at the far end of a line which may be smaller than the minimum available wire width. Additional considerations in the design of a tapered clock tree are discussed in section 3.

3. Design Issues in Exponentially Tapered H-Trees

Different issues that affect the design of an H-tree structured clock network are discussed in this section. In subsection 3.1, the effect of tapering on the signal characteristics of an H-tree is described. The area overhead of the interconnect network of an exponentially tapered tree is discussed in subsection 3.2. In subsection 3.3, skew reduction in an exponentially tapered H-tree network is discussed.

3.1. Signal Integrity

The line width of an interconnect within an H-tree is typically divided by two in a uniformly tapered tree to match the line impedance at the branch points as shown in Fig. 3a. In a uniformly tapered tree, the interconnect inductance often cannot be ignored, particularly at the source of the tree where the line is widest. Matching the impedance reduces reflections and improves signal integrity [2]. This characteristic is not maintained in exponential tapering.

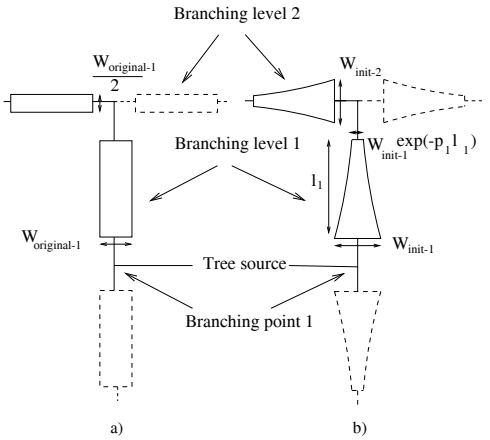

Figure 3: Interconnect in an H-tree a) uniform tapering b) exponential tapering

The branches of a tree are numbered according to the number of branch points (see Fig. 3). As shown in Fig. 3b, the initial width of the interconnect at each branch level W_{init-i} is chosen based on the constraints described in section 2. The tapering factor of each branch level p_i is determined by satisfying (1). All of the interconnects in the tree which belong to the same branch level have the same p_i and W_{init-i}.

With the criterion proposed in this paper, the impedance mismatch does not affect the signal integrity of the lines since the interconnect resistance is greater. The line resistance dominates the line impedance at the branch points, reducing the inductive behavior of the line. Alternatively, an increase in the line resistance does not affect the signal characteristics as the line capacitance decreases. Tapering also reduces the resistance at the source of the interconnect branch since the width is greater. A reduction in resistance at the source of the line compensates the signal degradation that occurs due to the increase in the line resistance at the far end of the line.

The inductive behavior of the line can be characterized by the damping factor of a line $\zeta = \frac{R_{line}}{2}\sqrt{\frac{C_{line}}{L_{line}}}$ [3], where R_{line}, C_{line}, and L_{line} are, respectively, the line resistance, capacitance, and inductance. The inductive behavior decreases as the damping factor increases, reducing the importance of matching the line impedance at the branch points. A mismatch in the branch points does not increase the reflections as illustrated in the simulation results presented in section 4. The difference between the first overshoot and undershoot $\Delta V_{over-under}$ at the driving point of the tree is treated as a metric characterizing the reflections in the tree.

3.2. Routing Area

In the proposed H-tree structure, the interconnects comprising the clock network are assumed to be shielded by two ground lines. Coplanar shielded structures are commonly used in industry, particularly in clock networks, to reduce

the effect of interconnect coupling with adjacent lines on the signal characteristics and minimize delay uncertainty of the clock signal [4]. In the proposed structure, the interconnect width at the near end is larger, reducing the space between the signal (or clock) line and the ground shield. The space is assumed to be minimum in the uniform structure shown in Fig. 2b. In order to maintain the space between the signal and ground shield, the space between the ground lines S_{large} is increased by the same amount as the increase in the initial width W_{init}, as shown in Fig. 4, where $S_{large} = \frac{W_{init} - W_{original}}{2} + S_{min}$.

For the same area overhead, the line capacitance is reduced by increasing the space between the ground shield lines without changing the signal (or clock) line width as shown in Fig. 4b. The capacitance (and therefore the dynamic power dissipation) of a line structure with wider spacing and a uniform interconnect width is greater than the capacitance of an exponentially tapered structure.

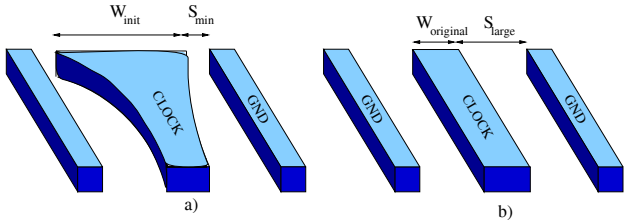

Figure 4: Coplanar clock line a) exponential tapering b) uniform line with wider spacing

Increasing the space between the ground shield and the signal lines, as shown in Fig. 4, achieves a smaller reduction in the line capacitance (and dynamic power) as compared to exponentially tapering the lines. Furthermore, a wider space between the ground lines increases the inductive characteristics of the lines. The area of the current return path is larger, increasing the line inductance. Furthermore, an increase in the spacing without a change in the interconnect width, as shown in Fig. 4b, maintains the same resistance as a uniform structure. An increase in the line inductance (without an increase in the resistance) increases the inductive behavior of the line. In section 4, a comparison between the proposed tapered structure and two alternative non-tapered structures is presented.

3.3. Skew Reduction

H-trees are primarily used in clock distribution networks. An important issue in the design of a clock distribution network is clock skew. Different techniques have been developed to minimize clock skew in trees with varying loads. These techniques can be classified into two categories; (1) techniques that employ active elements (dummy loads or inserted buffers), [2], and (2) techniques that passively change the tree structure (the interconnect width or length or the topology of the tree) [5].

An exponentially tapered tree structure can be integrated with active skew reduction techniques without changing the skew reduction phase of the design process. The active element, inserted along the tree to reduce the skew, can be placed in the same locations in a tapered tree. Alternatively, in passive techniques, a more complicated model should be used to optimize the tree for low power while simultaneously minimizing the skew.

4. Simulation Results

Different industrial H-tree structured clock distribution networks have been investigated to evaluate the proposed design technique. The optimum width W_{init-i} and tapering factor p_i for each branch level within each tree are determined. Closed form expressions for the line impedance parameters (resistance, capacitance, and inductance) are used to model the tree interconnect [1]. Each interconnect branch is divided into a number of sections with length $l_1 = 125\ \mu m$. l_1 is chosen to be greater than l_{min}, the shortest line in the tree. Two ground lines, with a 1 μm spacing, shield the tree interconnects. The minimum distance between the clock line and the ground shield S_{min} is 1 μm. Copper interconnect and low-k dielectric materials are assumed in evaluating the inductive properties of the lines.

A 64 sink clock tree covering a die area of 4.25 X 4.25 mm is modeled as a distributed RLC network to observe the signal characteristics. A symmetric capacitive load is assumed at all of the sinks (no clock skew among the sinks).

As listed in Table 1, different techniques are used to size the interconnect within the tree. The interconnect branch level is listed in the first column. The width of the uniform wires that achieves the minimum signal transition time at the loads of the tree is listed in the second column. In the third and fourth columns, the optimum initial width and tapering factor, respectively, of each branch level are listed. In order to compare the proposed structure with a uniform structure with the same area overhead, the spacing S_{min} is increased to S_{large} while maintaining the lines unshaped.

In Table 2, the signal characteristics (the propagation delay and transition time) and the transient power dissipated by a tree are listed for three interconnect structures. Exponential tapering and uniform tapering with a larger spacing maintain the same signal characteristics while dissipating less power. Exponential tapering, however, further reduces the power. A reduction in power dissipation of about 12% is achieved as compared to about 4.5% with no tapering.

A reduction in the inductive behavior of the line can be observed by a change in the damping factor of the lines within the tree. As listed in Table 1, the damping factor ζ of an exponentially tapered structure increases while the damping

Table 1: H-tree design techniques

Interconnect Branch Level	Uniform tapering	Exponential tapering			Uniform with larger spacing	
	$W_{original}$ (μm)	W_{init} (μm)	p (mm^{-1})	$\zeta/\zeta_{original}$	S_{large} (μm)	$\zeta/\zeta_{original}$
1	10.0	14.7	1.8	1.3	3.4	0.83
2	5.0	8.3	1.8	1.18	2.6	0.80
3	2.5	4.3	3.7	1.14	2.0	0.83
4	1.3	2.6	4.0	1.11	1.7	0.84
5	0.6	0.7	2.5	1.01	1.0	0.98
6	0.5	0.5	0	1.00	1.0	1.00

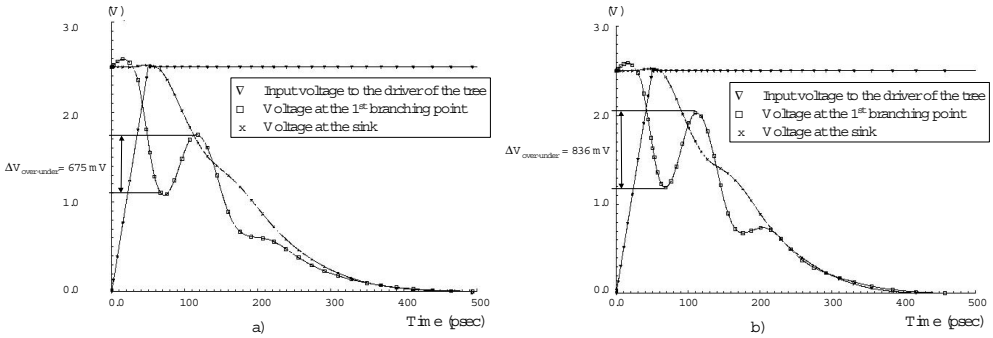

Figure 5: Waveforms at different nodes within the tree a) exponential tapering b) uniform tapering (with large spacing)

factor of a uniform (with wider spacing) structure decreases. An increase in the damping factor reduces the inductive behavior of the interconnects.

A 0.24 μm CMOS inverter is used to drive the tree. An input ramp signal with a 50 psec transition time is applied at the input of the driver of the tree. The signal waveform at three points; the input of the driver, the first branching point, and the sinks (or load) is shown in Fig. 5.

Note that the difference between the first overshoot and undershoot $\Delta V_{over-under}$ decreases from 683 mV to 675 mV at the first branching point of a tapered structure. Alternatively, the difference increases to 836 mV when a larger spacing is assumed without shaping the lines. Tapering the interconnects achieves a reduction in $\Delta V_{over-under}$ of approximately 20% with the same area overhead.

5. Conclusions

Exponentially tapered interconnect can reduce the dynamic power dissipation of a clock distribution network. A structure for sizing the interconnects within an H-tree network is proposed. The structure does not maintain a tapering factor of two in the line width at the branch points along the H-tree. The proposed technique reduces the power dissipation without affecting the signal characteristics. Exponentially tapered interconnects are shown to reduce the power dissipation of an industrial clock distribution network by up to 12% while maintaining the same signal transition times and propagation delay at the load. Furthermore, the inductive behavior of the interconnects is reduced, decreasing the inductive noise. Exponentially tapered interconnects also reduce by around 20% the difference between the signal overshoots at the input of a tree as compared to a uniform structure with the same area overhead.

Table 2: Signal characteristics and power dissipation of different H-tree clock distribution structures

Technique	t_{pd} (psec)	t_r (psec)	P_{total} (mW)
Uniform Tapering	149	227	5.18
Exponential Tapering	141	215	4.71
Uniform (larger spacing)	143	208	5.00

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