ENERGY EFFICIENT DUAL THRESHOLD VOLTAGE DYNAMIC CIRCUITS EMPLOYING SLEEP SWITCHES TO MINIMIZE SUBTHRESHOLD LEAKAGE

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Abstract **–** A sleep switch dual threshold voltage domino logic circuit technique for placing idle domino circuits into a low leakage state is proposed in this paper. The circuit technique reduces the leakage energy by up to 830 times as compared to a standard low threshold voltage domino logic circuit in a 0.18 µm CMOS technology. The sleep switch circuit technique significantly enhances the effectiveness of a dual threshold voltage CMOS technology to reduce subthreshold leakage current by strongly turning off all of the high threshold voltage transistors. The circuit technique reduces leakage energy by up to 714 times as compared to a standard dual threshold voltage domino logic circuit. A domino adder enters and leaves the low leakage sleep mode within a single clock cycle. The energy overhead of the circuit technique is low, justifying the activation of the proposed sleep scheme by producing a net savings in total power consumption during idle periods as short as 57 clock cycles.

1. INTRODUCTION

Subthreshold leakage power is soon expected to dominate the total power consumed by a CMOS circuit [1]-[5]. Circuit techniques aimed at lowering leakage currents are, therefore, highly desirable. A circuit technique is proposed in [4] for reducing the subthreshold leakage energy of domino logic circuits. This technique utilizes a combination of high and low threshold voltage transistors [4]. High threshold voltage (high-V_t) transistors are employed on the non-critical precharge paths. Alternatively, low threshold voltage (low-V_t) transistors are employed on the speed critical evaluation paths. Gating all of the inputs of the first stage domino circuits in a domino pipeline has been proposed to place the idle domino gates into a low leakage state [4].

The energy and delay overhead for entering and leaving the sleep mode, however, have not been addressed in [4]. Due to the additional gates at the inputs, significant dynamic switching energy is consumed to activate the sleep mode with the technique proposed in [4]. Furthermore, significant energy is dissipated to precharge all of the dynamic nodes while reactivating a domino logic circuit at the end of an idle period. In order to justify the use of additional circuitry to place a dual threshold voltage (dual-V_t) circuit into a low leakage state, the total energy consumed to enter and leave the standby mode must be significantly less than the savings in standby leakage energy. Gating all of the inputs of the first stage of a domino circuit in a domino pipeline also increases the circuit area and active mode power while degrading the circuit speed. A circuit technique with low delay and power overhead that places a dual-V_t domino logic circuit into a low leakage state is desirable.

A circuit technique employing sleep switch transistors for placing a dual-V_t domino logic circuit into a low leakage state is proposed in this paper. The circuit technique is based on the concepts presented in [3] and [5] for leakage current reduction in high speed dynamic circuits. An eight bit domino carry lookahead adder is evaluated based on the sleep switch circuit technique, assuming a 0.18 µm CMOS technology. The sleep switch circuit technique reduces the leakage energy by up to 830 times as compared to a standard low threshold voltage circuit.

The sleep switch dual-V_t circuit technique strongly turns off all of the high-V_t transistors; thereby, exploiting the full effectiveness of employing a dual-V_t CMOS technology to reduce subthreshold leakage current. The sleep switch circuit technique reduces the subthreshold leakage energy by up to 714 times as compared to a standard dual-V_t domino logic circuit. The energy overhead of the circuit technique is low, justifying the activation of the proposed sleep scheme by producing a net savings in total power consumption during idle periods as short as 57 clock cycles.

The operation of the sleep switch dual-V_t domino logic circuit technique is described in Section 2. Simulation results characterizing the standby leakage energy and active mode delay, power consumption, and noise immunity of the sleep switch technique as compared to standard dual-V_t and low-V_t domino logic circuits are presented in Section 3. Some conclusions are offered in Section 4.

2. DUAL THRESHOLD VOLTAGE DOMINO LOGIC EMPLOYING SLEEP SWITCHES

An implementation of the carry propagate function of a domino carry lookahead adder with low-V_t, standard dual-V_t, and sleep switch circuit techniques is shown in Fig. 1 (the high-V_t transistors are represented by a thick line in the channel region). A high-V_t NMOS sleep transistor is added to the dynamic node of a sleep switch dual-V_t domino logic circuit as shown in Fig. 1c. The operation of this transistor is controlled by a separate sleep signal. During the active mode of operation, the sleep signal is set low, cutting off the sleep switch, and the sleep switch circuit operates similar to a standard dual-V_t domino circuit. During the standby mode of operation, the clock signal is maintained high, turning off the high-V_t pull-up transistor of a domino gate. The sleep signal transitions high, turning on the sleep switch. The dynamic node of the domino gate is discharged through the sleep switch, turning off the high-V_t NMOS transistor within the output inverter. The output transitions high, cutting off the high-V_t keeper. After the node voltages settle to a steady state, all of the high-V_t transistors

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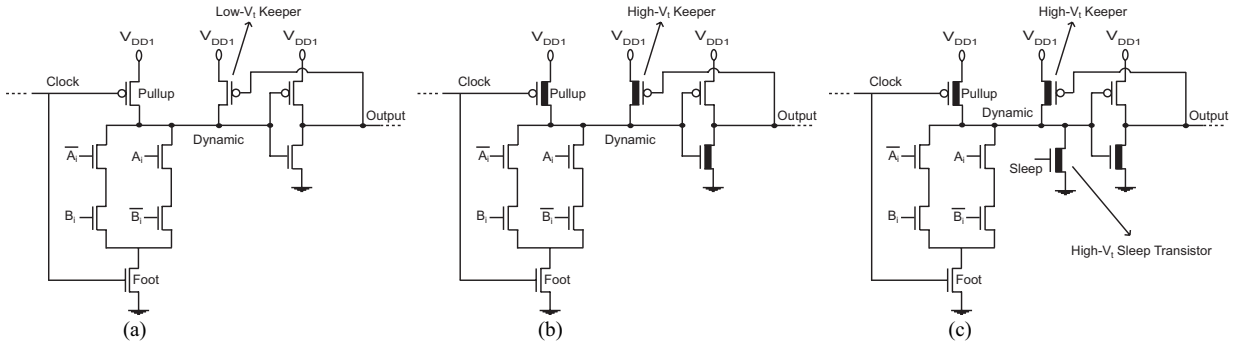

Fig. 1. Low-V_t, standard dual-V_t, and sleep switch domino cells for a carry lookahead adder. (a) Low-V_t domino carry propagate. (b) Standard dual-V_t domino carry propagate. (c) Sleep switch dual-V_t domino carry propagate.

in a sleep switch domino logic circuit are strongly cut-off, significantly reducing the subthreshold leakage current. Note that this technique, requiring no additional gating on the input signals while strongly turning off all of the high-V_t transistors within a single clock cycle, is significantly more power, delay, and area efficient as compared to the technique proposed in [4].

3. SIMULATION RESULTS

Eight input clock-delayed domino carry lookahead adders based on low-V_t, standard dual-V_t, and sleep switch circuit techniques are evaluated assuming a 0.18 µm CMOS technology ($V_{tnlow} = |V_{tplow}| = 200$ mV, $V_{tnhigh} = |V_{tphigh}| = 500$ mV, and T = 110°C). A 1 GHz clock with a 50% duty cycle is applied to the domino logic circuits. The block diagram of an eight bit clock-delayed domino carry lookahead adder based on the proposed sleep switch circuit technique is shown in Fig. 2.

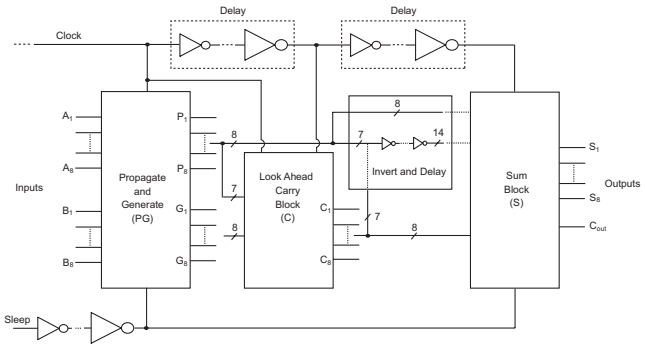

Fig. 2. Block diagram of a clock-delayed domino carry lookahead adder with the sleep switch circuit technique.

In the sleep switch adder, all of the propagate (P) and generate (G) domino gates have sleep switches. When the domino adder is idle, the dynamic nodes of P and G domino gates (in the first stage propagate and generate (PG) block) are discharged via the sleep switches. The domino gates within the lookahead carry (C) block do not have sleep switches. Following the output low-to-high transition of the P and G gates, the domino gates within the C block also evaluate and discharge in a domino fashion. Some of the signals originating from the PG and C blocks are inverted before being fed into the sum block (see Fig. 2). The domino logic circuits within the sum block, therefore, also require sleep switches in order to be placed into a low leakage state.

As listed in Table 1, the leakage current characteristics of the circuits are evaluated for six input vectors, V_0 to V_5. C_{out} (S_8) is evaluated through the critical path of the carry chain within the carry block for V_2 (V_3). The delay and active mode power are calculated for V_2 and V_3. During evaluation of the noise immunity, the same noise signal is coupled to all of the inputs of a domino logic circuit as this situation represents the worst case noise condition.

TABLE 1. INPUT VECTORS APPLIED TO AN ADDER

	V_0	V_1	V_2	V_3	V_4	V_5
A	0	0	1	1	255	255
B	0	255	255	127	255	0

The standby leakage current characteristics of the sleep switch circuit technique is presented in Section 3.1. The active mode delay, power consumption, and noise immunity characteristics of the circuit technique are discussed in Section 3.2. The sleep/wake-up delay and energy overhead of the sleep switch circuit technique are presented in Section 3.3.

3.1. Reduction in Subthreshold Leakage Energy

The leakage energy consumption (per clock cycle) of low-V_t, standard dual-V_t, and sleep switch adders is shown in Fig. 3. The leakage energy of a standard dual-V_t circuit is reduced by 1.2 X to 2.8 X as compared to a low-V_t circuit. In a standard domino circuit, the standby leakage energy is dependent on the input vector applied to the circuit after the clock signal is gated high [2]. The dynamic nodes of all of the domino logic circuits are precharged when the clock is low. After the clock transitions high, a portion of these domino gates discharges, provided that a necessary input combination to discharge the dynamic node is applied. For V_0, the dynamic nodes of all of the domino logic gates of a standard dual-V_t adder are maintained high after the clock is gated. This condition is typically the highest leakage state for a dual-V_t domino logic circuit since all of the high-V_t transistors (other than the pull-up transistors) operate in the strong inversion region [2]. The V_0 vector, therefore, produces the maximum leakage current in a standard dual-V_t adder.

As shown in Fig. 3, the sleep switch circuit technique reduces the leakage energy as compared to both the low-V_t and standard dual-V_t circuits for all of the input vectors. The sleep switch circuit technique lowers the total leakage energy by 461 X to 830 X as compared to a low-V_t adder. The proposed circuit technique strongly cuts off all of the high-V_t transistors; thereby exploiting

the full effectiveness of employing dual-V_t transistors to reduce subthreshold leakage current. An adder with the sleep switch circuit technique consumes 167 X to 714 X less leakage energy as compared to a standard dual-V_t adder.

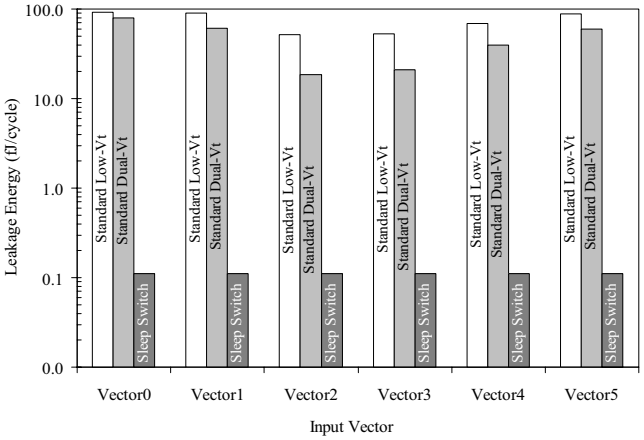

Fig. 3. Comparison of the leakage energy (per cycle) of the adder circuits with the low-V_t, standard dual-V_t, and sleep switch circuit techniques for six different input vectors.

3.2. Delay and Power Reduction in the Active Mode

The active mode delay, power consumption, and power delay product (PDP) of low-V_t, standard dual-V_t, and sleep switch adders are shown in Fig. 4. The proposed circuit technique enhances circuit speed by 12% and 21% for V_2 and V_3, respectively, as compared to a low-V_t adder. The sleep switch circuit technique also reduces the active mode power consumption. The power consumption is reduced by 14.4% and 14.6% for the input vectors V_2 and V_3, respectively, as compared to a low-V_t adder. The savings in the active mode power consumption and delay is primarily due to reduced contention current [1] of the high-V_t keeper transistors in a dual-V_t domino logic circuit (see Figs. 1b and 1c). The reduced power consumption in the dual-V_t delay elements is another factor that lowers the active mode power. The delay and power characteristics of a standard dual-V_t adder are similar to a sleep switch adder.

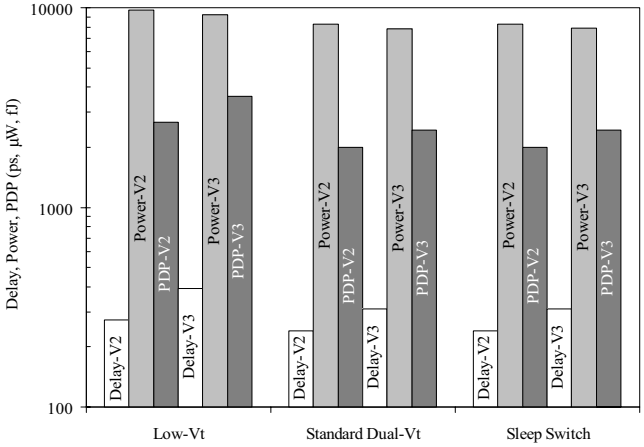

Fig. 4. Comparison of the delay, power, and power delay product (PDP) of the adder circuits with the low-V_t, standard dual-V_t, and sleep switch circuit techniques for the V_2 and V_3 input vectors.

The current supplied by a high-V_t keeper transistor to preserve the state of a dynamic node is reduced, thereby degrading the noise immunity as compared to a low-V_t circuit operating in the active mode [2]. The average degradation in noise immunity for the P, G, C, and sum (S) domino logic gates are listed in Table 2. The degradation in noise immunity of the sleep switch domino adder varies between 11.3% and 14.9% for different circuit blocks as compared to the low-V_t adder.

TABLE 2. DEGRADATION IN NOISE IMMUNITY OF SLEEP SWITCH ADDER AS COMPARED TO LOW-V_t ADDER

	P	G	C	S
Average Reduction in Noise Immunity	12.2%	14.9%	12.9%	11.3%

3.3. Sleep/Wake-up Delay and Energy Overhead of the Sleep Switch Circuit Technique

When a domino logic circuit is idle, the clock is gated high. The sleep signal should be applied after the low-to-high edge of the clock signal propagates to the gates in the last stage of a clock-delayed domino logic circuit. Activating the sleep switches after the low-to-high transition of the clock ensures that no short-circuit power is consumed while entering the sleep mode. Following the activation of the sleep switches, all of the domino gates are forced to a low dynamic node voltage state. After the node voltages settle, all of the high-V_t transistors are strongly cut off, thereby minimizing the subthreshold leakage currents with the proposed sleep switch circuit technique. Depending upon the input vector, from 829 ps to 850 ps is required (after the clock is gated) for the sleep switch adder to be placed into a low leakage state. Before the end of an idle mode, the sleep signal transitions low, cutting off all of the sleep switches. The clock is reactivated and all of the dynamic nodes are recharged to activate a sleeping domino logic circuit. The duration of reactivation is equal to the precharge time of a domino circuit. An adder circuit, therefore, enters and leaves the standby mode within a single clock cycle with the proposed circuit technique.

The energy overhead for implementing the standby mode with the sleep switch circuit technique is also evaluated. Activating the sleep switches to place a domino logic circuit into standby mode requires a specific amount of energy. All of the dynamic nodes in a domino circuit are discharged during the standby mode with the sleep switch circuit technique. Additional energy is dissipated at the end of an idle period while disabling the sleep switches and precharging the dynamic nodes in order to reactivate a domino logic circuit. In order to justify the activation of the proposed sleep switches to place a dual-V_t circuit in a low leakage state, the total energy consumed to enter and leave the sleep mode must be less than the savings in standby leakage energy.

The cumulative energy dissipated in the standby mode by the low-V_t and sleep switch adders is shown in Fig. 5. The energy of a low-V_t domino circuit is only affected by the leakage current during the standby mode. Alternatively, both the leakage energy and the energy overhead of entering and leaving the sleep mode are included in the cumulative energy characteristics of the sleep switch adder. The total energy overhead of the proposed technique is included as an energy step in the first cycle of the standby mode (see Figs. 5 and 6). Similar to the low-V_t and standard dual-V_t energy characteristics, after the first clock cycle, the sleep switch energy is only due to the subthreshold leakage current. A specific amount of time in the idle mode, dependent upon the input vector,

is necessary for the cumulative leakage energy of a low-V_t circuit to exceed the cumulative energy of a sleep switch circuit.

The intersection of the sleep switch and low-V_t cumulative energy characteristics determine the necessary minimum duration of the sleep mode of operation such that the sleep switch circuit technique offers a net savings in energy as compared to a low-V_t circuit. As shown in Fig. 5, the cumulative energy of the low-V_t and sleep switch circuits exhibit different behavior depending upon the input vector applied during the standby mode. The leakage energy of the low-V_t adder is smallest for V_2 and highest for V_0. Alternatively, the leakage energy of a sleep switch adder is virtually independent of the input vectors. Depending upon the input vector, the relative energy overhead of the proposed scheme changes. For V_0, none of the dynamic nodes of a low-V_t circuit are discharged during the standby mode. Alternatively, all of the dynamic nodes are discharged in a sleep switch circuit. The relative reactivation energy overhead of the sleep switch circuit technique is, therefore, highest for V_0. As shown in Fig. 5, a minimum of 42 clock cycles is required for the sleep switch circuit technique to provide a net savings in energy as compared to a low-V_t circuit operating in the standby mode.

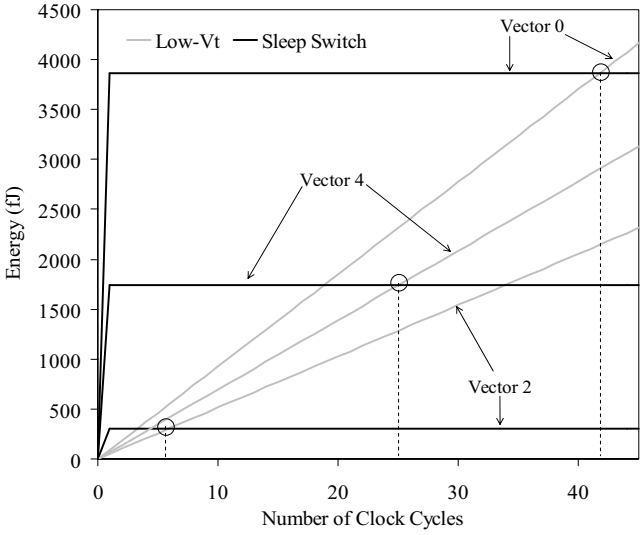

Fig. 5. Cumulative standby energy dissipation of low-V_t and sleep switch adders for three different input vectors.

The cumulative standby mode energy dissipation of the sleep switch and standard dual-V_t adders is shown in Fig. 6. V_0 and V_2 cause the highest and lowest, respectively, leakage states in a standard dual-V_t circuit. No input vector exists that can place a standard dual-V_t adder into a lower leakage state as compared to a sleep switch adder. Circuit techniques based on the application of a selected input vector to place a circuit into a low leakage state (such as the technique proposed in [4]) are, therefore, ineffective in decreasing the subthreshold leakage current of the domino adder discussed in this paper.

As shown in Fig. 6, a minimum of 57 clock cycles is required for the sleep switch circuit technique to provide a net savings in energy as compared to a standard dual-V_t circuit operating in the standby mode. Although the leakage energy of the standard dual-V_t domino adder is 167 X to 714 X higher as compared to the sleep switch adder, a standard dual-V_t circuit technique is preferable in applications with idle periods shorter than 57 clock cycles.

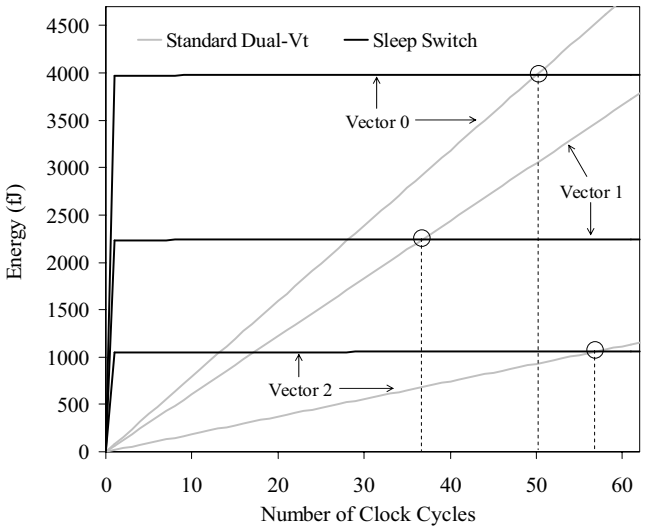

Fig. 6. Cumulative standby energy dissipation of the standard dual-V_t and sleep switch adders for three different input vectors.

4. CONCLUSIONS

A circuit technique is proposed for reducing the standby leakage energy of domino logic circuits. The circuit technique employs sleep switch transistors for placing a dual threshold voltage domino logic circuit into a low leakage state. A dual threshold voltage domino adder enters and leaves the low leakage sleep mode within a single clock cycle with the sleep switch circuit technique.

The sleep switch circuit technique reduces the leakage energy by up to 830 times as compared to a standard low-V_t circuit, assuming a 0.18 µm CMOS technology. The circuit technique also reduces the active mode delay and power by up to 21% and 14.6%, respectively, as compared to a low-V_t circuit.

The sleep switch circuit technique strongly turns off all of the high-V_t transistors; thereby exploiting the full effectiveness of a dual-V_t CMOS technology to reduce subthreshold leakage current. The sleep switch circuit technique reduces leakage energy by up to 714 times as compared to a standard dual-V_t circuit. The energy overhead of the circuit technique is low, justifying the activation of the proposed sleep scheme by producing a net savings in total power consumption during idle periods as short as 57 clock cycles.

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