# A Low Power Thyristor-Based CMOS Programmable Delay Element

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***Abstract*— A delay element insensitive to power supply and temperature variations become important as circuit speeds increase. A delay element, based on a CMOS thyristor, is proposed in this paper. This thyristor uses current rather than voltage to control the delay, exhibiting a low power supply noise sensitivity of 9.43% and a temperature variation sensitivity of 314 PPM/°C. A technique to cancel the charge sharing effect during switching is incorporated into the delay element to further enhance power supply insensitivity. The delay element is combined with a bandgap reference voltage generator to produce a digitally controlled variable delay line. Simulation results show that the proposed delay element has a lower power supply and temperature sensitivity than a classical chain of inverters. The power consumed by the proposed delay element is lower than an inverter chain, and is much lower than a differential delay element.**

## I. Introduction

DELAY elements are widely used to manipulate timing in both digital and analog circuits. A delay buffer is often inserted between flip flops to satisfy setup and hold time requirements in digital systems. A self-timed dynamic logic family, such as clock-delayed domino logic, uses a delay element to match the propagation time of the clock to that of the signal. A delay locked loop (DLL) in an analog system uses a voltage controlled delay line (VCDL) for clock synchronization. In switched-capacitor circuits, a delay element is used to generate non-overlapping clock.

The requirement for increasing circuit speed creates a need for a small value delay element with less jitter. A mechanism to reject power supply noise and delay uncertainty due to external temperature variations, therefore, should also be considered in the design of a delay element.

An inverter chain, as shown in Fig. 1, is the most common circuit architecture for a delay element due to the simplicity and low power consumption. An inverter chain, however, requires multiple inverter stages to produce a large delay. The delay of an inverter is inversely proportional to the power supply ($t_d \propto 1/V_{dd}$) and is sensitive to power supply noise. Furthermore, the delay of an inverter chain is sensitive to temperature variations. Other versions of delay elements based on an inverter, such as a current-starved inverter [1] and capacitor-loaded inverter, adds functionality to control the delay value by the voltage, but the power supply noise and temperature sensitivities are degraded as compared to a simple chain of inverters.

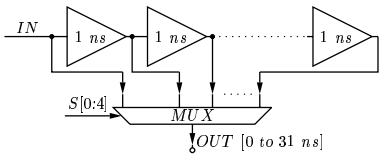



Fig. 1. Variable delay line based on an inverter chain

A differential delay element [2] produces a delay value with less jitter and smaller power supply and temperature variations by using feedback. The feedback circuit, however, requires an OPAMP to generate the bias voltage, increasing the complexity of the delay element and making it more difficult to implement in a low voltage application. A differential delay element consumes static power since the transistors conduct all of the time. The more stages in the delay line, the higher the power consumption, making it impractical to implement a large delay using differential delay elements.

A thyristor is commonly used in high voltage power electronics to switch large amounts of power using a small triggering current. A thyristor usually has three electrodes: an anode, a cathode, and a gate (the control electrode). When the cathode is negatively charged relative to the anode, no current flows until a pulse is applied to the gate. With the arrival of a pulse, the thyristor begins to conduct, and continues to conduct until the voltage between the cathode and anode is reversed or reduced below a certain threshold value.

A thyristor can be used as a delay element in CMOS technologies [3]. Since the delay is controlled by current rather than by voltage, a thyristor-based delay element exhibits high power supply noise rejection and is insensitive to temperature variations. Furthermore, a thyristor-based CMOS delay element consumes less power since the transistors conduct only at the time of switching and do not dissipate static power. A thyristor-based circuit architecture of a delay element is described in [3]. This circuit, however, has a charge sharing problem. Furthermore, any mismatch between the two current sources in this circuit leads to a change in the pulse width of the clock.

Based on a CMOS thyristor, a circuit architecture of a delay element with a charge sharing cancellation technique is proposed and described in this paper. The principle operation of a CMOS thyristor is explained in Section II, followed by a review of the proposed architecture of the delay element and the technique to cancel charge sharing effects. In Section III, a digitally controlled variable delay line based on the proposed circuit is described, and the results of post-layout simulation are presented, followed by a comparison with an inverter chain. Some conclusions are offered in Section IV.

## II. Circuit Architecture of CMOS Thyristor Delay Element

The circuit architecture of a CMOS thyristor is shown in Fig. 2 [3], where $C_1$ and $C_2$ are parasitic capacitances. The operation of this circuit is similar to the operation of a three terminal thyristor device used in high voltage power electronics. If node $\overline{Q}$ is precharged to $V_{dd}$, node $Q$ is discharged to ground, and pass transistors $M_3$ and $M_4$ are on. When the clock $CLK$ transitions high, node $\overline{Q}$ begins to discharge with current $I_{ctrl}$. Once the voltage at node $\overline{Q}$ drops below the threshold voltage, transistor $M_1$ turns on, and node $Q$ is charged through $M_1$. When node $Q$ is charged to the threshold voltage $V_{tn}$, transistor $M_2$ turns on. Transistors $M_1$ and $M_2$ produce a positive feedback, which quickly flips the state of the thyristor, pulling down node $\overline{Q}$ to ground and charging node $Q$ to $V_{dd}$. The rising edge of the signal at node $Q$ can be viewed as a delayed version of the rising edge of the clock $CLK$. Note that during the operation of a CMOS thyristor, no current conducts directly from the power supply to ground, and therefore no static power is consumed.

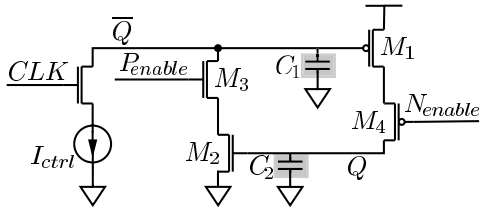



Fig. 2. Circuit architecture of a CMOS thyristor

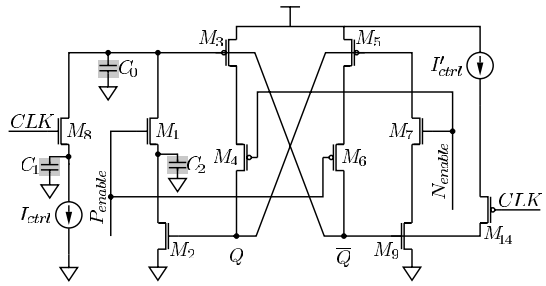



Fig. 3. CMOS thyristor delay element originally described in [3]

The time required to discharge node $\overline{Q}$ from $V_{dd}$ to $V_{dd} - V_{tp}$ by current source $I_{ctrl}$ is

$$t_{d1} = \frac{C_1 V_{tp}}{I_{ctrl}} . \tag{1}$$

Once node $\overline{Q}$ drops to $V_{dd} - V_{tp}$, transistor $M_1$ turns on and operates in the saturation region, and the drain current $I_{d1}$ is

$$V_{gs1} = |V_{\overline{Q}} - V_{dd}| = V_{tp} + \frac{I_{ctrl} t}{C_1} , \tag{2}$$

$$I_{d1} = \frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{gs1} - V_{tp})^2 , \tag{3}$$

$$= \frac{\mu_p C_{ox}}{2} \frac{W}{L} \frac{I_{ctrl}^2 t^2}{C_1^2} . \tag{4}$$

The time $t_{d2}$ required to charge node $Q$ from ground to $V_{tn}$ by drain current $I_{d1}$ satisfies

$$\int_0^{t_{d2}} I_{d1}\, dt = V_{tn} C_2 , \tag{5}$$

$$t_{d2} = \sqrt[3]{\frac{6 C_1^2 C_2}{\kappa I_{ctrl}^2} V_{tn}} , \tag{6}$$

where

$$\kappa = \mu_p C_{ox} \frac{W}{L} . \tag{7}$$

Combining (1) and (6), the delay of a CMOS thyristor is

$$t_d = \frac{C_1 V_{tp}}{I_{ctrl}} + \sqrt[3]{\frac{6 C_1^2 C_2}{\kappa I_{ctrl}^2} V_{tn}} + \delta t , \tag{8}$$

where $\delta t$ is the regeneration time for the positive feedback of a CMOS thyristor. Since only $\delta t$ is affected by the power supply, and the major delay components ($t_{d1}$ and $t_{d2}$) are independent of $V_{dd}$, the delay element is fairly insensitive to power supply variations. The delay of a CMOS thyristor, therefore, is controlled by the current source $I_{ctrl}$ rather than by the power supply voltage.

The CMOS thyristor shown in Fig. 2 can only flip once, *i.e.*, only the rising edge of the clock is delayed. To delay the falling edge of the clock, a complementary CMOS thyristor can be used. The complete delay element, as described in [3], is composed of two complementary CMOS thyristors, as shown in Fig. 3. This circuit, however, suffers from charge sharing. The voltage at node $\overline{Q}$ before it is discharged by the current source $I_{ctrl}$ is assumed to be at the power supply $V_{dd}$. At the rising edge of clock $CLK$ and signal $P_{enable}$, the charge stored on the parasitic capacitance $C_0$ is shared with the parasitic capacitances $C_1$ and $C_2$. Because the parasitic capacitances $C_1$ and $C_2$ are connected to ground, the voltage at node $\overline{Q}$ changes from $V_{dd}$ to

$$V_{\overline{Q}} = V_{dd} \frac{C_0}{C_0 + C_1 + C_2} . \tag{9}$$

The amount of delay, therefore, is reduced due to the charge sharing effect.

Additionally, the delay circuit shown in Fig. 3 could change the pulse width of the clock due to mismatches between the two current sources. The two current sources $I_{ctrl}$ and $I'_{ctrl}$ are not identical because the current source is mirrored through two stages of a current mirror. The delay of the rising and falling edges of the clock are controlled, respectively, by the two complementary CMOS thyristors. The delay of the two complementary thyristors are controlled, respectively, by the current source $I_{ctrl}$ and $I'_{ctrl}$. Different values of $I_{ctrl}$ and $I'_{ctrl}$ make the delay of the rising edge of the clock different from the delay of the falling edge of the clock. The pulse width of the clock, therefore, changes at the output of the delay element.

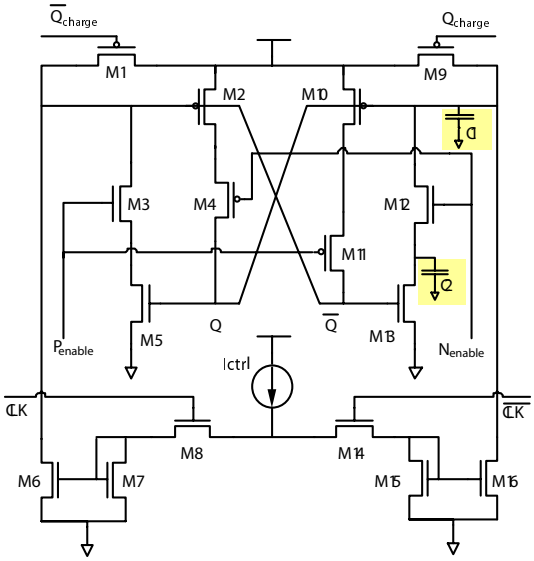
The circuit architecture shown in Fig. 4(a) is proposed to cancel the charge sharing effect. The timing signal is shown in Fig. 4(b), where the signal $N_{enable}$ is produced by delaying signal Q with delay time $t'_d$. The signal $P_{enable}$ is an inverse of signal $N_{enable}$. $t'_d$ is chosen to be larger than the regeneration time $\delta$t, and the variation of $t'_d$ from the power supply noise does not affect the delay of the CMOS thyristor. Signals $\overline{Q}_{charge}$ and $Q_{charge}$ are introduced to cancel the charge sharing effect. Signal $\overline{Q}_{charge}$ is generated by a NAND gate with inputs $\overline{CLK}$ and $P_{enable}$. Signal $Q_{charge}$ is generated by a NAND gate with inputs $CLK$ and $N_{enable}$.

If node $\overline{Q}$ is assumed high, and transistors $M_3$ and $M_4$ are on, $M_1$ is off, enabling the left thyristor and disabling the right thyristor. At the rising edge of the clock $CLK$, transistor $M_8$ turns on, node $\overline{Q}$ begins to discharge with current $I_{ctrl}$, and the left thyristor begins to flip. After a delay time $t_d$, the left thyristor regenerates, pulling down node $\overline{Q}$ to ground and charging node $Q$ to $V_{dd}$. The rising edge of the clock, therefore, is delayed by $t_d$.

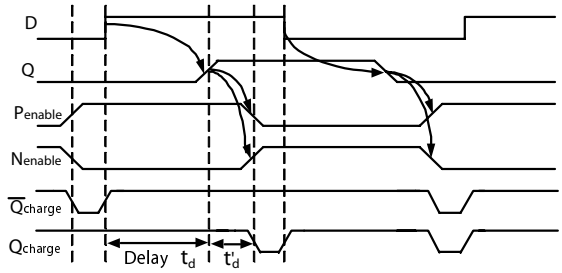
Signal $N_{enable}$ is a delayed version of signal $Q$, which changes to $V_{dd}$ after a delay time $t'_d$. Signal $P_{enable}$ also changes to ground, disabling the left thyristor and enabling the right thyristor. At the falling edge of the clock $CLK$, signal $Q_{charge}$ turns $M_9$ off, the right thyristor begins to flip, delaying the falling edge of the clock. The output nodes $Q$ and $\overline{Q}$ are further shaped by the inverter load. Note that the output node $Q$ is the delayed version of the clock.

When $M_{12}$ is turned on by signal $N_{enable}$, charge sharing occurs between the parasitic capacitances $C_1$ and $C_2$, pulling down the voltage at node $Q$ from $V_{dd}$ to $\frac{C_1}{C_1+C_2} V_{dd}$. When signal $Q_{charge}$ turns on transistor $M_9$, the voltage at node $Q$ is charged to $V_{dd}$, canceling the charge sharing effect. Furthermore, only one current source is used in the circuit, eliminating the issue of mismatch between $I_{ctrl}$ and $I'_{ctrl}$. The clock switches $M_8$ and $M_{14}$ in the original circuit, as shown in Fig. 3, are between the current sources and nodes $\overline{Q}$ and $Q$, respectively. When the clock is switched on, charge sharing occurs between the parasitic capacitances $C_0$ and $C_1$ shown in Fig. 3. In the proposed circuit shown in Fig. 4(a), the

clock switches $M_8$ and $M_{14}$ are placed away from nodes $\overline{Q}$ and $Q$, eliminating the problem of charge sharing.




(a) Proposed circuit architecture of a CMOS delay element




(b) Timing diagram of control signals

Fig. 4. Proposed circuit architecture of a CMOS thyristor delay element and related timing diagram

## III. Results and Analysis

Based on the proposed circuit architecture shown in Fig. 4(a), three CMOS thyristor delay elements of 4 ns, 8 ns, and 16 ns have been designed and implemented in a 0.35 $\mu$m CMOS process. Furthermore, a digitally controlled variable delay line ranging from 0 ns to 31 ns with a step size of 1 ns has also been developed, as shown in Fig. 5, where $S[0\text{-}5]$ are the digital control signals. When the delay value is small, the major delay component in a CMOS thyristor, as shown in (8), is the regeneration time $\delta t$. The power supply noise rejection (PSR) in this circuit is about the same as an inverter chain. Delay values of 1 ns to 3 ns, therefore, should be based on an inverter chain. Since the delay of a CMOS thyristor is controlled by a current source, an on-chip bandgap voltage reference [4] is used to provide a constant current source. The bandgap voltage reference is insensitive to power supply noise and temperature variations. The layout of the variable delay line is shown in Fig. 6.

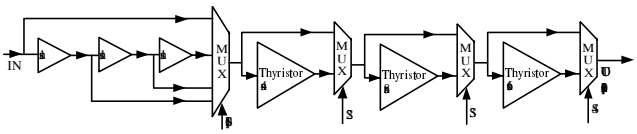



Fig. 5. Circuit diagram of a variable delay line based on a CMOS thyristor. Note that the delay circuit can vary from 0 ns to 31 ns with a step size of 1 ns.

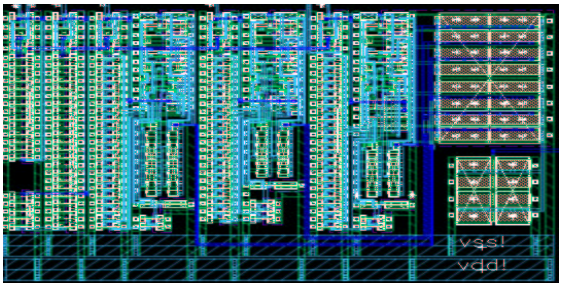



Fig. 6. Layout of the variable delay line based on a CMOS thyristor

To compare the delay characteristics of the proposed CMOS thyristor with an inverter chain, the sensitivity of the delay to the power supply noise is defined as

$$S_V \equiv \frac{\Delta t_d / t_d}{\Delta V_{dd} / V_{dd}} . \tag{10}$$

Similarly, the sensitivity of the delay to temperature variations is defined as

$$S_T \equiv \frac{1}{t_d} \frac{\Delta t_d}{\Delta T} . \tag{11}$$

The smaller the value of $S_V$ and $S_T$, the less variation of the delay to the power supply noise and temperature variations, respectively.

Delay variations due to the power supply noise are compared in Fig. 7 for the inverter chain and three CMOS thyristor delay elements, where the power supply is varied $\pm 0.3$ volts from a nominal value of 3.3 volts. To compare the variation of the delay elements with different delay values, the delay is normalized to the delay value at a nominal power supply ($V_{dd} = 3.3$ volts). The delay variation of the CMOS thyristor delay elements are much smaller than those of the inverter chain with the same power supply noise, as shown in Fig. 7. The 16 ns CMOS thyristor delay element is preferable since the per cent change in delay caused by a change in the regeneration time $\delta t$, which is the delay component affected by the power supply, is the smallest among all of the delay elements. Delay variations due to temperature changes are compared in Fig. 8, where the temperature is varied from 0°C to 65°C, and the delay is normalized to the nominal delay at 25°C. Delay variations of the CMOS thyristors are smaller than those of inverter chains with the same temperature variation. The sensitivity to power supply noise and temperature variations for the inverter chain and the CMOS thyristors are summarized in Table I. The power consumed by the CMOS thyristors is also smaller than the inverter chains because CMOS thyristors do not consume static power and have fewer stages than an inverter chain.

The digitally controlled variable delay line (0-31 ns) is compared to the inverter chain in Figs. 9 and 10 for sensitivities to power supply noise and temperature variations, respectively. Since the delay of an inverter chain is inversely proportional to the power supply ($t_d \propto S[0\text{-}5]/V_{dd}$), the sensitivity to the power supply noise $S_V$

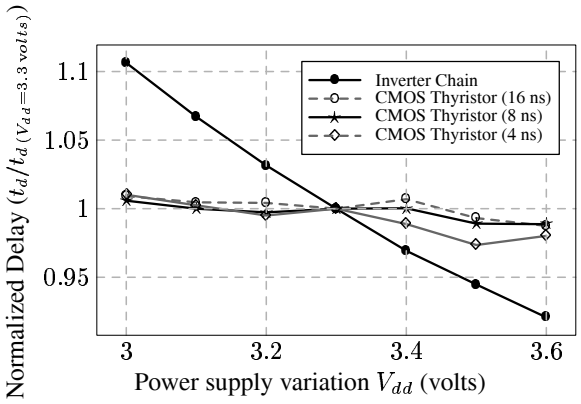



Fig. 7. Comparison of delay variation to the power supply noise for the inverter chain and CMOS thyristors ($t_d/t_{d\,(V_{dd}=3.3\,volts)}$)

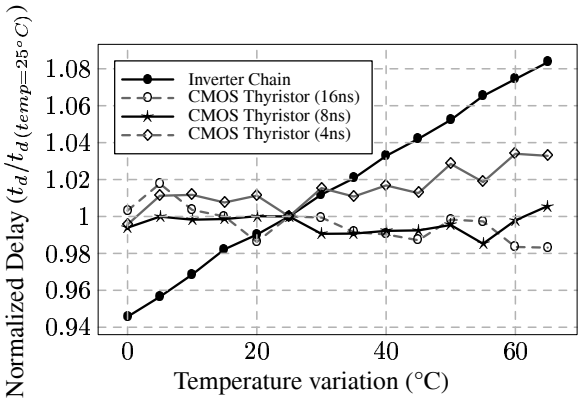



Fig. 8. Delay variation with temperature ($t_d/t_{d\,(temp=25^\circ C)}$)

is constant for all control signals $S$[0-4]. Similarly, the sensitivity to temperature variations $S_T$ is also constant for all control signals $S$[0-4]. When the delay value is larger than 3 ns, for the CMOS thyristor delay elements, the power supply noise sensitivity $S_V$ and temperature variation sensitivity $S_T$ of the proposed variable delay line are much smaller than those of an inverter chain. The power dissipated by the proposed variable delay line is 890 $\mu$W, much less than the 1122 $\mu$W dissipated by the inverter chain.

## IV. Conclusions

A circuit architecture for a delay element based on a CMOS thyristor which cancels the charge sharing effect is proposed in this paper. Using current rather than voltage to control the delay, the delay element exhibits a low power supply noise sensitivity of 9.43% and a low temperature variation sensitivity of 314 PPM/°C. Based on CMOS thyristor delay elements and a bandgap voltage reference generator, a digitally controlled variable delay line capable of varying from 0 ns to 31 ns with a step size of 1 ns has been developed and the layout implemented. Post-layout simulation results show that the thyristor-based variable delay line has a much higher power supply noise rejection and lower temperature variation sensitivity than an inverter chain. The power consumption of the variable delay line is also less than that of the inverter chain, and much less than differential delay elements.

TABLE I
Comparison of delay variation to power supply noise and temperature variations for inverter chain and CMOS thyristor

| | $S_V$ | $S_T$ ($PPM/^\circ$C) | Power ($\mu W$) |
|---|---|---|---|
| Inverter Chain (0-31 ns) | 102.10% | 1970 | 1122 |
| CMOS Thyristor (16 ns) | 11.94% | 517 | 310 |
| CMOS Thyristor (8 ns) | 9.43% | 314 | 208 |
| CMOS Thyristor (4 ns) | 20.16% | 590 | 197 |

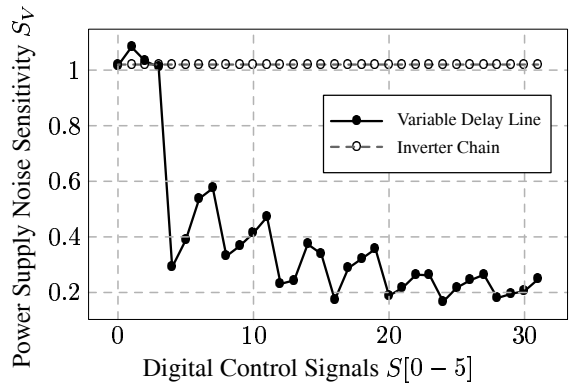



Fig. 9. Sensitivity of thyristor-based variable delay line (0 to 31 ns) to power supply noise $S_V$ and comparison with an inverter chain

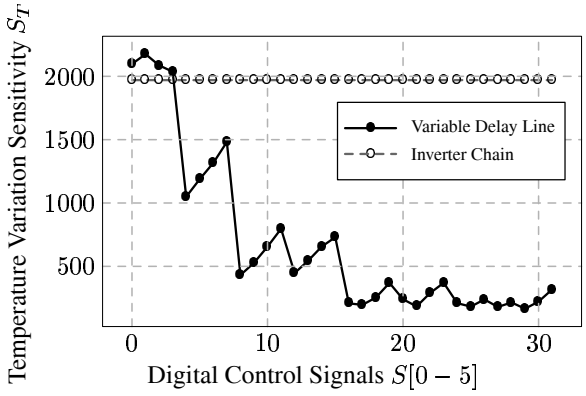



Fig. 10. Sensitivity of thyristor-based variable delay line (0 to 31 ns) to temperature variations $S_T$ and comparison with an inverter chain

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