CASCODE BUFFER FOR MONOLITHIC VOLTAGE CONVERSION OPERATING AT HIGH INPUT SUPPLY VOLTAGES

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ABSTRACT

A high-to-low switching DC-DC converter that operates at input supply voltages up to two times as high as the maximum voltage permitted in a nanometer CMOS technology is proposed in this paper. The circuit technique is based on a cascode bridge that maintains the steady-state voltage differences among the terminals of all of the transistors within a range imposed by a specific fabrication technology. The proposed circuit technique permits the full integration of active and passive devices of a switching DC-DC converter with a high voltage conversion ratio in a standard low voltage CMOS process. An efficiency of 87.8% is achieved for 3.6 volts to 0.9 volts conversion assuming a 0.18 μm CMOS technology. The DC-DC converter operates at a switching frequency of 97 MHz while supplying a DC current of 250 mA to the load.

1. INTRODUCTION

Voltages significantly higher than current board level voltages will become necessary to efficiently deliver significantly greater levels of power to future high performance integrated circuits [1]. Distributing power at a higher voltage reduces the supply current of an integrated circuit. At a reduced supply current, resistive voltage drops and parasitic power dissipation of the off-chip power distribution network is reduced, thereby enhancing the energy efficiency and quality of the distributed voltage [1]-[3]. Once the required energy reaches the input pads of a microprocessor, the lower supply voltage of the microprocessor circuitry can be generated by a monolithic DC-DC converter on the same die as the microprocessor, as shown in Fig. 1.

Monolithic DC-DC conversion on the same die as the load provides several desirable aspects [1], [2]. In a typical non-integrated switching DC-DC converter (as shown in Fig. 2), significant energy is dissipated in the parasitic impedances of the circuit board interconnect and among the discrete components of the regulator [1], [2]. As microprocessor current demands increase, the energy losses of the off-chip power generation increase, further degrading the efficiency of a discrete DC-DC converter. Integrating both the active and passive devices of a DC-DC converter onto the same die as a microprocessor improves energy efficiency, enhances the quality of the voltage regulation, decreases the number of I/O pads dedicated for power delivery on the microprocessor die, and reduces the cost of fabrication and area of the DC-DC converter [1], [2], [5].

Because of the advantages of a high voltage power delivery on a circuit board and monolithic DC-DC conversion, next generation low voltage and high power microprocessors are likely to require high input voltage large-step-down DC-DC converters monolithicly integrated onto the same die. Operating voltages of standard non-isolated switching DC-DC converters are, however, limited due to MOSFET reliability issues. In a standard buck converter circuit as shown in Fig. 2, the input voltage V_{DD1} is limited to less than or equal to the maximum voltage that is allowed to be directly applied across the terminals of a MOSFET, V_{max}, which is specific to a particular fabrication technology. Provided that a DC-DC converter is integrated onto the same die as the microprocessor (fabricated in a scaled low voltage nanometer CMOS technology), the range of input voltages that can be applied to a standard DC-DC converter circuit are further reduced. A standard non-isolated switching DC-DC converter topology such as a standard buck converter circuit as shown in Fig. 2 is, therefore, not suitable for future high performance integrated circuits which are likely to require high distribution voltages (on the printed circuit board) and monolithic DC-DC converters that can operate at high input voltages.

A cascode buffer circuit that can be used in a monolithic non-isolated switching DC-DC converter operating at a high input voltage is proposed in this paper. The proposed circuit can also be used as an I/O buffer to interface circuits operating at significantly different voltages. The proposed circuit, when used as part of a voltage regulator, ensures that the voltages across the terminals of all of the MOSFETs in a DC-DC converter are maintained within the limits imposed by an available low voltage CMOS technol-

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ogy. With the proposed circuit technique, high-to-low DC-DC converters operating at input voltages up to two times the maximum voltage (V_{max}) in a 0.18 μm CMOS technology are designed. An efficiency of 87.8% is demonstrated for a voltage conversion from 3.6 volts to 0.9 volts while supplying 250 mA of DC current.

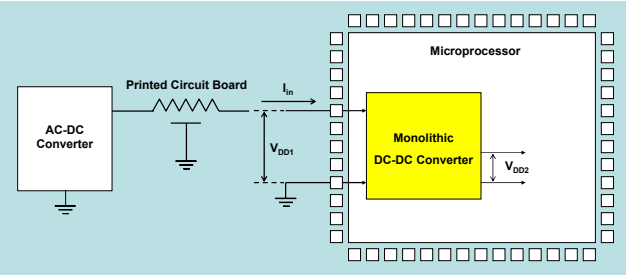

Fig. 1. High voltage off-chip power delivery and on-chip DC-DC conversion.

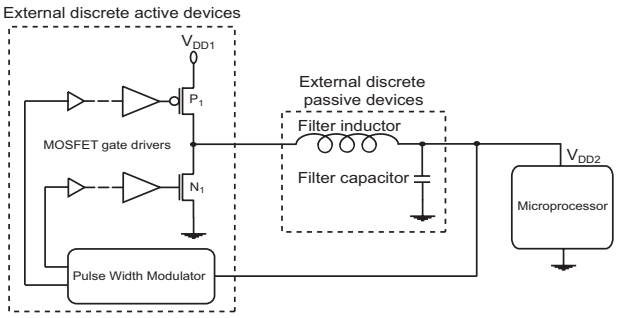

Fig. 2. A standard off-chip buck converter circuit ($V_{DD1} \leq V_{max}$).

The paper is organized as follows. The operation of the proposed cascade buffer and DC-DC converter is presented in Section 2. Simulation results of three voltage converters based on the proposed circuit technique are described in Section 3. Some conclusions are offered in Section 4.

2. LARGE STEP-DOWN NON-ISOLATED SWITCHING DC-DC CONVERTER

A non-isolated switching DC-DC converter circuit that can operate at input voltages higher than the maximum voltage (V_{max}) that can be directly applied across the terminals of a MOSFET in a deep submicrometer low voltage CMOS technology is described in this section. The operation of the proposed cascode buffer is described in Section 2.1. The DC-DC converter based on the proposed cascode buffer circuit is presented in Section 2.2.

2.1. Operation of the Proposed Cascode Buffer

A high-to-low DC-DC converter with a cascode buffer operating at an input supply voltage of $V_{DD1} = 2V_{max}$ is shown in Fig. 3. The proposed cascode buffer circuit generates an output signal swinging between ground and V_{DD1} from an input control signal swinging between ground and V_{DD3}, while guaranteeing that the voltages applied across the gate-to-source, gate-to-drain, and gate-to-body terminals of the MOSFETs do not exceed the maximum voltage difference, V_{max}, allowed in a CMOS technology. As shown in Fig. 3, the input supply voltage V_{DD1} can be as high as twice V_{max} while complying with the steady state voltage constraints across the terminals of all of the MOSFETs.

In Fig. 3, $V_{DD1} = 2V_{max}$ and $V_{DD3} = V_{max}$. The proposed cascode buffer behaves in the following manner. When the output of the pulse width modulator ($Node_7$) transitions low, $Node_4$ is pulled up to $2V_{max}$, turning off P_1. $Node_6$ is pulled up to V_{max}, turning on N_1. $Node_2$ transitions low through N_2 and N_1. $Node_1$ is discharged to $V_{DD3}+|V_{tp}|$. When the output of the pulse width modulator transitions high, $Node_6$ is pulled down to ground, cutting off N_1. $Node_4$ is pull down to V_{max} turning on P_1. $Node_2$ is pulled up to $2V_{max}$ through P_1 and P_2. $Node_3$ is charged to $V_{DD3}-V_{tn}$. $Node_5$ is maintained at V_{max} via V_{DD3}. The source and body terminals of P_2 and N_2 are shorted in order to ensure that the maximum permitted source-to-body and drain-to-body junction reverse bias voltages are not exceeded. With the proposed circuit technique, voltage differences between the terminals of all of the MOSFETs satisfy the voltage constraints dictated by a low voltage process technology while operating at high input and output voltages.

2.2. Operation of the Proposed DC-DC Converter

The operation of the proposed DC-DC converter circuit behaves in the following manner. The proposed cascode buffer produces an AC signal at $Node_2$ by a switching action controlled by a pulse width modulator. The AC signal at $Node_2$ is applied to a second order low pass filter composed of an inductor and a capacitor. The low pass filter passes the DC component of the signal at $Node_2$ to the output. A small amount (assuming the filter corner frequency is much smaller than the switching frequency f_s of the DC-DC converter) of high frequency harmonics generated by the switching action of the MOSFETs also reaches the output due to the nonideal characteristics of the output filter.

The output voltage $V_{DD2}(t)$ is

$$V_{DD2}(t) = V_{DD2} + V_{ripple}(t), \tag{1}$$

where V_{DD2} is the DC component of the output voltage and $V_{ripple}(t)$ is the voltage ripple waveform observed at the output due to the nonideal characteristics of the output filter. The DC component of the output voltage is

$$V_{DD2} = \frac{1}{T_s}\int_0^{T_s} V_s(t)dt = DV_{DD1}, \tag{2}$$

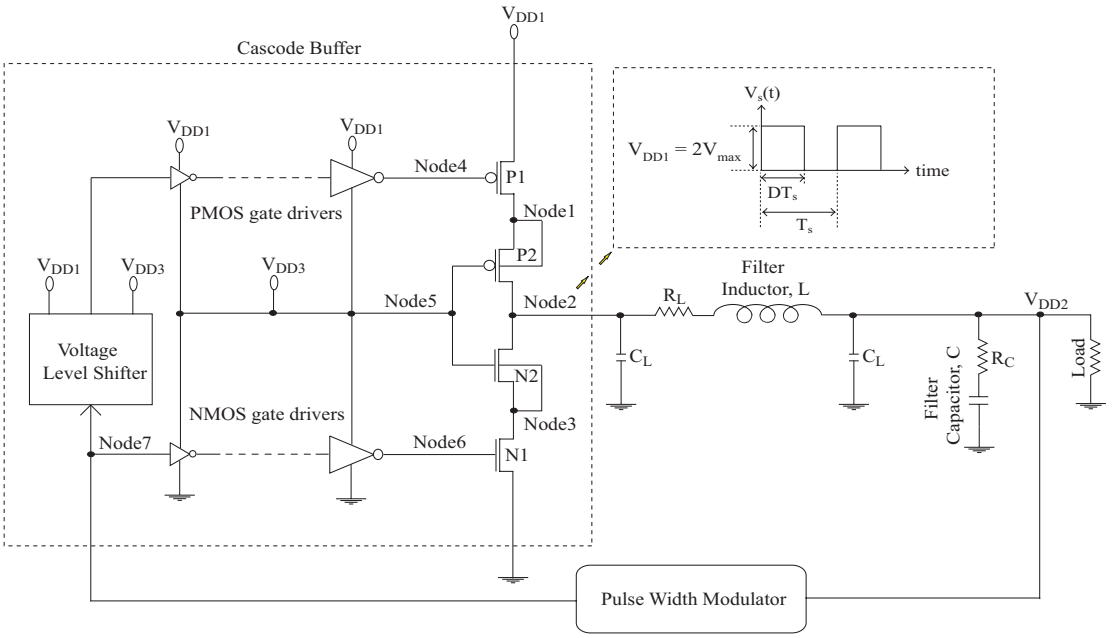

Fig. 3. The proposed DC-DC converter operating at an input supply voltage of $V_{DD1} = 2V_{max}$ ($V_{DD3} = V_{max}$).

where $V_s(t)$ is the ac signal generated at $Node_2$ and T_s, D, and V_{DD1} are the period, duty cycle, and amplitude, respectively, of $V_s(t)$. As given by (2), any positive output DC voltage less than V_{DD1} can be generated by the proposed DC-DC converter by varying the switching duty cycle D of the pull-up and pull-down network transistors.

3. SIMULATION RESULTS

Three DC-DC converters have been designed based on the proposed cascode bridge circuit. Simulation results characterizing the optimized maximum efficiency circuit configurations are presented in Section 3.1. A charge recycling mechanism in the proposed cascode bridge circuit significantly reduces the energy overhead of the proposed circuit technique and is discussed in Section 3.2.

3.1. Maximum Efficiency Circuit Configurations

The maximum voltage that can be applied across the terminals of a MOSFET (V_{max}) for the targeted 0.18 μm CMOS technology is 1.8 volts. The DC-DC converter shown in Fig. 3 provides 3.6 volts ($2V_{max}$) to 0.9 volts ($V_{max}/2$) conversion while supplying 250 mA per phase DC current to the load. Two other DC-DC converters have been designed for 2.7 volts ($1.5V_{max}$) to 0.9 volts ($V_{max}/2$) and 1.8 volts (V_{max}) to 0.9 volts ($V_{max}/2$) conversion using a similar circuit topology as shown in Fig. 3.

All three DC-DC converters have been simulated assuming a 0.18 μm CMOS technology. The circuit parameters are optimized to maximize efficiency while satisfying output voltage and current requirements. The efficiency of a DC-DC converter is

$$\eta = 100 \times \frac{P_{load}}{P_{load} + P_{internal}}, \tag{3}$$

where P_{load} is the average power delivered to the load and $P_{internal}$ is the average power dissipated in the internal parasitic impedances of a DC-DC converter. The optimized circuit configurations offering the highest efficiency for different voltage conversion ratios are listed in Table 1.

As listed in Table 1, an efficiency of 87.8% is achieved with the proposed DC-DC converter circuit for 3.6 volts to 0.9 volts conversion. The circuit operates at a switching frequency of 97 MHz. The filter capacitor and inductor of this maximum efficiency circuit configuration are 3 nF and 13.92 nH, respectively.

Efficiencies of 84.8% and 83.5% are observed for the 2.7 volts to 0.9 volts and 1.8 volts to 0.9 volts DC-DC converters, respectively. The parasitic energy dissipation within the DC-DC converter increases since the parasitic series resistances of the MOSFETs increase when the input supply voltage V_{DD1} is decreased. The efficiency achievable with the proposed DC-DC converter circuit is, therefore, reduced when the conversion ratio is decreased. Similarly, as listed in Table 1, the optimum transistor width that maximizes efficiency increases as the voltage conversion ratio is reduced.

A standard buck converter circuit has also been designed with the maximum input supply voltage ($V_{DD1} = V_{max} = 1.8$ volts) that can be applied to a standard buck converter. For 1.8 volts to 0.9 volts conversion while supplying 250 mA current, the efficiency attained with a stan-

TABLE 1
CIRCUIT CHARACTERISTICS OF THE OPTIMIZED MAXIMUM EFFICIENCY CASCODE BUFFER DC-DC CONVERTERS AND A STANDARD BUCK CONVERTER FOR DIFFERENT INPUT SUPPLY VOLTAGES

DC-DC Converter	Conversion Ratio	V_{DD1} (V)	V_{DD2} (V)	V_{DD3} (V)	Max η (%)	f_s (MHz)	C (nF)	L (nH)	W_{NMOS} (mm)	W_{PMOS} (mm)	I_{VDD3} (mA)
$Circuit_1$	4:1	3.6	0.9	1.8	87.8	97	3	13.92	6.05	7.25	-2.89
$Circuit_2$	3:1	2.7	0.9	1.35	84.8	97	3	12.37	8	11.2	-1.01
$Circuit_3$	2:1	1.8	0.9	0.9	83.5	97	3	9.28	11.61	24.39	-0.88
Buck	2:1	1.8	0.9	N/A	87.8	97	3	9.28	4.39	9.21	N/A

dard buck converter is 4.3% higher than the efficiency achieved with the proposed DC-DC converter. The width of the power MOSFETs in a buck converter are also significantly smaller as compared to the proposed DC-DC converter (for a 2:1 conversion ratio).

3.2. Charge Recycling Mechanism

As listed in Table 1, the proposed circuit technique offers a similar efficiency while doubling the voltage conversion ratio (as compared to a standard buck converter circuit producing the same output voltage) without creating any MOSFET reliability issues. The high efficiency achieved for a significantly higher voltage conversion ratio as compared to a standard buck converter circuit is attributed to a charge recycling mechanism that exists in the proposed cascode buffer circuit. At any time during a state changing transition of the output of the pulse width modulator (independent of the direction of the transition), a portion of the charge required by the inverters to drive $Node_6$ originates from the discharging parasitic capacitances of the gate drivers of P_1 rather than from the power supply V_{DD3}. Most of the charge drawn from V_{DD1} during an output low-to-high transition of a gate driver of P_1 is thereby recycled for use inside the drivers of N_1 before discharged to ground.

As listed in Table 1, the average current drawn from V_{DD3} is significantly smaller than the load current. The energy overhead of the additional reference voltage required for proper operation of the proposed cascode bridge circuit is, therefore, small. V_{DD3} can be generated by a simple integrated linear regulator without significantly affecting the overall efficiency of the proposed DC-DC converter. For all three DC-DC converters, the average current supplied by V_{DD3} is negative, meaning that the extra power supply essentially sinks rather than supplies current. The primary purpose of V_{DD3} is, therefore, to maintain the voltage of $Node_5$ at V_{max} rather than supply current to the switching gate driver buffers of N_1.

4. CONCLUSIONS

A cascode bridge circuit that can be used in a monolithic non-isolated switching DC-DC converter with a high voltage conversion ratio is proposed in this paper. The proposed circuit can also be used as an I/O buffer to interface circuits operating at significantly different voltages without creating any MOSFET reliability issues due to high voltage stress. The proposed circuit, when used as part of a voltage regulator, ensures that the voltages across the terminals of all of the MOSFETs in a monolithic DC-DC converter are maintained within the limits imposed by an available low voltage CMOS technology.

High-to-low DC-DC converters have been designed based on the proposed cascode bridge circuit. Reliable operation of the proposed DC-DC converters operating at an input supply voltage up to two times as high as the maximum voltage (V_{max}) that can be directly applied across the terminals of a MOSFET is verified assuming a 0.18 μm CMOS technology. The energy overhead of the proposed circuit technique is low due to a charge recycling mechanism in the MOSFET gate drivers. An efficiency of 87.8% is demonstrated for a voltage conversion from 3.6 volts to 0.9 volts while supplying 250 mA of DC current.

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5. REFERENCES

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