Low Power Repeaters Driving RLC Interconnects with Delay and Bandwidth Constraints

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***Abstract*— Interconnect plays an increasingly important role in deep submicrometer VLSI technologies. Multiple design criteria are considered in interconnect design, such as delay, power, and bandwidth. In this paper, the effects of inductance on the delay, bandwidth, and power of an RLC interconnect with repeaters are analyzed. A repeater insertion methodology is presented for achieving the minimum power in an RLC interconnect while satisfying delay and bandwidth constraints. By including inductance, the minimum interconnect power under a delay and/or bandwidth constraint decreases as compared with an RC interconnect.**

I. Introduction

Repeater insertion is an efficient method for reducing interconnect delay and signal transition times. The optimal number and size of the repeaters to achieve the minimum delay of an RLC interconnect has been described in [1]. The size of an optimal repeater is typically much larger than a minimum sized inverter. Since millions of repeaters will be inserted to drive global interconnects in future high complexity integrated circuits, significant power will be consumed by these repeaters, particularly if delay-optimal repeaters are used. A power-delay tradeoff is, therefore, necessary to support efficient repeater insertion methodologies [2].

The number and size of repeaters are determined in [3] to minimize the total dynamic switching power and area while satisfying a target delay constraint. By including both short-circuit and leakage power, a more practical design methodology is presented in [4]. In [5], closed form solutions for achieving the minimum power while satisfying delay and bandwidth constraints are developed. In these papers, inductance effects are not included. In upper metal layers, wide interconnects are frequently used, which have low resistance, making inductance effects non-negligible.

In this paper, the results described in [5] are extended by including inductance effects on the delay, transition time, and power. The paper is organized as follows. In section II, a timing and power model of an RLC interconnect with repeaters is presented. In section III, the effects of inductance on the design space of repeaters are analyzed. In section IV, the power consumption while satisfying delay and bandwidth constraints is described. Finally, some conclusions are offered in section V.

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II. Timing and Power Model

As shown in Fig. 1, a distributed RLC interconnect with length l is evenly divided into k segments with uniformly sized repeaters. The repeaters are h times as large as a minimum sized repeater, with the output resistance R_{tr0}/h, output capacitance hC_{d0}, and input capacitance hC_{g0}, where R_{tr0}, C_{d0}, and C_{g0} are, respectively, the output resistance, output capacitance, and input capacitance of a minimum sized repeater.

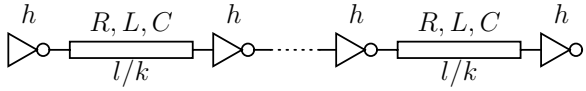

Fig. 1. Repeater insertion in an RLC interconnect.

The repeater is assumed in this paper to be implemented as a CMOS inverter. The inverter is also assumed to be symmetric such that the effective output resistance is the same for both rising and falling signal transitions. The Berkeley predictive technology model (BPTM) [6] for a 45 nm printed channel length is used, corresponding to the 80 nm technology node described in the ITRS [7]. Some model parameters are modified to capture the trends of the saturated drain current and subthreshold current predicted by the ITRS.

By including the repeater output capacitance, the variable ζ [1] used to characterize the inductance effect becomes

$$\zeta = \frac{Rl}{2k}\sqrt{\frac{C}{L}} \cdot \frac{R_T C_T (1+\frac{C_{d0}}{C_{g0}}) + C_T + R_T + 0.5}{\sqrt{1+C_T}}, \quad (1)$$

where $R_T = kR_{tr0}/(hRl)$ and $C_T = hkC_{g0}/(Cl)$. R_{tr0} can be approximated as $R_{tr0} = KV_{dd}/I_{dn0}$, where K is a fitting parameter, and I_{dn0} is the saturated drain current of a minimum sized NMOS transistor with both V_{gs} and V_{ds} equal to V_{dd}. K can be determined by matching the step response of an RC equivalent circuit to SPICE simulations. Note that the K obtained by matching the 50% delay and by matching the transition time is different, and the corresponding ζ is therefore denoted as ζ_d and ζ_r, respectively. The delay model of the

interconnect is an extension of the result from [1] where the repeater output capacitance and input slew effects are included. The delay of a single stage interconnect can be obtained by curve fitting,

$$t_{ds} = \frac{e^{-2.3\zeta_d^{1.5}} + 1.48\zeta_d}{w_n}, \tag{2}$$

where $w_n = k/\sqrt{Ll(Cl + C_{g0}hk)}$. The coefficients in (2) are slightly different from those in [1] due to the effects of the repeater output capacitance. In [8], an accurate estimate of the rise time in an RLC interconnect is also obtained by curve fitting. The expressions, however, are analytically complicated. In this paper, a simplified piecewise approximation of the rise time is used,

$$t_r = \frac{t_{90\%} - t_{10\%}}{0.8} = \begin{cases} \frac{4.4\zeta_r - 1.8}{0.8 w_n} & \zeta_r > 0.41, \\ 0 & \text{otherwise.} \end{cases} \tag{3}$$

When $\zeta_r < 0.5$, the interconnect is highly inductance dominant, and (3) can introduce a large error.

Input slew effects are also not considered in (2). With a finite input slew rate, the repeater delay depends linearly on the input transition time [9]. The contribution of t_r to the repeater delay can be represented by γt_r, where [9]

$$\gamma = \frac{1}{2} - \frac{1 - v_t}{1 + \alpha}. \tag{4}$$

In (4), α is the velocity saturation index, and v_t is the normalized threshold voltage. The input slew effect on the far end transition time is ignored. The total delay of the interconnect with repeaters is

$$T_{total} = k(t_{ds} + \gamma t_r). \tag{5}$$

There are three types of power consumption in digital CMOS circuits: dynamic switching power, short-circuit power, and leakage power. The interconnect power models used in this analysis are the same as those used in [5].

III. Effects of Inductance on the Repeater Design Space

A design space for investigating the optimal design of a repeater system is determined to satisfy a delay or bandwidth constraint [5]. By including inductance, both the delay and transition time of an RLC interconnect are affected. The design space for repeaters will, therefore, also change.

A. Bandwidth constraints

The bandwidth of an interconnect is limited by the signal transition time. Shorter signal transition times support a smaller signal bit period, therefore, a higher bandwidth. The signal transition time at the far end of an RLC interconnect decreases with increasing inductance effects [10]. Inductance, therefore, improves the bandwidth of an interconnect. For a bandwidth constraint B_{req}, the signal transition time is assumed to be less than or equal to half the bit period, *e.g.*, $t_r \leq 1/2B_{req}$. The design space of repeaters under a bandwidth constraint is plotted in Fig. 2 for different inductance values. With increasing inductance, the number and size of the repeaters can be reduced while maintaining the same signal transition time. The design space is the area in the upper-right side of the curve, as shown in Fig. 2.

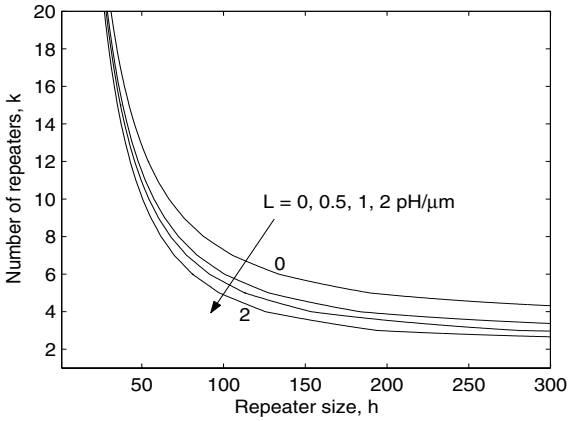

Fig. 2. Effects of inductance on the design space of repeaters satisfying bandwidth constraints. $B_{req} = 2$ Gb/s, $l = 10$ mm, and $W = 10W_{min}$, where W_{min} is the minimum wire width specified in the ITRS.

B. Delay constraints

The delay of an interconnect with repeaters can be affected by inductance in three ways. First, the propagation delay along the interconnect can increase with increasing inductance [11]. Second, inductance reduces the signal transition time, decreasing the gate delay due to the input slew effect. Third, due to the shielding effects of the interconnect inductance, both the effective capacitance seen by the driver and the equivalent output resistance of the driver are reduced [11]. The gate delay, therefore, is further reduced. (Since the delay model used in this paper is based on curve fitting, and a constant driver resistance is assumed, the third inductance effect is not considered in the model).

As presented above, interconnect inductance has competing effects on the total delay. The total delay of an interconnect with repeaters is plotted in Fig. 3. As shown in Fig. 3, with increasing line inductance, the total delay decreases until a minimum delay is achieved. The analytic model overestimates the inductance effects when the inductance is low, however, the trend of the inductance effect is captured. In Fig. 4, the design space for repeaters under a delay constraint is plotted for different inductance values. The operational design space is the area inside a closed curve. Only the portion with fewer and smaller repeaters is of interest and plotted in Fig. 4. Note that the design space first expands and then shrinks with increasing inductance.

IV. Power Dissipation with Delay and Bandwidth Constraints

The inductance affects the minimum power with delay and bandwidth constraints in two ways. First, the design space is changed as discussed in section III. Second, the short-circuit power consumed by the repeaters may also be affected by inductance for a fixed interconnect configuration.

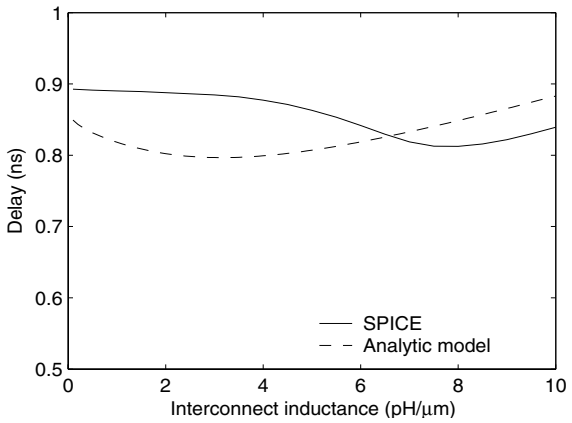

Fig. 3. Effects of inductance on interconnect delay with repeaters. $l = 10\,\text{mm}$, $k = 10$, $h = 100$, and $W = 10W_{min}$.

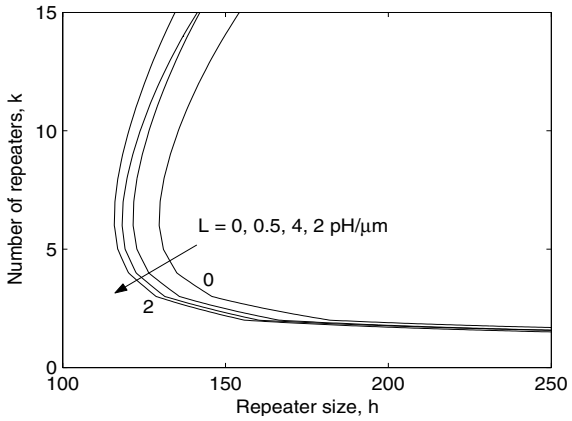

Fig. 4. Effects of inductance on the design space of repeaters with delay constraints. $T_{req} = 700\,\text{ps}$, $l = 10\,\text{mm}$, and $W = 10W_{min}$.

As presented in section III, inductance can produce faster signal transition times, reducing the time during which the short-circuit current can flow [10]. Inductance also shields part of the far end capacitance [11], resulting in a smaller effective load capacitance and increasing the peak short-circuit current.

By matching the moments of the driving point admittance, a distributed RLC interconnect with a capacitive load can be represented by a π model, as shown in Fig. 5. The effective capacitance of this π structure can be obtained in a similar way as in [12]. Since the effective capacitance should be evaluated to determine the short-circuit current, which exists during a non-step input signal transition time, the evaluation time point is taken as $t_r/2$. In [12], the driver output is approximated by a quadratic function followed by a linear function. The output waveform of the repeaters generally follows a quadratic function during the input transition time. With this assumption, the effective capacitance of the π model is

$$C_e = C_n + C_f\left(1 - \frac{4R_\pi C_f}{t_r} + \frac{8k_3}{t_r^2 s_1}\left(e^{\frac{s_1 t_r}{2}} - 1\right) + \frac{8k_4}{t_r^2 s_2}\left(e^{\frac{s_2 t_r}{2}} - 1\right)\right), \tag{6}$$

where s_1 and s_2 are the roots of $L_\pi C_f s^2 + R_\pi C_f s + 1 = 0$, and $k_3 = 1/[s_1^2(s_1 - s_2)L_\pi C_f]$ and $k_4 = 1/[s_2^2(s_2 - s_1)L_\pi C_f]$.

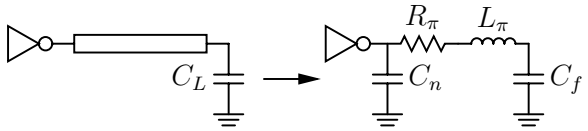

Fig. 5. π model representation of a distributed RLC interconnect.

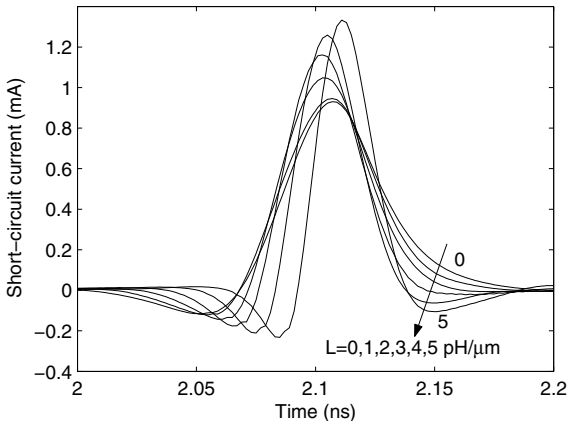

Fig. 6. Effects of inductance on short-circuit current in repeaters. $l = 10\,\text{mm}$, $k = 10$, $h = 150$, and $W = 10W_{min}$.

In Fig. 6, the short-circuit current of a repeater in an interconnect system is shown for different inductance values. The short-circuit energy consumed in one signal transition is shown in Fig. 7. When $h = 100$, the inductance effect on the transition time cancels the inductive shielding effect on the load, making the short-circuit power less sensitive to inductance. This result shows that the common assumption that inductance can reduce short-circuit power is not always true. Actually, the short-circuit energy slightly increases with increasing inductance until a maximum energy is achieved. With increasing repeater size, the effect of inductance on the transition time increases and starts to dominate the inductive shielding effect on the load for large inductances, decreasing the short-circuit power. For $h = 150$, the short-circuit energy is almost constant when $L < 2\,\text{pH}/\mu\text{m}$, however, both the period and peak value of the short-circuit current vary over this inductance range, as shown in Fig. 6. For larger repeaters (*e.g.*, $h = 200$), the effect of inductance on the transition time dominates the shielding effect for any value of inductance. The short-circuit power always decreases with increasing inductance.

As described in [5], the minimum power of an RC interconnect with repeaters can be achieved on the edge of the design space. For practical RLC interconnect structures, this behavior is also valid. Given a design space, the minimum power can be solved numerically by applying the Lagrange method. In Fig. 8, the minimum achievable power of an interconnect with inserted repeaters while satisfying a delay constraint is plotted for different values of inductance. The clock frequency is 1 GHz, and the switching coefficient is 0.15 [4]. As shown in Fig. 8, by including inductance, the minimum interconnect

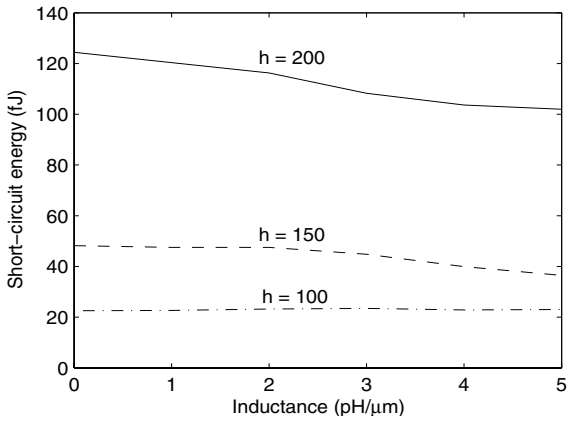

Fig. 7. Effects of inductance on the short-circuit power of repeaters. $l = 10\,\text{mm}$, $k = 10$, and $W = 10W_{min}$.

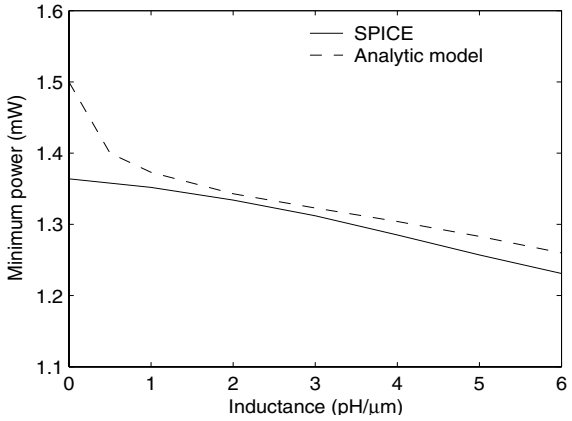

Fig. 8. Effects of inductance on the minimum interconnect power satisfying a delay constraint. $l = 15\,\text{mm}$, $W = 10W_{min}$, and $T_{req} = 1\,\text{ns}$.

power under a delay constraint is slightly reduced. This reduction is partially due to the extension of the design space (for small inductance values) and partially due to the reduction in short-circuit power (for large inductance values).

As described in [5], the minimum power of an RC interconnect with bandwidth constraints can be achieved with minimum sized repeaters. This statement, however, is not correct for RLC interconnect. The optimal k for an RLC line to achieve the minimum power with a bandwidth constraint, however, is normally unpractically large. In Fig. 9, the minimum achievable power of an RLC interconnect with a bandwidth constraint is plotted for different inductance values, and the error of the analytic model is less than 6% as compared with SPICE. In this example, k is limited to 10. As shown in Fig. 9, the inductance slightly reduces the minimum power under a bandwidth constraint.

V. Conclusions

Given a delay and/or bandwidth constraint, a design space for repeaters inserted in an RLC interconnect can be determined. Based on the analysis of inductance effects on this design space, a repeater design methodology is presented for

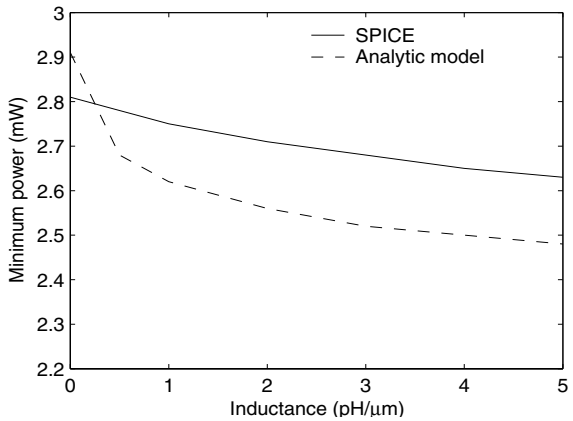

Fig. 9. Effects of inductance on the minimum interconnect power satisfying a bandwidth constraint. $l = 15\,\text{mm}$, $W = 10W_{min}$, and $B_{req} = 2$ Gb/s.

achieving the minimum power while satisfying delay and/or bandwidth constraints. It is also shown in this paper that the effect of inductance on interconnect delay (including the delay of the repeaters) and on short-circuit power is non-monotonic. The overall effects of inductance reduce the minimum achievable power under a delay and/or bandwidth constraint.

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