# Managing Substrate and Interconnect Noise from High Performance Repeater Insertion in a Mixed-Signal Environment

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*Abstract*—**With technology advancements in the very-deep submicrometer (VDSM) regime and system-on-a-chip (SOC) integration, high performance, low-voltage, and low-noise are becoming stringent challenges. Interconnect and crosstalk dominated digital design requires solutions to manage interconnect delay and crosstalk noise. SOC integration requires minimal interaction between the digital and analog/RF on-chip blocks that operate at increasingly lower power supplies. Such power supplies affect the signal-to-noise ratio of both the analog/RF as well as the digital blocks. These topics describe the general area of this paper. High-performance digital buffers targeting SOC are presented. Methods for reducing the impact of interconnect and substrate crosstalk generated by the buffers with implications on the on-chip analog/RF and digital blocks are discussed.**

## I. INTRODUCTION

The complexity of the design process for high-performance Systems-on-a-Chip (SOC) mixed-signal systems is tremendous [1, 2]. There is no clear boundary between the digital, analog/RF, and high-performance circuits. For example, the high performance digital circuits operating at several GHz clocks requires in-depth analog and, in certain cases, microwave techniques.

In an era dominated by interconnect [3], a highly demanding area is the design of amplifying buffers for reasons such as:

1. A buffer is a high-current circuit.
2. Buffers are required to drive $RC$ and $RLC$ interconnect [4–7], requiring methodologies for optimal placement [8].
3. A buffer is a source of skew and process parameter variations (PPV).
4. The delay of a buffer needs to be tightly controlled.
5. The rise and fall times at the output of a buffer and along the interconnect need to be short and repeatable in order to minimize jitter.
6. Noise generated by such buffers, either across the interconnect or into the substrate, must be well controlled to minimize the effects of noise on neighboring digital, analog, and RF blocks (in a mixed-signal SOC environment) [9, 10].
7. Power and area need to be maintained at acceptable levels.
8. The noise immunity of the buffer needs to be controlled (a buffer affected by noise may generate spurious transitions, or produce increased jitter) [11].
9. Parasitic impedances of the power/ground lines and electromigration need to be controlled due to the large current spikes in these buffers.
10. The placement of decoupling capacitors to minimize aspects such as resonances in the power/ground lines and to provide local charge.
11. The signal-to-noise ratio in low-voltage deep-submicrometer circuis.

Note the multiple challenges that a good buffer design imply: timing, PPV, noise, power, area, parasitic impedances, electromigration, power/ground distribution issues, SOC aspects, analog/RF integration, and low-voltage design.

## II. ADDRESSING CHALLENGES THROUGH CIRCUIT AND PHYSICAL DESIGN

The tapered buffer, as shown in Fig. 1, is the classic technique to drive capacitive loads [12]. Tapered buffers or single inverters are used as repeaters to drive $RC$ and $RLC$ loads. Optimal repeater insertion methodologies have been developed and are widely used to satisfy specific optimization criteria.

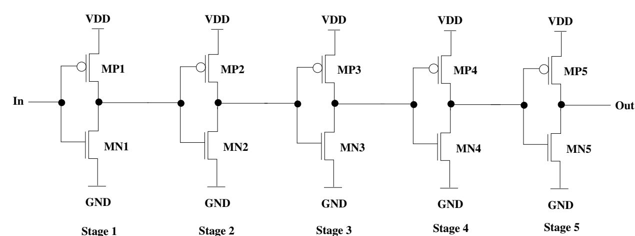


Fig. 1. A classic tapered buffer

With every generation of deep-submicrometer technology, the cost of the design process of a buffer circuit becomes greater:

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• Timing - depending on the direction of the signal transition of a node, either the N or the P transistor is a parasitic load (see Fig. 1) [13].
• PPV - many stages and low driving efficiency increase the effect
• Noise - large parasitic capacitances produce large current on the power/ground lines, increasing the simultaneous switching noise (SSN) and the substrate noise
• Power - large parasitic capacitances produce large dynamic power, and high short-circuit power due to slow signal transitions
• Area - low driving efficiency and large number of stages lead to large area
• Large current spikes lead to significant power distribution network issues and poor signal-to-noise ratio in low-voltage circuits

The buffer shown in Fig. 2, called the HD buffer [13], eliminates the parasitic load transistors in the signal path by implementing two parallel paths, each optimized for the low-to-high and high-to-low transitions, respectively.

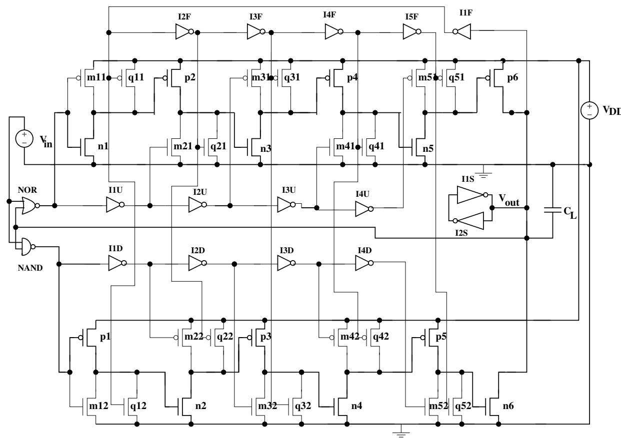


Fig. 2. Optimized buffer for efficient driving

Depending upon the target tradeoff, the buffer can be optimized for speed by up to 2.5x, reduced power dissipation, up to 500% area savings, or faster transition times, as compared to a classic tapered buffer. The peak current is also significantly reduced, decreasing the effect of noise.

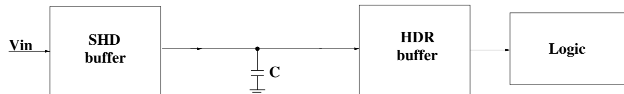


Fig. 3. Optimized buffer scheme to drive large capacitive loads with significant power savings

The buffer can be optimized to drive very large capacitive loads while producing significant power savings [14]. In Fig. 3, an SHD buffer is an HD buffer optimized for power dissipation.

Specifically for $RC$ lines, such as a long bus line, the HD buffer can be optimized to exploit the native hysteresis of a circuit [15]. The resulting buffer, shown in Fig. 4, inserted as a repeater along an $RC$ line, achieves significant savings in delay, power, and area.

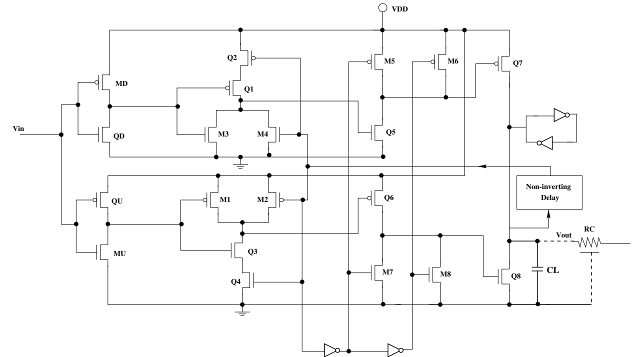


Fig. 4. A three stage HDR buffer optimized to drive $RC$ lines

One drawback of the HDR buffer is the increased sensitivity to noise due to the lower switching thresholds. The differential HDR buffer [16], the HDRN buffer, used as shown in Fig. 5, addresses this drawback, eliminating any parasitic switching due to spurious interconnect-coupled noise.

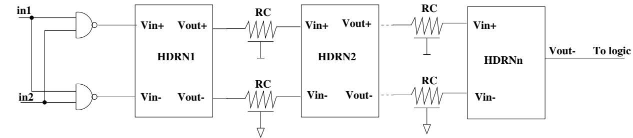


Fig. 5. The use of an HDRN buffer to eliminate sensitivity to noise

If the improvements in speed provided by the HDR and HDRN buffers are not sufficient for a specific $RC$ line, the *transparent repeater*, TR [17], shown in Fig. 6, can be used. With a power and area penalty, the transparent repeater can drive an $RC$ line up to five times faster than a standard repeater insertion methodology.

Optimizing the capacitance at internal nodes, minimizing the number of stages in a buffer, and using analog design techniques to implement a digital function are the primary techniques used to achieve these significant performance improvements. Any buffer circuit, however, generates large instantaneous current spikes, therefore, large interconnect and substrate noise. The large transistor size and fast transition times are directly proportional to the amount of noise generated on both the interconnect and substrate. Interconnect and substrate noise are fundamentally related - for example, a large interconnect noise on the power/ground

network generates substrate noise through the substrate/well contacts (see Fig. 7).

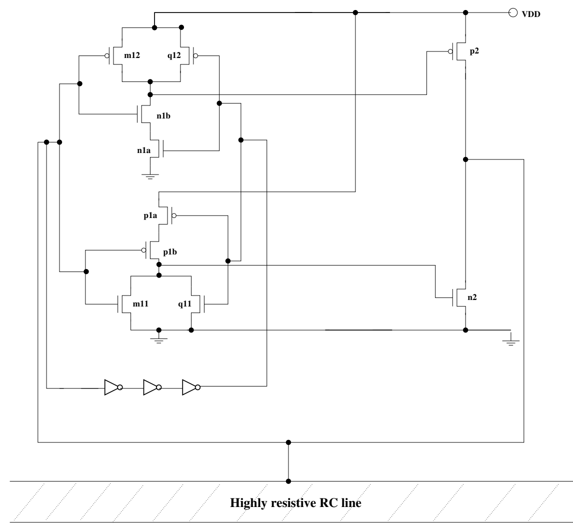


Fig. 6. A transparent repeater ($TR$) and method of insertion in an interconnect line

Minimizing these two types of noise, interconnect and substrate, is a fundamental requirement in SOC integration of mixed-signal systems operating at low voltages. An SOC may include high performance digital circuit blocks (highly sensitive to noise induced jitter and skew), analog/RF circuit blocks (highly sensitive to both types of noise), power management blocks and power amplifiers (large noise generators with specific noise generating characteristics), and memory blocks. Electromagnetic interaction plays a significant role in such on-chip integration [18], not only due to the interaction between the on-chip inductors and the surrounding circuit blocks/substrate, but also by means of interaction between the interconnect carrying various types of signals, as well as by means of interactions between the electromagnetic fields of the bonding wires.

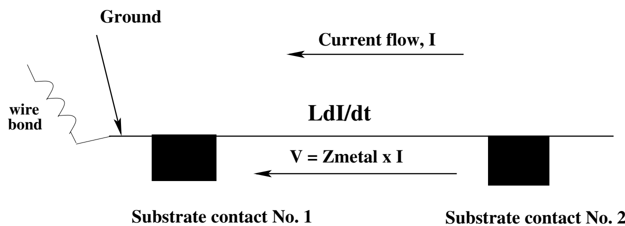


Fig. 7. Connection between interconnect (power/ground) and substrate noise

A digital noise, generated by a buffer into the substrate, and monitored close to the generating buffer is illustrated in Fig. 8. The transition of the input signal generates noise spikes in the substrate, characterized by an amplitude and settling time. The two characteristics of this noise depends upon a large number of variables, such as the rise and fall times of the input signal, the relative position of the substrate contacts and rings in the vicinity of the noise generator, and the different strategies for noise reduction such as the use of triple wells.

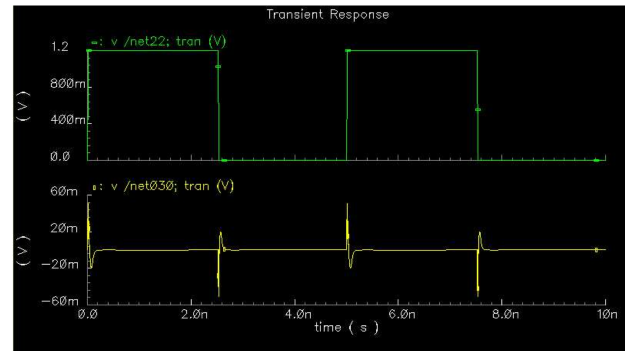


Fig. 8. Noise generated by a buffer in the substrate

The dependence of the noise being generated in the substrate on the rise and fall times is shown in Fig. 9. Note a 4x decrease in noise when the rise and fall times are increased from 20 ps to 150 ps. This large degradation in the rise and fall times is typically not possible or desirable in gigahertz frequency clocks. A moderate decrease in rise and fall times, however, may be acceptable. For example, for large busses, a reduced rise/fall time may be affordable (low noise generated by the large buffers). At the receiver, a Schmitt trigger is inserted to restore the rise/fall signal times (low noise, since the Schmitt trigger drives a reduced load). The approach has certain similarities with the circuit shown in Fig. 3.

Physical design techniques represent a powerful tool to reduce substrate noise. For example, the presence of a guard ring in the vicinity of a digital block may reduce the amplitude of the peak-to-peak noise by a factor of three. Reducing the noise does not represent the only technique for achieving improved noise immunity in a mixed-signal environment. Physical design techniques to insure noise uniformity across the substrate in a sensitive area represents a powerful approach to improve noise immunity. Such an approach insures that the noise in the sensitive area is common mode, and, depending on the circuit architecture, is rejected.

Shielding the sensitive interconnect can protect the sensitive nodes from capacitive coupling induced noise from the neighbouring interconnect or substrate. A shield can significantly minimize the impact of elctromagnetic interactions.

A powerful technique to minimize the impact of

noise generated due to large current spikes generated by the buffers is by controlling the parasitic impedances of the power/ground distribution network. Using multiple power/ground lines and ensuring that the sensitive parts of the circuit are powered by a low-inductance power/ground network carrying a low amount of current, are effective ways to reduce the impact of such noise.

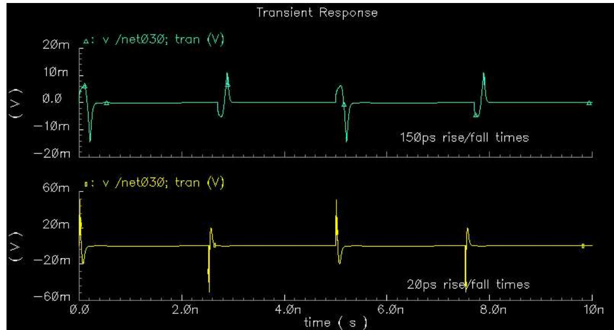


Fig. 9. Dependence of noise generated in the substrate on digital input rise/fall times

## III. CONCLUSIONS

Interconnect dominated digital design requires efficient techniques to drive deep submicrometer interconnect operating in the GHz frequency range. High frequency effects, *RLC* interconnects, low-voltage issues, and SOC integration each create a challenging design environment.

The driving efficiency of a buffer represents a key issue in addressing many of the challenges in buffer design. Several original buffer circuits that achieve various optimization criteria are presented. Each of these buffers provide significantly improved driving efficiency. Possible optimizations achieve significantly improved speed, power, area, noise, and address the optimal driving of a large range of critical loads.

Noise is a highly critical challenge in a mixed-signal SoC. A high performance buffer is a large noise generator. Interconnect noise, in particular with reference to power/ground lines, as well as substrate noise aspects, are discussed. Recommendations to improve the noise behavior in mixed-signal systems are provided.

A high performance buffer design needs to consider a multitude of challenges. A customized buffer design to optimally address a multitude of critical design aspects, to provide high drive efficiency, to minimize the generated current spikes, as well as employing an optimal physical design and technology specific noise reduction techniques, represent powerful strategies to address many of the challenges in current and future buffer circuit design.

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