Via Placement for Minimum Interconnect Delay in Three-Dimensional (3-D) Circuits

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Abstract— **The propagation delay of interlayer 3-D interconnects is investigated in this paper. For *RC* interconnects connecting two circuits located on different physical planes, the interconnect delay is minimized by optimally placing the non-stacked interlayer vias. The problem of determining these optimum via locations under the Elmore delay model is described as a geometric program. Simulations indicate delay improvements of up to 26% for relatively short interconnects. The proposed approach is also compared with a wire sizing algorithm. Timing-driven via placement exhibits better results both in terms of delay and power consumption.**

I. INTRODUCTION

The performance of integrated circuits (ICs) can be enhanced by technology scaling, producing smaller and faster devices; long interconnects, however, can significantly degrade this improvement. Repeater insertion and other design techniques, such as wire sizing, have been developed to mitigate these effects. As clock frequencies increase, however, both the number and power of the buffers increase beyond where there is no longer any performance benefit. To sustain performance improvements in future technology generations, non-conventional design paradigms are required.

Three-dimensional (3-D) integration is such a promising alternative which offers the opportunity to relieve the deleterious effects of long interconnects. Another important characteristic of 3-D structures is that these circuits can include various technologies such as GaAs and SiGe, and design disciplines such as analog, digital, and MEMS within a single 3-D multiplane system. Several research efforts have focused on developing manufacturing techniques for 3-D technologies [1-3]. A schematic of a 3-D circuit is illustrated in Fig. 1, where several physical planes are bonded with adhesive materials or metal pads [4]. Each physical plane of the stack is similar to a conventional two-dimensional (2-D) circuit, in that a plane includes a device layer and multiple metal layers to connect individual circuits located on the same physical plane (the intralayer interconnects). Interconnections among the physical planes (the interlayer interconnects) are implemented by vertical through vias, which are called vias here for brevity.

To evaluate the performance of three-dimensional circuits, several *a priori* interconnect prediction models have been described in the literature [5]-[7]. The delay expressions included in these interconnect prediction models for 3-D circuits are similar to traditional CMOS models, neglecting the impact of the vias. Zhang *et al.* [8] consider the effect of the vertical vias on the interlayer interconnects in their delay expression; however, the via is assumed to be placed in the middle of the line, independent of the line length and impedance, leading to significantly inaccurate delay estimation [9].

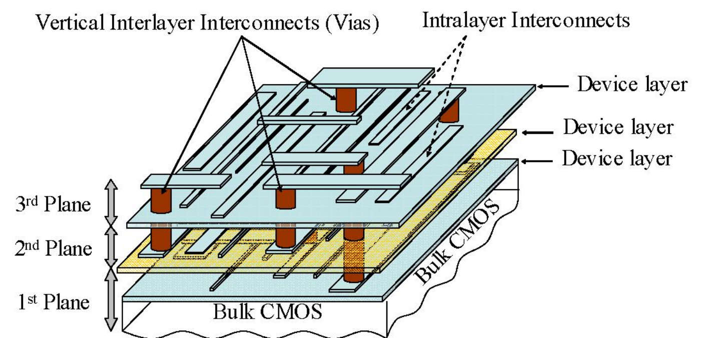

Figure 1. Schematic of a three-dimensional circuit.

To fully exploit the potential of 3-D circuits, sophisticated placement and routing algorithms are required [10], [11]. Due to the significance of thermal effects in 3-D circuits, a thermal-driven algorithm for via placement was presented in [12]. These algorithms, however, do not address the savings in delay that can originate from the optimum placement of the vias while simultaneously considering the non-uniform impedance characteristics of the interlayer interconnects. It is shown in [9] that considerable delay savings can be achieved when the via location is considered during the routing process. In this paper, the results presented in [9] are extended to more complicated structures such as vias that cannot be stacked due to obstacles or other routed interconnects.

In the following section, the problem of timing-driven placement of vias between interlayer interconnects in 3-D ICs is described. A delay expression for a 3-D interconnect system as a function of the length of the interconnect segments is presented in Section 3. In Section 4, simulation

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results that demonstrate the decrease in interlayer interconnect delay and power consumption achieved by optimally placing the vias are presented along with a comparison with a wire sizing algorithm. Finally, some conclusions are offered in Section 5.

II. Problem Formulation

The primary contribution of this work is introduced in this section. Consider the interlayer inteconnect shown in Fig. 2 that consists of n horizontal segments connecting two circuits located m physical planes apart. Each of the horizontal segments of the line corresponds to a metal layer of some physical plane of the stack. The horizontal segments of the line are connected through the vias which can traverse more than one plane. Consequently, the number of horizontal segments of the line is smaller than or at most equal to the number of physical planes between the two circuits, *i.e.*, $m \geq n$, where the equality applies when each of the vias connects metal layers from two adjacent physical planes.

In conventional 2-D circuits, a two terminal net such as the structure shown in Fig. 2 is modeled as a line with uniform impedance characteristics, while the vias are either ignored or considered as lumped capacitive loads. The heterogeneity of 3-D circuits, however, does not support a uniform line model. In 3-D systems, circuits from different processes and disparate technologies are integrated onto a single multiplane system. The interlayer interconnect lines are therefore modeled as wire segments with non-uniform impedance characteristics. Due to the non-uniform impedance characteristics of the line, the via locations or, alternatively, the length of each horizontal wire segment affects the delay of the line. Thus, the objective is to place the vias such that the interconnect delay is minimum. To analyze the delay of a line, the Elmore delay model has been adopted due to the simplicity and high fidelity of this model. The accuracy of the model can be further improved as discussed in [13]. Interconnects that exhibit inductive behavior are not addressed in this paper. The analysis of the optimum via placement problem is presented in the following section.

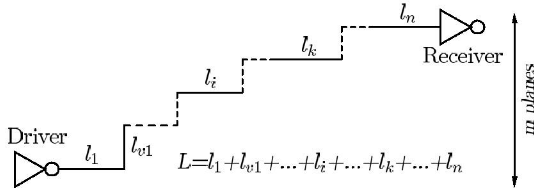

Figure 2. Interlayer interconnect consisting of n segments and connecting two circuits located m planes apart.

III. Optimum Via Placement

In this section, the optimum via location problem is discussed. Consider again the interlayer interconnect shown in Fig. 2. Each horizontal segment i of the line is located on a different physical plane with length l_i. The vias are denoted by the index of the first of the two connected segments. For example, if a via connects segment i and i+1, the via is denoted as v_i with length l_{vi}. The total length of the line L is equal to the summation of the length of the horizontal segments and vias and can be written as

$$L = l_1 + l_{v1} + \ldots + l_i + l_{vi} + \ldots + l_n \,. \tag{1}$$

In addition, the length of each horizontal segment is bounded,

$$l_{i\min} \leq l_i \leq L - \sum_{j=1, j\neq i}^{n} l_{j\min} \,. \tag{2}$$

The lower bound in (2) results from the presence of obstacles that prohibit the placement of a via in certain locations, while the upper bound is set such that only two circuits are connected. If no obstacles exist, the minimum length requirement for the first and last segment is constrained by the design rules that determine the distance between a cell and a via, which are technology dependent. For the remaining segments, the distance can be set to zero. Additionally, the upper bound can be changed as desired without altering the proposed methodology.

The corresponding electrical model of the line is shown in Fig. 3. The total resistance and capacitance of a horizontal (vertical) segment i (v_i) is $R_{i(vi)} = r_{i(vi)} l_{i(vi)}$ and $C_{i(vi)} = c_{i(vi)} l_{i(vi)}$, where $r_{i(vi)}$ and $c_{i(vi)}$ denote the resistance and capacitance, respectively, per unit length. The driver is modeled as a step input voltage and a linear resistance R_S, and the load stage as a capacitive load C_L. The Elmore delay of the line in matrix form is

$$T(\mathbf{l}) = 0.5\, \mathbf{l}^{\mathrm{T}} \mathbf{A} \mathbf{l} + \mathbf{b} \mathbf{l} + D \,, \tag{3}$$

where

$$\mathbf{l} = \begin{bmatrix} l_1 & l_2 & \cdots & l_{n-1} & l_n \end{bmatrix}^{\mathrm{T}} , \tag{4}$$

$$\mathbf{A} = \begin{bmatrix} r_1 c_1 & r_1 c_2 & \cdots & r_1 c_n \\ \vdots & \vdots & \cdots & \vdots \\ r_1 c_n & r_2 c_n & \cdots & r_n c_n \end{bmatrix} , \tag{5}$$

$$\mathbf{b} = \begin{bmatrix} r_1 \left(\sum_{i=1}^{n-1} c_{vi} l_{vi} + C_L \right) + c_1 R_S \\ \vdots \\ r_n C_L + c_n \left(R_S + \sum_{i=1}^{n-1} r_{vi} l_{vi} \right) \end{bmatrix}^{\mathrm{T}} , \tag{6}$$

$$D = R_S \sum_{i=1}^{n-1} c_{vi} l_{vi} + C_L \sum_{i=1}^{n-1} r_{vi} l_{vi} + \frac{1}{2} \sum_{i=1}^{n-1} r_{vi} c_{vi} l_{vi}^2 + R_S C_L \ . \qquad (7)$$

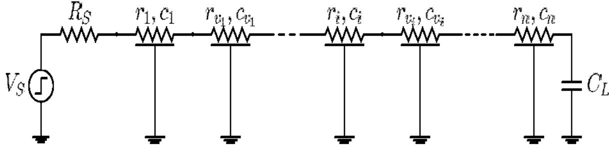

Figure 3. Interlayer interconnect model composed of a set of non-uniformly distributed *RC* segments.

Since (7) is a constant quantity, the optimization problem can be described as follows,

(P) **min.** $T(\mathbf{l}) = 0.5\ \mathbf{l}^{\mathrm{T}}\mathbf{A}\mathbf{l} + \mathbf{b}\mathbf{l}$

subject to (1) and (2).

The primal problem (P) is a quadratic programming problem, which in general is not convex. Applying a variable transformation, (P) is converted to a convex optimization problem [14]. Problem (P) can be effectively solved through geometric programming [15]. In the following section, simulation results and a comparison with a wire sizing algorithm in terms of the delay and power consumption are presented.

IV. SIMULATION RESULTS

In this section, the improvement in delay and the decrease in power consumption achieved by optimally placing the vias are demonstrated. The interlayer interconnects for various numbers of physical planes are analyzed. The impedance characteristics of the horizontal segments and vias are extracted for several interconnect structures using a commercial impedance extraction tool [16]. Based on the extracted impedances, the resistance and capacitance of the horizontal segments range from 5 Ω/mm to 25 Ω/mm and from 100 fF/mm to 300 fF/mm, respectively. Copper interconnect has been assumed. For each horizontal segment, the lower bound in (2) is randomly generated. For simplicity, all of the vias connect the segments of two adjacent physical planes. The delay of the line, where the total line length is divided equally among the horizontal segments, is compared to the line delay where the vias are optimally placed. These via locations or, alternatively, the length of the horizontal segments are obtained solving (P) with a generic optimization solver YALMIP that also supports geometric programs [17].

SPICE delay measurements are reported in Table 1. Note that the variation in delay improvement changes significantly for the listed instances even when the interconnect lengths are similar. Depending upon the impedance characteristics of the line segments, the equally spaced via placement is a near optimal case for certain instances, explaining why the delay improvement is not significant for those instances. From Table 1, delay improvements of up to 26% are observed for relatively short interconnects.

TABLE I. Delay savings by optimum via placement. The resistance and capacitance per unit length of the vias is r_{vi} = 6.7 Ω/mm and c_{vi} = 6 pF/mm, respectively. The length of the vias is l_{vi} = 20 μm. The driver resistance is R_S = 15 Ω and the load capacitance is C_L = 50 fF.

Length [mm]	T_{el} (equally spaced) [ps]	T_{el}^* [ps]	Improvement [%]	*n*
1.560	56.11	52.40	7.08	10
1.609	58.78	53.15	10.59	10
2.383	75.00	64.11	16.99	10
1.665	60.36	50.10	20.48	10
1.749	63.10	52.42	20.37	10
1.233	35.92	33.11	8.49	7
1.167	34.97	31.43	10.12	7
1.132	34.26	30.28	11.62	7
1.933	45.23	34.65	23.39	7
1.716	46.18	37.18	19.49	7
2.428	29.03	23.89	17.71	4
1.875	44.28	38.73	12.53	4
2.121	34.56	25.62	25.86	4
3.429	56.11	42.47	24.31	4
1.701	27.34	25.69	6.03	4
Average Improvement			15.67	

Wire sizing is a well-known technique to reduce the interconnect delay. Wire shaping, however, is not always feasible due to routing congestion or obstacles such as placed cells. Additionally, as the interconnect is tailored to lower the interconnect resistance, the capacitance and, consequently, the power consumption of the interconnect increases. The wire sizing algorithm described in [18] has been applied to several interconnects to improve the line delay. The interconnect length is divided equally among the horizontal segments that constitute the interconnect. For the same interconnects, the line delay where the width is minimum and the vias are optimally placed is also determined.

In Fig. 4, the average interconnect delay for the optimum via placement and wire sizing technique is shown. The instance where the optimum via placement outperforms wire sizing (and vice versa) is depicted. The average delay improvement ranges from 6.23% for n = 4 to 17.8% for n = 5, justifying that via placement can reduce delay in interlayer interconnects in 3-D circuits without requiring additional area. The primary reason wire sizing does not significantly reduce delay is due to the via impedance characteristics and because the vias cannot be sized as aggressively as the horizontal segments. Furthermore, via sizing is not desirable as wider vias decrease the via density or, equivalently, the number of interlayer interconnects that can be routed throughout the 3-D system. In Fig. 5, the normalized average power consumption (NAPC) for various interconnects is illustrated. The crosshatched bar corresponds to interconnects of minimum width and horizontal segments of equal length. The white bar considers those interconnects where the horizontal segments are of equal length and wire sizing has been applied. The NAPC where the line segments are of minimum width and optimum length is depicted by the gray bar. The proposed technique exhibits a lower power consumption as compared to the other two cases. The aforementioned wire sizing increases the capacitance of the

line, resulting in a greater NAPC than the optimum via placement technique. Note that although the NAPC is the lowest for optimally placing the vias, the capacitance and therefore the NAPC is not minimum as the time constant for the interconnect also depends upon the resistance of the line. Due to this dependency, the capacitance is not minimized to avoid an increase in the interconnect resistance. Note that the reduction in NAPC is of considerable importance due to pronounced thermal effects in 3-D circuits [19].

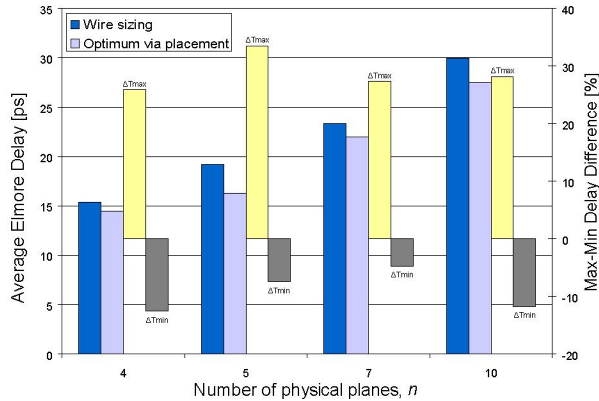

Figure 4. Comparison of the average Elmore delay based on wire sizing and optimum via placement techniques. The instance where the optimum via placement performs the best as compared to wire sizing (and vice versa) is also depicted.

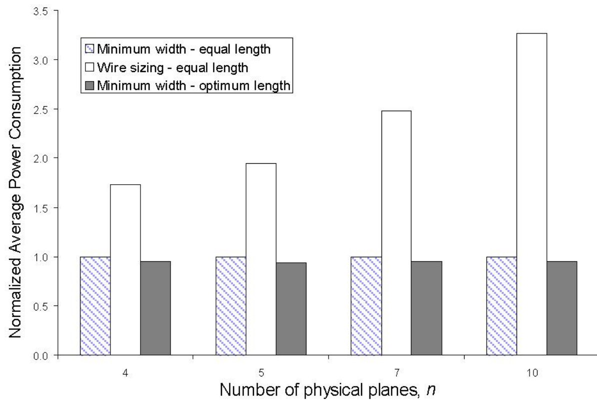

Figure 5. Normalized average power consumption for minimum width and equal length, wire sizing and equal length, and minimum width and optimum via placement.

V. Conclusions

The delay savings resulting from optimally placing the vias between the interlayer interconnects of 3-D circuits is explored. Simulation results indicate that optimum via placement considerably lowers the interconnect delay. In addition, the delay improvement occurs with no additional area cost and with a decrease in power consumption as compared to wire sizing techniques, supporting via placement as a useful delay reduction technique in the design of 3-D circuits.

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