Design Methodology for Global Resonant H-Tree Clock Distribution Networks

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***Abstract* — Design guidelines for resonant H-tree clock distribution networks are presented in this paper. A distributed model of a two level resonant H-tree is presented, supporting the design of low power, low skew, and low jitter resonant H-tree clock distribution networks. Excellent agreement is shown between the proposed model and SpectraS simulations. A case study is presented that demonstrates the design of a two level resonant H-tree network, distributing a 5 GHz clock signal in a TSMC 0.18 µm CMOS technology. The design methodology enables tradeoffs among design variables to be examined, such as the operating frequency, size of the on-chip inductors and capacitors, the output resistance of the driving buffer, and the interconnect width.**

***Index Terms*— Resonance, clock distribution networks, on-chip inductors and capacitors, H-tree sector.**

I. INTRODUCTION

CLOCK signals in digital systems are simultaneously distributed to physically remote locations across an integrated circuit (IC) [1-3]. A clock signal is usually distributed from a common global source through metal interconnect networks and clock drivers, dissipating power. The capacitive load of the clock distribution network can be significant, requiring a large numbers of buffers distributed throughout the network. All of the stored energy in the capacitor is lost as heat.

To dissipate less power, clock generation and distribution networks based on *LC* oscillators in the form of transmission line systems have been considered. In salphasic clock distribution networks [4], a sinusoidal standing wave is established within a transmission line. Coupled standing oscillators of this type are used in [5] to distribute a high frequency clock signal. A similar approach uses traveling waves in coupled transmission line loops [6] driven by distributed cross coupled inverters. In [8,9], a resonant global clock distribution network is described where on-chip spiral inductors and decoupling capacitors are connected to traditional clock trees.

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A comprehensive, constraint free, and robust design methodology for resonant H-tree clock distribution networks is presented in this paper. The methodology is based on the transfer function of a two level H-tree, defined here as a sector, such that the fundamental harmonic of the input square wave is transferred to the output. The output signal at the leaf nodes exhibits a sinusoidal behavior. Inverters are placed at the leaf nodes to convert the sinusoidal waveform into a quasi-square waveform. On-chip spiral inductors and capacitors are used to resonate the clock signal around the harmonic frequency.

This paper is organized as follows: the background and problem formulation of the resonant clock network are presented in section II. In section III, design guidelines are provided. In section IV, a case study is presented. Finally, some conclusions are offered in section V.

II. BACKGROUND AND PROBLEM FORMULATION

The concept of exploiting resonant transmission lines was first introduced by Chi in 1994 [4]. A global resonant clock distribution network was later introduced in 2003 by Chan *et al.* [7]. In this circuit, a set of discrete on-chip spiral inductors and capacitors is attached to a traditional H-tree structure, as depicted in Figure 1. On-chip spiral inductors are connected at four points in the tree, while decoupling capacitors are attached to the other side of the spiral inductors.

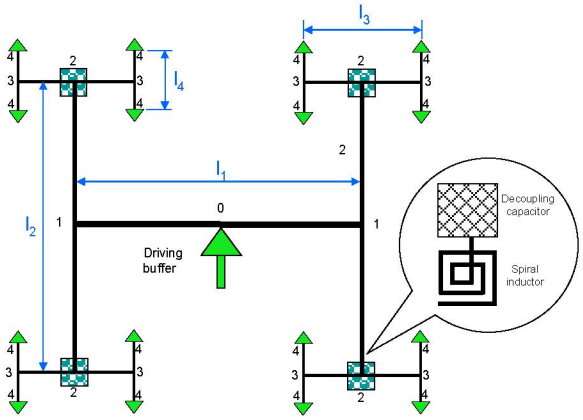


Figure 1. H-tree sector with on-chip inductors and capacitors

The capacitance of the clock distribution network resonates with the inductance, while the on-chip capacitors establish a mid-rail DC voltage around which the grid oscillates. This approach lowers the power consumption, since the energy resonates between the electric and magnetic fields rather than dissipated as heat. Consequently, the number of gain stages is

reduced, resulting in further reductions in power consumption, skew, and jitter.

In this paper, a resonant sector (such as the network shown in Figure 1) is used as a building block, in a modular sense, to construct a much larger global clock distribution network. In this example, the entire network is divided into sectors of 16 leaves. Hence, the design flow is bottom to top, starting with the H-tree sectors at the leaf portion of the tree network and moving up to the central sector.

The design methodology considers the physical geometry of the structure and the technology, and can be formulated as

$$\text{H-Tree Sector} = f\left(w_i, l_i, h_i, f_o, C_l\right) \ \forall i, \qquad (1)$$

where w_i, l_i, and h_i are the width, length, and thickness of each section of the H-tree sector, respectively, f_o is the clock frequency, and C_l is the capacitive load at each leaf node. The index i varies between one and four, representing each section of the H-tree sector (see Figure 1). The H-tree sector function is used to determine the value of the on-chip spiral inductors (considering the effective series resistance), capacitors, and driving buffer resistance that produces the minimum power consumption.

III. Design Guidelines for H-Tree Sector

A methodology for designing resonant H-tree clock distribution networks is described in this section. In section III-A, a distributed model is presented for the H-tree sector. Applying the proposed model and a graphical representation of the design space, the optimum value of the on-chip inductors, capacitors, and output resistance of the driving buffer for minimum power consumption is determined as described in section III-B.

A. H-Tree Sector Model

The proposed model is based on a two level H-tree network as depicted in Figure 1. The distributed *RLC* network shown in Figure 2 represents the clock tree depicted in Figure 1. The parameters R_i, L_i, and C_i are the resistance, inductance, and capacitance per unit length, respectively, where i varies from one through four. The parameter N is the depth of the tree, which in the example shown in Figure 1 equals four, while the number of leafs is 2^N.

Since all of the nodes labeled 1 in Figure 1 are symmetric, the waveforms at these nodes are assumed to be identical, and as a result, can be assumed to be shorted together [9]. The same assumption applies to nodes 2, 3, and 4. This simplification is exploited to transform the circuit shown in Figure 2 into a distributed *RLC* transmission line as shown in Figure 3, making the analysis considerably simpler. Since the interconnect lines between each pair of nodes are assumed to be connected in parallel, the capacitance per unit length is increased by approximately a factor of two, while the resistance and inductance per unit length is decreased by a factor of two at each level of the hierarchy. An analytic model of this structure is developed based on *ABCD* parameters [10].

From transmission line theory, the *ABCD* matrix for the overall structure is a product of the individual matrices,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = M_1 \cdot M_2 \cdot M_s \cdot M_3 \cdot M_4 \cdot M_l, \qquad (2)$$

where M_i (i = 1..4), M_s, and M_l are the *ABCD* matrix of the four sections, the on-chip inductors and capacitors, and the load, respectively.

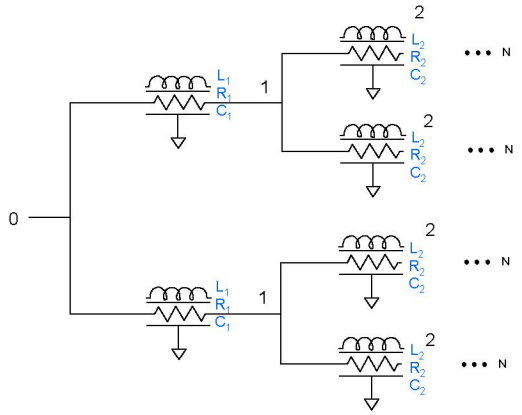


Figure 2. Distributed *RLC* network representation of an H-tree

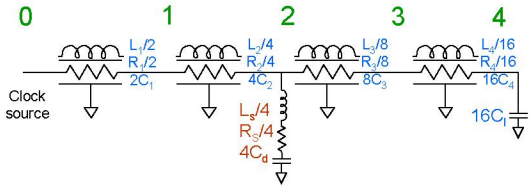


Figure 3. Resonant H-tree network simplified to a distributed *RLC* line

From the overall *ABCD* parameters, the transfer function $H(s)$ and input impedance $Z(s)$ of the system is, respectively,

$$H(s) = \frac{1}{A} = K(s) \cdot \frac{a_2 \cdot s^2 + a_1 \cdot s + a_0}{b_3(s) \cdot s^3 + b_2(s) \cdot s^2 + b_1(s) \cdot s + b_0(s)} \qquad (3)$$

$$Z_{in}(s) = \frac{A}{C} = \frac{b_3(s) \cdot s^3 + b_2(s) \cdot s^2 + b_1(s) \cdot s + b_0(s)}{d_3(s) \cdot s^3 + d_2(s) \cdot s^2 + d_1(s) \cdot s + d_0(s)}, \qquad (4)$$

where a_0, a_1, and a_2 are constants and the parameters K, b_0, b_1, b_2, b_3, d_0, d_1, d_2, and d_3 are functions of frequency, the geometry of the structure, and the on-chip inductors and capacitors. These functions can be determined from (2) and the corresponding M matrices.

B. On-Chip Inductor, Capacitor, and Output Resistance of the Driving Buffer

Since the transmission line network of the resonant H-tree is a passive linear network (assuming the inverter at the leaf node is modeled as a constant gate capacitance), a one-port network, as depicted in Figure 4, is used to model the H-tree sector.

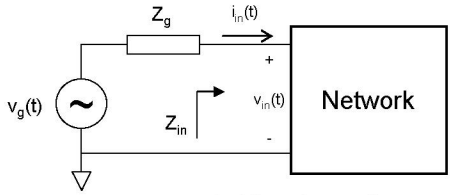


Figure 4. One-port network driven by a voltage source

The driving buffer of the resonant clock tree is modeled as a voltage source $V_g(t)$ with a finite output impedance. The output impedance of the voltage source Z_g and the input impedance of the network Z_{in} can be expressed, respectively, as

$$Z_g = R_g + jX_g, \tag{5}$$

$$Z_{in} = R_{in} + jX_{in}. \tag{6}$$

The rate at which energy is absorbed is the power, given by [11]

$$P_{net} = \frac{1}{2} V_{rms,g}^2 \cdot \rho, \tag{7}$$

where ρ is the real part of the input admittance of the H-tree sector,

$$\rho = \frac{R_{in}}{\left(R_{in} + R_g\right)^2 + \left(X_{in} + X_g\right)^2}. \tag{8}$$

Note from (7) that in order to reduce the power consumption P_{net}, ρ should be made smaller. A second constraint is that the magnitude of the transfer function should be equal to or greater than 0.9 at the operating frequency in order to achieve full swing at the output. To justify a value of 0.9, consider a Fourier series representation of a periodic square waveform $x(t)$ with an amplitude of V_{DD},

$$x(t) = \sum_{k=-\infty}^{\infty} a_k e^{jk\omega_0 t}, a_k = V_{DD} \frac{1}{\pi k} \sin\left(k\omega_0 T_1\right), \tag{9}$$

where ω_0 is the radian frequency, and T_1 is a quarter of the period of the square wave. Since the transfer function of the H-tree sector at resonance is designed to transfer the fundamental harmonic of the square wave, consider the elements $k = \pm 1$ in (8),

$$a_{\pm 1} = V_{DD} \frac{1}{\pi}. \tag{10}$$

From (10), the amplitude transferred to the output therefore equals $V_{DD} \cdot (2/\pi)$. The required sinusoidal amplitude at the output is 1 volt (swinging around 0.9 volts) to allow the buffers at the leaf nodes to charge and discharge the load at frequencies as high as 5 GHz in a 0.18 µm CMOS technology. From this discussion, the required peak value of the magnitude of the transfer function is

$$\left|H'\left(j\omega_0\right)\right| = \frac{\pi}{2V_{DD}} = \frac{\pi}{2 \cdot 1.8} \approx 0.9. \tag{11}$$

These design constraints for a resonant H-tree network are summarized in (12). Since the power consumption is inversely proportional to the output resistance, (8) suggests that the output resistance of the driving buffer should be maximized.

$$\begin{cases} \min\left(P_{net}\right) & \text{(12a)} \\ \max\left(R_g\right) & \text{(12b)} \\ \left|H'\left(j\omega_0\right)\right| \geq 0.9. & \text{(12c)} \end{cases}$$

In (12c), $|H'(j\omega)|$ is

$$\left|H'(j\omega)\right| = \sqrt{\frac{R_{in}^2 + X_{in}^2}{\left(R_g + R_{in}\right)^2 + \left(X_g + X_{in}\right)^2}} \cdot \left|H(j\omega)\right|, \tag{13}$$

where $|H(j\omega)|$ is described in (3) in the S-domain.

The three conditions in (12) can be used to determine the optimal value of the on-chip inductors, capacitors, and driving buffer resistance that produces a full swing sinusoidal waveform while dissipating minimum power. Since the closed-form analytic expressions for the input impedance and the transfer function, given by (3) and (4), are somewhat cumbersome, the solution to (12) is graphically evaluated. In this manner, the design space and related tradeoffs among the different parameters can be explored.

Three design variables, L_s, C_d, and R_g, are solved simultaneously to satisfy (12). In order to graphically represent the design space, one of the three design variables is eliminated. Equating $|H'(j\omega)|$ to 0.9 and solving for R_g (assuming $X_g = 0$),

$$R_g = \left(\sqrt{\frac{\left|H(j\omega)\right|^2}{0.9^2} \cdot \left(R_{in}^2 + X_{in}^2\right) - X_{in}^2} \right) - R_{in}. \tag{14}$$

Substituting (14) into (8) yields

$$\rho = \frac{0.9^2 \cdot R_{in}}{\left|H(j\omega)\right|^2 \cdot \left(R_{in}^2 + X_{in}^2\right)}. \tag{15}$$

Note from (15) that ρ is only a function of the on-chip spiral inductor and capacitor at a specific frequency.

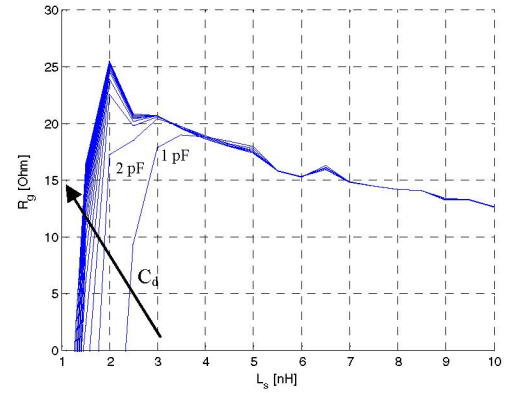
IV. Case Study

In this section, a 5 GHz resonant H-tree sector is designed as a basic building block of a large global clock distribution network. The design guidelines and principles presented in section III are demonstrated in this case study. The case study is based on a TSMC 0.18 µm CMOS technology. The resistance, inductance, and capacitance per unit length of the transmission lines are extracted using HENRY™ and METAL™ from the OEA software suite [12].

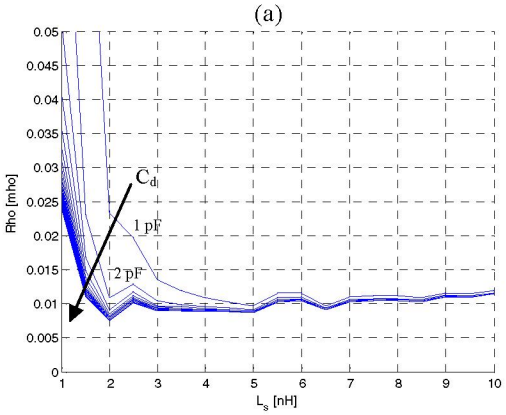
Expressions (14) and (15) at a 5 GHz operating frequency as a function of the spiral inductance are plotted in Figure 5 over a wide range of capacitance values (1 pF through 40 pF). In order to satisfy condition (12a), the spiral inductance is chosen to be L_s = 2 nH, thereby minimizing ρ and maximizing R_g, as evident from Figure 5. Consequently, the maximum output resistance is $R_g \approx 25\ \Omega$ and the corresponding on-chip capacitor is C_d = 15 pF.

The output waveform at the leaf nodes described in the time domain is shown in Figure 6. Note that the square clock waveform is distributed to the leaf node, achieving a full rail-to-rail voltage swing. Also note that the output waveform exhibits a quasi-sinusoidal characteristic which is common even in non-resonant multi-gigahertz clock distribution networks [7].

In the frequency domain, the magnitude of the transfer function and input impedance around a 5 GHz operating frequency is shown in Figure 7. Good agreement between simulation results and the proposed analytic expressions is achieved, exhibiting less than 5% error. Note that the peak magnitude (= 0.9) at 5 GHz maximizes the output resistance of the driving buffer. As predicted by the design expressions and verified by simulation, the power consumption in this example is $P_{net} \approx$ 15 mW (including buffers) as compared to a nonresonant H-tree sector, where the power consumption is 93 mW (84% greater than the resonant circuit).



(a)



(b)

Figure 5. Design tradeoffs for an H-tree sector: (a) Output resistance as a function of the spiral inductor, (b) ρ as a function of the on-chip spiral inductor

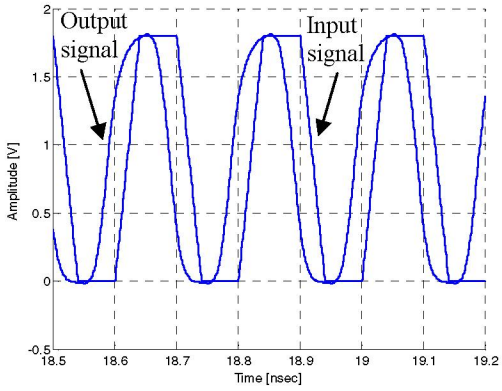


Figure 6. Output waveform at the leaf nodes

Note that by eliminating the need for buffers in a resonant clock network, significant power savings can be achieved. In Figure 8, the power consumption as a function of the size of the on-chip inductors as expressed by (7) is shown.

Also note that the maximum resistance of the output buffer is determined for each value of inductance. Good agreement between simulation and (7) is illustrated, exhibiting less than 10% error. As indicated in Figure 8, the minimum power consumption for the circuit illustrated in Figure 1 is about 5 mW (not including buffers at the leaf nodes).

V. CONCLUSIONS

A methodology is described for designing resonant H-tree clock distribution sectors. These H-tree structures form the basic building block of a resonant network. An accurate model is developed which utilizes transmission line theory to characterize high frequency effects. The high accuracy and analytic nature of the model enables the exploration of tradeoffs in the design of a resonant H-tree sector. The optimal on-chip inductors and capacitors as well as the maximum allowable driving buffer output resistance are determined for a specific example circuit. This set of impedances produces the minimum power while satisfying the specified clock frequency.

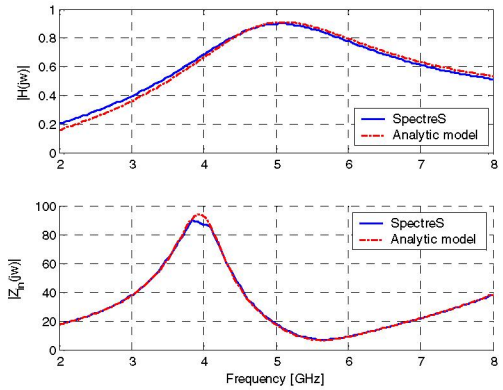


Figure 7. Magnitude of transfer function and input impedance

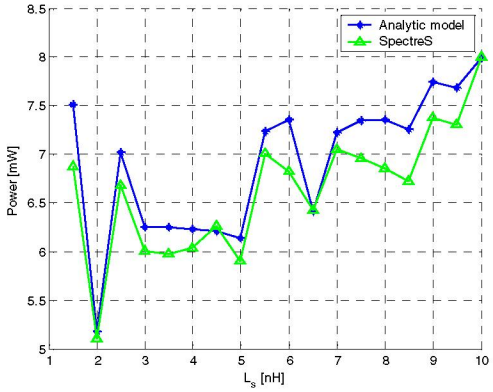


Figure 8. Comparison of power consumption between analytic model and SpectreS Spice simulation

REFERENCES

[1] E. G. Friedman, "Clock Distribution Networks in Synchronous Digital Integrated Circuits," *Proceedings of the IEEE*, Vol. 89, No. 5, pp. 665-692, May 2001.

[2] E. G. Friedman, *High Performance Clock Distribution Networks*, Kluwer Academic Publishers, 1997.

[3] S. Sauter, D. Schmitt-Landsiedel, R. Thewes, and W. Weber, "Effect of Parameter Variations at Chip and Wafer Level on Clock Skews," *IEEE Transaction on Semiconductor Manufacturing*, Vol. 13, No. 4, pp. 395-400, Novermber 2000.

[4] V. L. Chi, "Salphasic Distribution of Clock Signals for Synchronous Systems," *IEEE Transaction on Computers*, Vol. 43, No. 5, pp. 597-602, May 1994.

[5] F. O. Mahony, C. P. Yue, M. A. Horowitz, and S. S. Wong, "A 10-GHz Global Clock Distribution Using Coupled Standing-Wave Oscillators," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 11, pp. 1813-1820, November 2003.

[6] J. Wood, T. C. Edwards, and S. Lipa, "Rotary Traveling-Wave Oscillator Arrays: A New Clock Technology," *IEEE Journal of Solid-State Circuits*, Vol. 36, No. 11, pp. 1654-1665, November 2001.

[7] S. C. Chan, K. L. Shepard, and P. J. Restle, "Design of Resonant Global Clock Distributions," *Proceedings of the IEEE International Conference on Computer Design*, pp. 248-253, October 2003.

[8] S. C. Chan, K. L. Shepard, and P. J. Restle, "Uniform-phase, Uniform-amplitude, Resonant-Load Global Clock Distributions," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 1, pp. 102-109, January 2005.

[9] H. B. Bakoglu, *Circuits, Interconnections, and Packaging for VLSI*, Addison-Wesley Publishing Company, 1990.

[10] D. M. Pozar, *Microwave Engineering*, Addison-Wesley Publishing Company, 1990.

[11] M. E. Van Valkenburg, *Network Analysis*, Prentice-Hall Inc., 1974.

[12] http://www.oea.com