Effective Capacitance of RLC Loads for Estimating Short-Circuit Power

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***Abstract*— An effective capacitance of a distributed RLC load for estimating short-circuit power is presented in this paper. Both resistive and inductive shielding effects of interconnects are considered and no iterations are required to determine the effective capacitance. The proposed method has been verified with Cadence Spectre. For a single switching input, the average error of the short-circuit power obtained with the effective capacitance is less than 2% for the example circuits as compared with an RLC π model. The proposed method can be used in look-up table or k-factor based models to estimate short-circuit power dissipation in CMOS gates with complex interconnects.**

I. Introduction

With CMOS technology scaling, power has become an important design criterion in integrated circuits due to the increasing number of portable applications. Furthermore, high power dissipation can generate significant heat which limits performance and increases cooling costs. A capability of accurately and efficiently estimating power is therefore needed in the circuit design process.

As compared with dynamic power which is well characterized, short-circuit power is more difficult to model due to the complicated transient behavior of the short-circuit current. In [1], Veendrick developed a closed form expression for short-circuit power dissipation in an unloaded CMOS inverter. More accurate analyses have recently been presented by including both short-channel effects and output overshoot effects [2], [3]. In these analyses, a lumped capacitor is assumed as the load. In [4], an RC π model is adopted as the load to characterize the shielding effect of the interconnect resistance. An effective capacitance of the RC π structure for short-circuit power estimation is described in [5] to maintain compatibility with popular look-up table or k-factor based power models. With increasing on-chip frequencies and longer interconnects, the interconnect inductance also needs to be considered. As described in [6], the interconnect inductance also exhibits a shielding effect on the load capacitance, increasing the short-circuit power dissipated by the driver.

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In this paper, an effective capacitance of an RLC load is developed to accurately estimate short-circuit power. Both resistive and inductive shielding effects are considered. The paper is organized as follows. In section II, a distributed RLC network is reduced into a π model. From this π model, the effective capacitance is determined. In section III, the proposed effective capacitance model is verified by Cadence Spectre simulations. Finally, some conclusions are offered in section IV.

II. Effective Capacitance of an RLC Load

As technology progresses, interconnect networks have become increasingly complicated. One efficient method for analyzing interconnect is the model order reduction technique. This technique has demonstrated significant efficiency in the timing and power analysis process. In section II-A, a π model is generated from a distributed RLC tree, which is further reduced into an effective capacitance in section II-B.

A. Model order reduction

By matching the first three moments (y_1, y_2, and y_3) of the admittance at the driving point, an RC network can be reduced into an RC π model [7]. In the same way, an RLC network can be reduced into an RLC π model by matching the first four moments. This reduction, however, can be unrealizable (the value of the circuit element is not positive real). In order to obtain a realizable RLC π model, a new coefficient y_3^* is introduced in [8], which is the third order admittance moment (without considering inductance). By matching y_1, y_2, y_3, and y_3^*, the π model parameters can be obtained as [8]

$$C_f = y_2^2/y_3^*, \tag{1}$$

$$C_n = y_1 - C_f, \tag{2}$$

$$R_\pi = -y_2/C_f^2, \tag{3}$$

$$L_\pi = (y_3^* - y_3)/C_f^2, \tag{4}$$

where C_n and C_f denote the near end and far end capacitance, respectively.

The input admittance of a distributed RLC interconnect with a load admittance Y_l is [9]

$$Y(s) = \frac{Z_c Y_l + \tanh\theta}{Z_c(1 + Z_c Y_l \tanh\theta)}, \tag{5}$$

where $\theta = \sqrt{(R+sL)sC}$ and $Z_c = \frac{\theta}{Cs}$. R, C, and L are the total resistance, capacitance, and inductance of the

interconnect, respectively. By expanding $Y(s)$ into a Taylor series of s around zero, the moments at the input of the RLC interconnect can be obtained as

$$y_1 = y_{l,1} + C, \tag{6}$$

$$y_2 = y_{l,2} - R(y_{l,1}^2 + y_{l,1}C + \frac{1}{3}C^2), \tag{7}$$

$$\begin{aligned} y_3 = {} & y_{l,3} - R(2y_{l,1}y_{l,2} + y_{l,2}C) \\ & + R^2(y_{l,1}^3 + \frac{4}{3}y_{l,1}^2C + \frac{2}{3}y_{l,1}C^2 + \frac{2}{15}C^3) \\ & - L(y_{l,1}^2 + y_{l,1}C + \frac{1}{3}C^2), \end{aligned} \tag{8}$$

$$\begin{aligned} y_3^* = {} & y_{l,3}^* - R(2y_{l,1}y_{l,2} + y_{l,2}C) \\ & + R^2(y_{l,1}^3 + \frac{4}{3}y_{l,1}^2C + \frac{2}{3}y_{l,1}C^2 + \frac{2}{15}C^3). \end{aligned} \tag{9}$$

The input admittance moments of a distributed RLC tree can be determined by recursively applying (6)-(9). From these moments and (1)-(4), the corresponding π structure can be obtained.

B. Effective capacitance for short-circuit power

Although a π model is highly accurate, four coefficients are required in this model, making it incompatible with k-factor expressions or look-up table based power models. An effective capacitance greatly simplifies the model with little penalty in accuracy.

The shielding effect of the interconnect resistance is well known and the effective capacitance of RC interconnects has been developed for estimating delay and short-circuit power in [5], [10]. The interconnect inductance however also has a shielding effect [6]. This inductive shielding effect is illustrated with an example (shown in Fig. 1). In Fig. 1, a distributed RLC tree is driven by a 0.18 μm CMOS inverter. The size of the transistors in the inverter is $W_n = 10\,\mu$m and $W_p = 25\,\mu$m. The impedance parameters of the interconnect are $R_{int} = 12.23\,\text{m}\Omega/\mu\text{m}$ and $C_{int} = 0.245\,\text{fF}/\mu\text{m}$. The load capacitance is $C_L = 100\,\text{fF}$. The short-circuit current of the inverter is illustrated in Fig. 2 for different values of interconnect inductance. When the interconnect inductance becomes larger, greater far end capacitance is shielded. Less effective capacitance is therefore seen at the inverter output, permitting the output voltage to change faster at the beginning of the signal transition, thereby producing a larger short-circuit current. The currents are measured at the source of the PMOS transistor with a rising input as shown in Fig. 3. The discontinuity of the waveform is due to the discontinuity of the transistor capacitance model used in the simulation. Strictly speaking, the currents illustrated in Fig. 2 include two non-short-circuit current components. The first component is the current flowing through the capacitance C_{gs}, as shown in Fig. 3. This component can be determined as $I_{gs} = C_{gs}V_{dd}/t_r$ and is independent of the load. The second component is the current I_{ov} flowing from the output to V_{dd} due to the overshoot at the output in the beginning of the signal transition. I_{ov} returns a small amount of charge stored in the output node back to V_{dd}, slightly reducing the dynamic power.

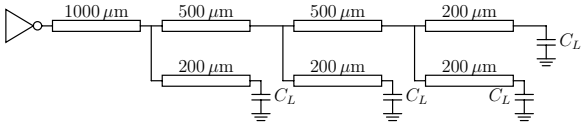

Fig. 1. A distributed RLC tree.

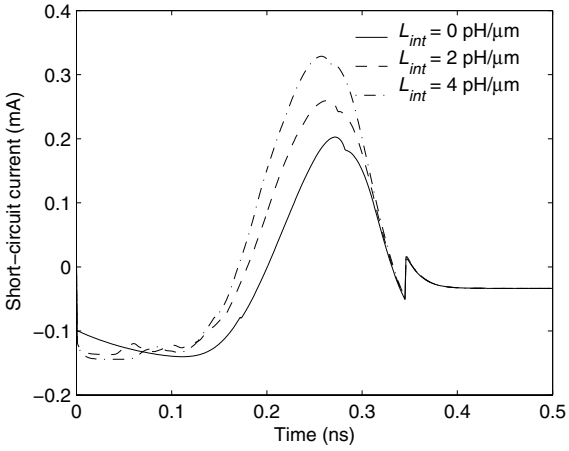

Fig. 2. Effect of inductance on the short-circuit current. $t_r = 0.5\,\text{ns}$.

In [10], the output waveform of a CMOS gate is approximated by a quadratic function followed by a linear function. In this paper, the output waveform of a gate is modeled as a quadratic function during the input transition time. Assuming the output waveform is $v(t) = at^2$ for a rising edge, the current drawn from the gate by an RLC π structure is

$$I_\pi(s) = \frac{2a}{s^3}\left(\frac{C_f s}{1 + R_\pi C_f s + L_\pi C_f s^2} + C_n s\right). \tag{10}$$

Applying an inverse Laplace transformation to (10), the current in the time domain is

$$i_\pi = 2aC_f(-R_\pi C_f + t + k_1 e^{s_1 t} + k_2 e^{s_2 t}) + 2aC_n t, \tag{11}$$

where

$$s_{1,2} = \frac{-R_\pi \pm \sqrt{R_\pi^2 - 4L_\pi/C_f}}{2L_\pi}, \tag{12}$$

$$k_1 = \frac{1}{s_1^2(s_1 - s_2)L_\pi C_f}, \tag{13}$$

$$k_2 = \frac{1}{s_2^2(s_2 - s_1)L_\pi C_f}. \tag{14}$$

The current drawn from the gate by an effective capacitance is $i_{ceff} = 2aC_{eff}t$. Equating the average of i_π and i_{ceff} during a period from 0 to an evaluation time t_{ev}, C_{eff} can be obtained as

$$\begin{aligned} C_{eff} = {} & C_n + C_f\left[1 - \frac{2R_\pi C_f}{t_{ev}} + \right. \\ & \left. \frac{2k_1}{t_{ev}^2 s_1}(e^{s_1 t_{ev}} - 1) + \frac{2k_2}{t_{ev}^2 s_2}(e^{s_2 t_{ev}} - 1)\right]. \end{aligned} \tag{15}$$

The effective capacitance $C_{eff\text{-}RC}$ for an RC π structure can be similarly determined. As expected, C_{eff} is between C_n

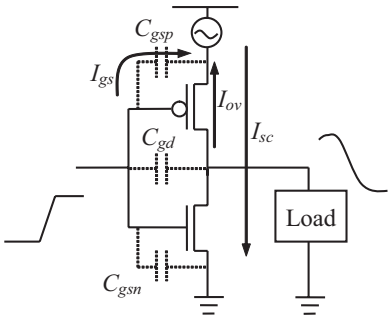

Fig. 3. Current components in a CMOS inverter.

and $C_n + C_f$. From (15), C_{eff} is a function of t_{ev} as shown in Fig. 4. The π model parameters are obtained from the tree structure as shown in Fig. 1 with $L_{int} = 0.74\,\text{nH}/\mu\text{m}$. With increasing t_{ev}, C_{eff} increases from C_n and approaches $C_n + C_f$. In [10], t_{ev} is the time when the driver output achieves 50% of V_{dd}, which is the objective and is not known *a priori*. Several iterations are therefore required to determine C_{eff}. In [5], t_{ev} is determined as the end point of the short-circuit period. Since the short-circuit current exists when the input is between V_{thn} and $V_{dd} + V_{thp}$, the evaluation time t_x is in the range from 0 to $t_r(1 - \frac{|V_{thp}|}{V_{dd}} - \frac{V_{thn}}{V_{dd}})$. Note that $t = 0$ corresponds to the time when the input reaches V_{thn} for a rising edge ($V_{dd} + V_{thp}$ for a falling edge). As shown in Fig. 4, for the time period $0 < t < t_x$, the effective capacitance is overestimated and the short-circuit current is underestimated. For the period $t_x < t < t_r(1 - \frac{|V_{thp}|}{V_{dd}} - \frac{V_{thn}}{V_{dd}})$, the effective capacitance is underestimated and the short-circuit current is overestimated. By properly adjusting t_x, the estimation error of the short-circuit current in different time regions can be canceled. By comparing Spectre simulations, a fitting parameter is adopted to determine t_x,

$$t_x = 0.46 t_r (1 - \frac{|V_{thp}|}{V_{dd}} - \frac{V_{thn}}{V_{dd}}). \tag{16}$$

The short-circuit current waveforms for an inverter with different load models are compared in Fig. 5. For this inverter, $V_{thn} = 0.5$ volts and $V_{thp} = -0.5$ volts. As shown in Fig. 5, the π model can accurately characterize a tree structure. The waveform obtained with a π model is indistinguishable from the waveform with the original RLC tree (shown in Fig. 1). Note that unlike C_{eff} for estimating the delay [10], C_{eff} for short-circuit power estimation is independent of the transistor size.

III. Model Verification

For the example shown in Fig. 1, the short-circuit energy dissipated over a full signal transition for different loads is compared in Fig. 6. As shown in Fig. 6, the total capacitance always underestimates the short-circuit energy as compared with a distributed RLC tree. For example, the error for $t_r = 0.5\,\text{ns}$ is 28.1%. More accurate estimations can be obtained with C_{eff_RC} (only considering the resistive shielding effect) and C_{eff} (considering both resistive and inductive shielding

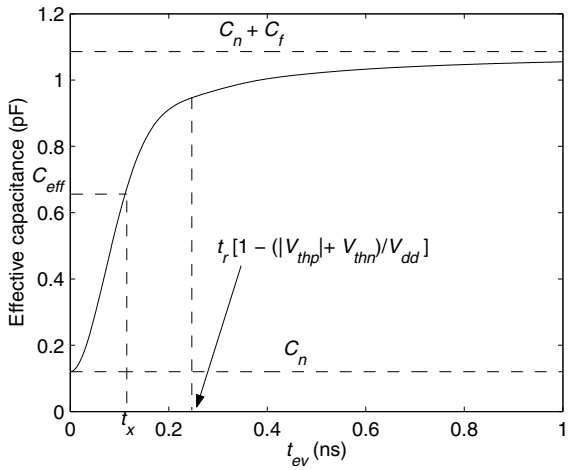

Fig. 4. Effective capacitance as a function of t_{ev}. $C_n = 120.1\,\text{fF}$, $C_f = 965.9\,\text{fF}$, $R_p = 15.9\,\Omega$, and $L_p = 0.96\,\text{nH}$.

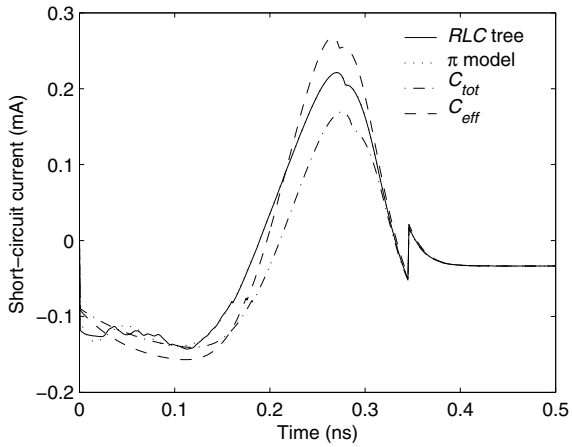

Fig. 5. Short-circuit current with different output loads.

effects). The inductive shielding effect is most important for this example in the range from $t_r = 0.2\,\text{ns}$ to $t_r = 0.8\,\text{ns}$. When t_r is sufficiently large, the driver output has sufficient time to converge to the RC response [11], making the shielding effect of the inductance negligible. If t_r is too small, although the effect of the inductance on the output voltage waveform is large, the duration of the short-circuit current period is small, making the total short-circuit power insignificant. Since dynamic power is usually determined as $\alpha f V_{dd}^2 C_{load}$ (where α is the switching factor), the reduction P_{red} in dynamic power due to I_{ov} is considered part of the short-circuit power such that the summation of the two power components (dynamic and short-circuit) can represent the total transient power. With fast inputs, P_{red} can dominate the short-circuit power, producing a negative short-circuit power, as shown in Fig. 6. Since P_{red} can not be characterized by C_{eff}, the error of the power estimation is greater for fast inputs.

The effective capacitance concept can also be applied to other logic gates, such as NAND and NOR gates. The short-circuit energy consumed by an inverter and a two input NAND

TABLE I

SHORT-CIRCUIT ENERGY DISSIPATION (pJ) DURING A FULL SIGNAL SWITCH.

T_r (ns)	$R_\pi/L_\pi/C_n/C_f$ (Ω/nH/fF/fF)	C_{eff} (fF)	Inverter			NAND (upper)			NAND (lower)			NAND (both)		
			π	C_{eff}	C_{tot}	π	C_{eff}	C_{tot}	π	C_{eff}	C_{tot}	π	C_{eff}	C_{tot}
0.5	100/2/200/600	369.4	0.16	0.16	0.11	0.12	0.12	0.08	0.11	0.10	0.07	0.06	0.05	0.02
1	100/2/200/600	517.3	0.45	0.44	0.38	0.35	0.35	0.30	0.36	0.35	0.29	0.30	0.29	0.24
2	100/2/200/600	641.3	1.13	1.13	1.06	0.93	0.93	0.87	0.98	0.97	0.91	0.88	0.86	0.81
0.5	200/3/100/800	205.2	0.20	0.20	0.10	0.15	0.15	0.08	0.14	0.13	0.06	0.09	0.07	0.02
1	200/3/100/800	322.6	0.51	0.51	0.36	0.41	0.41	0.28	0.41	0.41	0.28	0.35	0.34	0.23
2	200/3/100/800	483.3	1.21	1.20	1.01	0.99	1.00	0.83	1.05	1.05	0.87	0.94	0.93	0.78
0.5	300/4/100/300	167.9	0.21	0.21	0.15	0.16	0.16	0.12	0.15	0.14	0.10	0.09	0.08	0.05
1	300/4/100/300	228.8	0.56	0.56	0.48	0.45	0.45	0.38	0.45	0.45	0.38	0.38	0.37	0.32
2	300/4/100/300	292.7	1.34	1.33	1.25	1.11	1.11	1.04	1.16	1.16	1.09	1.03	1.02	0.96
Average % Error			—	0.9	22.1	—	1.2	22.2	—	1.6	24.4	—	7.2	33.5

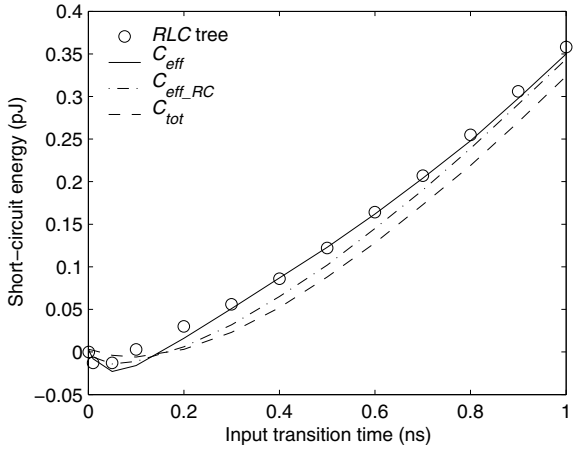

Fig. 6. Short-circuit energy with different loads. $L = 0.74\,\text{pH}/\mu\text{m}$.

gate during a full signal transition is listed in Table I for different inputs and loads. The two inputs of the NAND gate are denoted as the upper input and lower input according to the relative location of the input terminal. Three switching patterns are considered: only the upper input is switched (the lower input is tied to V_{dd}), only the lower input is switched, and both of the two inputs are connected and simultaneously switched. The size of the transistors in the NAND gate is $W_n = 10\,\mu$m and $W_p = 25\,\mu$m. For a single switching input, the average error of the short-circuit power is less than 2% as compared with the π model. The average error with the total capacitance, however, is more than 20% for these examples. As compared to the single switching input, the error with C_{eff} for the connected inputs is greater, exhibiting an average error of 7.2%. For multiple switching inputs with offsets in delay (non-simultaneous input signals), an equivalent input signal has been developed in [12] for estimating short-circuit power. From this equivalent input signal, an effective capacitance can be obtained from (15) and (16).

IV. CONCLUSIONS

Interconnect is highly significant in deep submicrometer integrated circuits. The interconnects not only dominate the overall circuit delay, but also greatly affect power dissipation. In this paper, the effective capacitance of a distributed RLC load is determined in order to accurately estimate short-circuit power by considering the shielding effects of both the interconnect resistance and inductance. This effective capacitance can be used in look-up tables or in empirical k-factor expressions to estimate short-circuit power as well as in analytic approaches to simplify interconnect load models.

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