Optimum Wire Tapering for Minimum Power Dissipation in RLC Interconnects

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Abstract—**The optimum tapered structure for RLC interconnect to minimize transient power dissipation is determined. Wire tapering can reduce the power dissipated by a circuit by up to 72% as compared to uniform wire sizing. An analytic solution to determine the optimum tapered structure exhibits an error of less than 2% as compared to SPICE.**

1. INTRODUCTION

/vspace-0.2cm Interconnect design has become a dominant issue in high speed integrated circuits (ICs). With decreasing feature size in CMOS circuits, the on-chip interconnect dominates both the circuit delay and power dissipation characteristics of high complexity integrated circuits. Different techniques have therefore been developed to enhance circuit performance. Wire sizing has been proposed as a technique to improve circuit performance [1]. Exponential wire tapering is an efficient technique to decrease the signal propagation delay in RC interconnects [2]. Wire tapering increases the interconnect width at the driver end of the line as shown in Fig. 1.

The inductive behavior of the interconnect can no longer be neglected, particularly in long interconnect lines operating at high frequencies. Wire tapering is usually applied to long lines, further increasing the importance of including the line inductance in the optimization process. Exponential tapering is shown in [3] to be the optimum shape function to minimize propagation delay in RLC lines.

Wire sizing can also affect the power dissipated by a circuit [4]. Uniform wire sizing decreases the transition time at the load, reducing the short-circuit power of the load gate [4]. Uniform wire sizing for RLC interconnects can decrease the total power dissipation of a circuit since the power dissipated in the load can be traded off with the power dissipated by the driver [1, 5, 6]. As described in [1, 5, 6], the width of an RLC interconnect can be optimized for minimum power dissipation.

In this paper, RLC wire tapering is shown to reduce the power dissipated by a circuit. An analytic solution to determine the optimum tapering structure that produces the minimum transient power dissipation is provided. Moreover, the efficiency of wire tapering over uniform wire sizing in reducing power dissipation is considered.

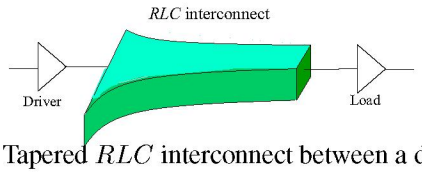

Figure 1: Tapered RLC interconnect between a driver and a load

The paper is organized as follows. In section 2, wire tapering as a criterion to minimize transient power dissipation is presented. An analytic solution to determine the optimum wire shape that produces the minimum power dissipation of an RLC line is characterized in section 3. In section 4, optimum wire tapering is compared with uniform wire sizing for minimum power dissipation. Simulation results are presented in section 5. Some conclusions are provided in section 6.

2. INTERCONNECT TAPERING FOR MINIMUM POWER DISSIPATION

Tapering an interconnect line can decrease the signal transition time at the load, decreasing the short-circuit current in the load gate. As described in [1, 5, 6], the reduction in line resistance (with increasing wire width) decreases the signal attenuation along the line, improving the signal transition time. The same criterion can be used to reduce the power dissipated by a load driven by a tapered interconnect line.

Exponential tapering produces the optimum shape to minimize the propagation delay in RLC interconnects [3]. Exponential tapering can also be used as a sizing technique to decrease the power dissipation. For the circuit shown in Fig. 1, a long (5 mm) interconnect line is used to connect the load (a CMOS inverter) with the driver (a CMOS inverter). The interconnect width is exponentially tapered based on the tapering function $W(x) = qe^{px}$, where $W(x)$ is the line width at a distance x from the load, q is the initial line width at the load, and p is the tapering factor. The signal transition time decreases as the tapering factor p increases. The line becomes less resistive (more inductive) with tapering, reducing the transition time at the load.

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For q = 0.1 μm and 0.2 μm, the power components of the circuit structure shown in Fig. 1 are illustrated in Fig. 2. For increasing tapering factor, the short-circuit power dissipated in the load gate decreases. The power dissipated by the driver increases, since the line capacitance is greater with tapering. A tradeoff, therefore, exists between the short-circuit power dissipated in the load and the dynamic power of the driver in long tapered interconnects. For high values of p, the increase in the driver power is greater than the reduction in the load power. An optimum tapering factor that produces the minimum total transient power dissipation exists in a tapered RLC interconnect. For each value of q, there is an optimum tapering factor p_{opt} at which the total transient power dissipation is minimum.

As q increases, the dynamic power dissipated by the driver increases, changing the optimum tapering factor that produces the minimum power. An optimum initial width q_{opt} exists that produces the minimum power dissipation. q_{opt} and p_{opt} are determined simultaneously. In section 3, an analytic solution that can be used to determine the optimum tapering structure for minimum power is described.

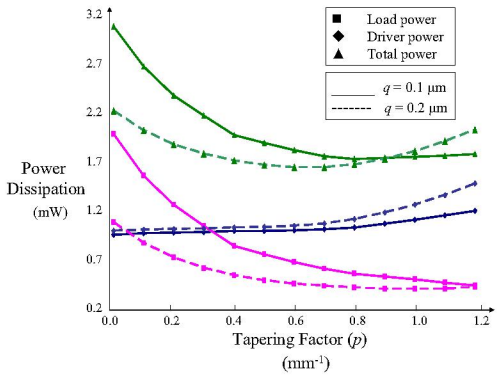

Figure 2: Power dissipation in a load driven by a long tapered RLC interconnect line

3. OPTIMIZATION CRITERION FOR A TAPERED LINE

The work described in [6] provides an analytic solution for the optimum uniform interconnect width that produces the minimum power dissipation. The total transient power dissipation is presented in terms of the uniform interconnect width W_{int}. The uniform width is replaced here with an exponential function qe^{px}. For an inverter driving N gates, the total transient power dissipation $P_t(q,p)$ is a function of the initial line width q and tapering factor p,

$$P_t(q,p) = P_{Driver}(q,p) + N\,P_{Load}(q,p) + P_c, \qquad (1)$$

where P_c is the summation of the dynamic power of the load gate and the short-circuit power of the driver and $P_{Driver}(q,p)$ and $P_{Load}(q,p)$ are the dynamic power of the driver and the short-circuit power of the load, respectively. P_c is a weak function of q and p. P_c is therefore assumed independent of q and p, since the dynamic power of the load gate depends upon the load characteristics and the short-circuit power of the driver depends primarily upon the signal transition time at the input of the driver.

To achieve the minimum transient power dissipation, the initial wire size and tapering factor are simultaneously determined. Differentiating (1) with respect to q and p and equating each expression to zero, two nonlinear equations in q and p are

$$\frac{\partial P_t}{\partial p} = fV_{dd}^2\frac{\partial C_{line}}{\partial p} + \frac{NfG}{0.8}\left(\frac{\partial t_{10\%}}{\partial p} - \frac{\partial t_{90\%}}{\partial p}\right) = 0, \quad (2)$$

$$\frac{\partial P_t}{\partial q} = fV_{dd}^2\frac{\partial C_{line}}{\partial q} + \frac{NfG}{0.8}\left(\frac{\partial t_{10\%}}{\partial q} - \frac{\partial t_{90\%}}{\partial q}\right) = 0, \quad (3)$$

where G is a function of V_{dd}, threshold voltage V_t, transconductance K of the load gate, and capacitive load C_L [6], f is the operating frequency, N is the number of driven gates, $t_{10\%}$ and $t_{90\%}$ are the times at which the voltage at the load end reaches 10% and 90% of the final voltage, respectively, $\frac{\partial t_{10\%}}{\partial p}$ and $\frac{\partial t_{90\%}}{\partial p}$ are described in [6], and $\frac{\partial C_{line}}{\partial p}$ is obtained from the capacitance expression described in [3]. The two nonlinear equations in q and p can be solved numerically. In section 4, tapered wire sizing is compared with uniform wire sizing to decrease the total power dissipation of a circuit. The optimum solution is determined for an example circuit and compared with simulations in section 5.

4. TAPERING VERSUS UNIFORM WIRE SIZING FOR MINIMUM POWER DISSIPATION

Uniform and tapered wire sizing can be used to minimize the power dissipation of a circuit. As compared to uniform wire sizing, tapered wire sizing can achieve enhanced signal characteristics with a lower total interconnect capacitance. As described in [7], for the same signal characteristics (signal propagation delay and transition time), the capacitance of a tapered interconnect line is smaller than the capacitance of a uniformly sized line, since the coupling component of the line capacitance is less. The decrease in line capacitance reduces both the short-circuit power of the load gate and the dynamic power of the driver, reducing the total power dissipation as compared to uniform sizing. The total power dissipation of an optimally tapered RLC interconnect for minimum power is less than the total power dissipation of a uniformly sized interconnect designed for minimum power. A comparison of the power components for both tapered and uniform wire sizing is presented for an example circuit in section 5.

5. SIMULATION RESULTS

In order to determine the optimum tapering factor, the line resistance R_{line}, inductance L_{line}, and capacitance C_{line} are expressed in terms of q and p. Closed form expressions for the line impedance parameters are provided in [3]. Since precise tapering is difficult, the interconnect line is divided into sections. The width of each line section is determined according to the initial width and tapering factor. Twenty RLC line sections are used to model the interconnect assuming the line is shielded with two $1.0\,\mu$m wide ground lines [8]. A fixed width is used for each section with an exponential increase in the section width towards the driver, permitting the impedance parameters of each section to be determined.

A 0.18 μm CMOS technology is used to demonstrate the efficiency of tapering an RLC line. A 5 mm long interconnect line with a line thickness $T = 0.5\,\mu$m, minimum width $W_{min} = 0.1\,\mu$m, maximum width $W_{max} = 20\,\mu$m, and minimum spacing between the line and ground shield $S_{min} = 1.0\,\mu$m is considered. CMOS inverters are used as the driver and loads. In subsection 5.1, the analytic solution is used to determine the optimum tapering structure to minimize the power dissipation. Tapered wire sizing is compared with uniform wire sizing in subsection 5.2.

5.1 TAPERING FOR MINIMUM POWER DISSIPATION

The analytic solution presented in section 3 is used to determine the optimum tapering factor for minimum power dissipation. The total power dissipation is determined assuming W_n = 20 μm, where W_n is the width of the NMOS transistor of the driver (for a symmetric CMOS inverter) and W_{nl} = 10 μm, where W_{nl} is the width of the NMOS transistor of the load inverter. The total power for q = 0.1 μm and N = 1, 2, and 5 is shown in Fig. 3. The total power dissipation decreases as the interconnect line is tapered until the minimum power is achieved. The total power dissipation has a local minimum for each initial width q, which can be obtained by determining the optimum tapering factor p_{opt} for (2). A tradeoff among the power components of the circuit exists in choosing the initial width q.

The optimum tapering structure described by p_{opt} and q_{opt} is determined by simultaneously solving (2) and (3). The optimum solution of the tapered structure and a uniformly sized line is listed in Table 1. In section 5.2, wire tapering is compared with uniform sizing to minimize the total transient power dissipation.

5.2 TAPERING VERSUS UNIFORM WIRE SIZING

The total power dissipation is determined for different sizing criteria to evaluate the tapering criteria presented in section 5.1. The power dissipation for the minimum interconnect width is listed in the second column of Table 2 for different number of loads. The power dissipation along with the per cent reduction using different interconnect sizing techniques are listed in the table.

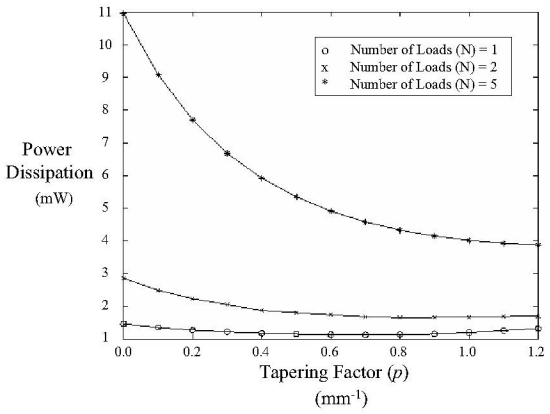

Figure 3: Power dissipation for different number of loads driven by a long tapered interconnect line

Table 1: Optimum sizing for minimum power dissipation

Number of loads (N)	Uniform sizing W_{opt} (μm)	Tapered sizing q_{opt} (μm)	Tapered sizing p_{opt} (mm^{-1})
1	0.8	0.3	0.45
2	1.2	0.7	0.38
5	2.1	1.2	0.34

The optimum initial interconnect width q_{opt} and tapering factor p_{opt} are used to size the interconnect section of a long interconnect line. The total power dissipated by the circuit is listed with the per cent reduction in power as compared to using the minimum interconnect width. Alternatively, circuit simulation is used to determine the optimum solution for minimum power. The power dissipation determined from both the analytic solution and simulations is listed in the final four columns. As listed in the table, the difference between the analytic solution and simulations of the power dissipation and per cent reduction in power is negligible ($< 2\%$). The analytic solution therefore achieves high accuracy in determining the optimum tapering solution for minimum power dissipation.

As the number of loads increases, the reduction in power dissipation becomes greater when tapering an interconnect line. A higher per cent of the power is dissipated in the load gates (inverters), increasing the efficiency of line tapering as a technique to decrease power dissipation. For a large number of loads (*e.g.*, N = 5), a significant reduction in power dissipation of around 72% is achieved.

Table 2: Optimum tapering for minimum power dissipation

Power dissipation (μW)							
Number of loads N	Minimum width	Uniform sizing		Tapered sizing			
			Reduction	Analytic	Reduction	Simulation	Reduction
1	1.4	1.2	17.4%	1.1	22.5%	1.0	23.7%
2	2.8	1.7	41.5%	1.6	44.0%	1.5	45.6%
5	11.0	3.3	69.7%	3.2	71.0%	3.1	71.5%

In the third and fourth columns of Table 2, the minimum power obtained using uniform wire sizing is listed with the per cent reduction in power. A greater reduction in power dissipation is achieved when an optimally tapered interconnect line is used rather than a uniformly sized interconnect. A reduction in power dissipation of 24% is achieved when optimum wire tapering is applied as compared to a 17% reduction with uniform sizing.

In Fig. 4, different power components of the optimum solution for both uniform and tapered lines are shown. The power dissipated by the driver and the total power is illustrated in Figs. 4a and 4b, respectively. As described in section 4, both power components decrease, since an optimally tapered line has a lower total line capacitance.

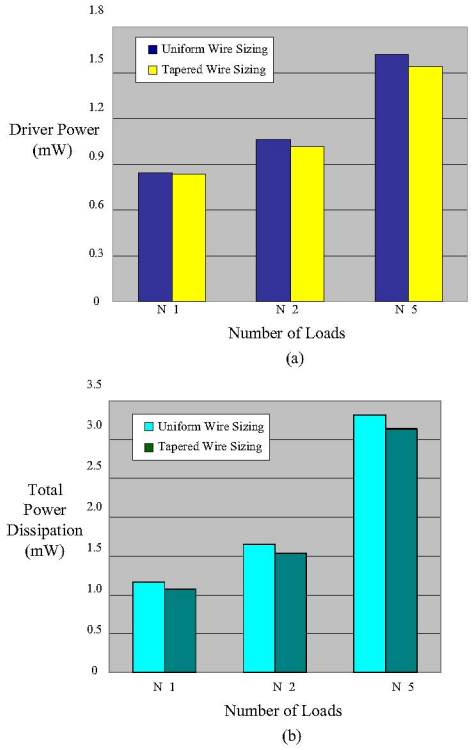

Figure 4: Power components for different number of loads using optimally tapered and uniform wire sizing a) driver power b) total power

6. CONCLUSIONS

Interconnect tapering is shown in this paper to minimize the transient power dissipation. Wire tapering reduces the power dissipated by the load gate and increases the power dissipated by the driver. A tradeoff, therefore, exists in a tapered line between the power dissipated in the load and the driver. An analytic solution for the power dissipation in tapered interconnect with an error of less than 2% is provided. The reduction in power becomes greater as the number of driven gates increases. A reduction in total power dissipation of about 72% is achieved when optimal tapering for minimum power is used rather than uniform sizing with minimum line width.

Optimum tapering for minimum power dissipation is more efficient than uniform wire sizing. Tapering lowers the interconnect capacitance, reducing both transient power components (dynamic and short-circuit). A 24% reduction in power dissipation is achieved when optimum tapering is applied as compared to a reduction of 17% with uniform wire sizing.

7. REFERENCES

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