Quasi-Resonant Interconnects: A Low Power Design Methodology

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Abstract — **Design and analysis guidelines for resonant interconnect networks are presented in this paper. The methodology focuses on developing an accurate analytic distributed model of the on-chip interconnect and inductor to obtain low power and low latency. Excellent agreement is shown between the proposed model and SpectraS simulations. The analysis and design of the inductance, the insertion point, and the driver resistance for minimum power consumption is described. A case study demonstrates the design of a resonant interconnect, transmitting a 5 Gbps data signal along a 5 mm line in a TSMC 0.18 µm CMOS technology. As compared to classical repeater insertion, an average reduction of 94.8% and 72.8% is obtained in power consumption and delay, respectively. As compared to optical links, a reduction of 98.5% and 60% is observed in power consumption and delay, respectively.**

Index Terms— **Resonance, on-chip interconnects, on-chip inductors, power dissipation, latency.**

I. INTRODUCTION

A primary challenge in high performance, high complexity integrated circuit design is the on-chip interconnect [1]. Transmitting clock, data, and communications signals over increasing silicon die area requires long interconnections among the various circuit modules. Consequently, as technology scales, the interconnect cross section decreases while the operating frequency increases. The impact of these trends on high performance systems is significant. Long interconnects with smaller cross sections exhibit increased capacitance and resistance, resulting in increased power consumption, latency, and signal attenuation. Furthermore, wire inductance can no longer be ignored, due to higher signal frequencies and longer wire lengths.

To combat these phenomena, traditional repeater insertion methods have been developed [2]. Low power techniques in the form of low swing signaling and optoelectronic links [3] have been considered. In [4], current mode signaling in an ultra low voltage environment is used to transmit high data rate signals. To improve both delay and energy dissipation, a transmitter generating a differential current sensed by a current mode sense amplifier receiver has been proposed in [5]. To minimize static power dissipation associated with current mode signaling, an adaptive bandwidth bus architecture based on hybrid current voltage mode repeaters for driving long *RC* interconnect has been proposed in [6]. Contrary to the current mode signaling approach, the authors of [7] suggest the use of low voltage signaling over long on-chip interconnects with repeaters. Also in [7], a heuristic algorithm for buffer insertion that accounts for noise, delay, and power is proposed.

A different approach exploiting wire inductance at high frequencies is introduced in [8]. In this scheme, a 1 GHz link operating with phase shift keying modulation on a 7.5 GHz sinusoidal carrier is presented. This type of modulation, however, results in relatively large power dissipation and poor spectral efficiency. Alternatively, the authors of [9] propose to mitigate dispersion by utilizing a return to zero (RZ) signaling scheme in which sharp current pulses are used to transmit data.

In this paper, a low power, low latency on-chip interconnect design methodology is proposed. The methodology is based on inserting on-chip spiral inductor in order to resonate the interconnect capacitance around the fundamental harmonic of the transmitted signal. This approach lowers the power consumption, since the energy resonates between the electric and magnetic fields rather than dissipated as heat.

This paper is organized into five sections. The interconnect and spiral inductor model as well as related design guidelines are described in section II. In section III, a case study is presented for a 5 mm long on-chip interconnect. Simulation results and a comparison to other schemes are presented in section IV. Finally, some conclusions are offered in section V.

II. DESIGN METHODOLOGY

The methodology is based on a shielded interconnect with a capacitive load, driven by a buffer such that the fundamental harmonic of the input bit stream is transferred to the output. Due to resonance, the output signal at the far-end exhibits a sinusoidal behavior. An inverter is placed at the far-end to convert the sinusoidal waveform into an inverted square bit stream. An on-chip spiral inductor resonates the data signal around the harmonic frequency, eliminating the need for repeaters and complex circuitry at the transmitter and receiver ends.

As illustrated in Figure 1, the return to zero (RZ) amplitude shift keying modulation scheme is chosen to support a single targeted transmission frequency of the input data. In this scheme, the data is transferred at $1/t_p$ bits per second. The scheme has three advantages when applying it to the proposed

*This research is supported in part by the Semiconductor Research Corporation under Contract No. 2003-TJ-1O68 and 2004-TJ-1207, the National Science Foundation under Contract Nos. CCR-0304574 and CCF-0541206, grants from the New York State Office of Science, Technology & Academic Research to the Center for Advanced Technology in Electronic Imaging Systems, and by grants from Intel Corporation, Eastman Kodak Company, Manhattan Routing, and Intrinsix Corporation.

quasi-resonant interconnect methodology. The transmitted signal has a single frequency (with one amplitude variation, *i.e.*, V_{dd} and 0 volts), designed to match the resonance frequency of the network. Moreover, power is dissipated only when the logic 1 state is transmitted, and only during half of the time period. Finally, no complex circuitry is required to produce the modulation scheme.

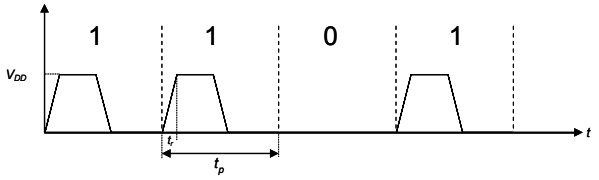

Figure 1. Example of transmitting a "1011" bit stream

The model of the resonant interconnect network is shown in Figure 2. The interconnect is represented by a distributed *RLC* transmission line, where l is the interconnect length, and R, L, and C are the resistance, inductance, and capacitance per unit length, respectively. The driver is linearized as a voltage source V_d serially connected with a driver resistance R_d. The load of the interconnect is modeled as a capacitor C_l. Note that the on-chip inductor is inserted at a distance l_d from the driver to resonate the data signal at a target transmission frequency.

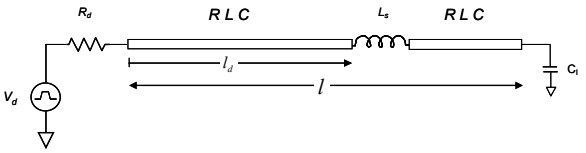

Figure 2. Resonant transmission line network

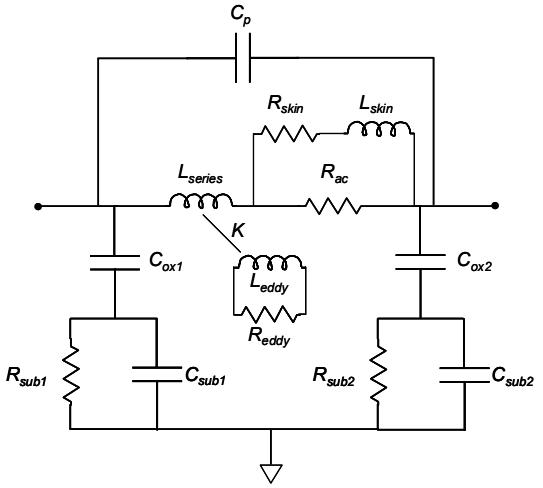

Figure 3. Lumped model of the on-chip inductor

A lumped model of the on-chip inductor is shown in Figure 3. To accurately account for the parasitic effects of the on-chip spiral inductor, a thirteen lumped element model is used. The capacitance C_p represents the capacitive coupling between the windings of the spiral inductor. The elements L_{series} and R_{ac} represent the inductance and parasitic resistance, respectively, while R_{skin} and L_{skin} model the skin effect. Also note that L_{series} incorporates the eddy current effect coupled to the inductor by the coefficient K. The parasitic capacitance between the lines and the substrate is modeled by C_{ox}, and the parallel C_{sub} and R_{sub} combination models the parasitic resistance and capacitance to the substrate.

To analyze the structure shown in Figure 2, an accurate analytic model is developed based on *ABCD* parameters [10]. From transmission line theory, the *ABCD* matrix for the entire structure is a product of the individual matrices,

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = M_1 \cdot M_s \cdot M_2 \cdot M_l, \tag{1}$$

where M_1, M_s, M_2, and M_l are the *ABCD* matrix of the first interconnect section, the on-chip inductor (based on the model of Figure 3), the second interconnect section, and the load capacitance, respectively. The transfer function and input impedance of the system are extracted from the overall *ABCD* parameters,

$$H(j\omega) = \frac{1}{A}, \tag{2}$$

$$Z_{in}(j\omega) = R_{in} + jX_{in} = \frac{A}{C}. \tag{3}$$

Since the resonant interconnect network is a passive linear network, a one-port network, as depicted in Figure 4, can be considered. The output impedance of the driver R_d and the input impedance of the network Z_{in} determine the power consumption of the network.

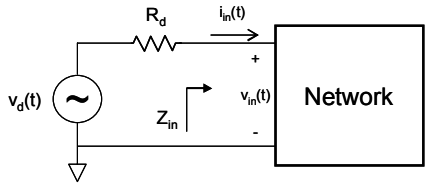

Figure 4. One-port network driven by a voltage source

The rate at which energy is absorbed is the power and is [11]

$$P_{avg} = \frac{1}{2} V_{in,rms}^2 \cdot \Re\left\{\frac{1}{Z_{in}}\right\} = \frac{1}{2} V_{d,rms}^2 \cdot \frac{R_{in}}{(R_{in} + R_d)^2 + X_{in}^2}, \tag{4}$$

where $V_{in,rms}$ and $V_{d,rms}$ are the effective or root-mean square value of the input signal and the driving signal, respectively. Based on (4), the on-chip inductor, the insertion location l_d, and the maximum driver resistance are determined to minimize power consumption. These values are extracted by graphically solving (4) so as to satisfy a full swing data bit stream at the far end of the line.

III. CASE STUDY

In this section, a 5 Gbps 5 mm long resonant transmission link network is assumed as illustrated in Figure 5. The design

guidelines and principles presented in section II are demonstrated in this case study. This example is based on a TSMC 0.18 µm CMOS technology. The resistance, inductance, and capacitance per unit length of the transmission line are extracted using HENRY™ and METAL™, while the on-chip octagonal inductor model parameters are extracted using SPIRAL™ from the OEA software suite [12].

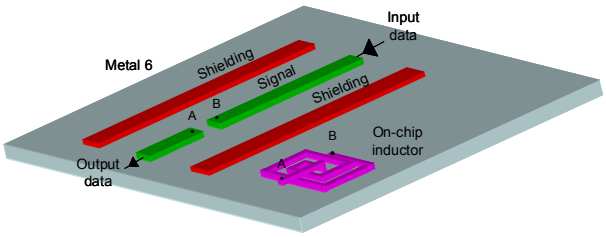

Figure 5. Layout of a resonant transmission line network

In this case study, the interconnect is shielded by ground lines. The separation between the signal and ground lines is 2 µm. The width of the signal and ground lines is 2 µm and 4 µm, respectively, while the thickness of each of the lines is 1 µm. In this example, the interconnect parameters (including the shield lines) are l = 5 mm, R = 17 mΩ/µm, L = 1.66 pH/µm, and C = 0.072 fF/µm.

The minimum power consumption as a function of the on-chip inductance, using (4), is shown in Figure 6(a). In this graph, each point represents the minimum power consumption achieved for a particular inductor. The corresponding insertion point and maximum driver resistance as a function of the on-chip inductance are shown in Figure 6(b) and 6(c), respectively. As evident from Figure 6, the minimum power dissipation occurs when an inductance of L_s = 7.5 nH, inserted at l_d = 4.1 mm, and a driver resistance of R_d = 191 is used. In this case, the power consumption is about 1.23 mW.

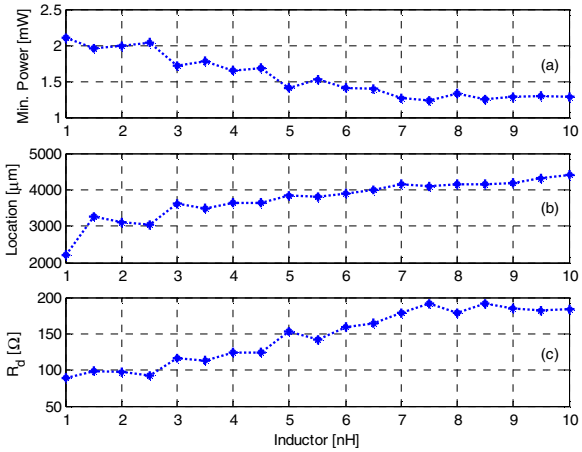

Figure 6. A design example of a 5 mm long interconnect operating at a 5 Gbps transmission frequency: (a) The minimum power as a function of inductance, (b) Insertion location as a function of inductance, and (c) Driver resistance as a function of inductance

The magnitude and phase of the transfer function of a transmission line network are depicted in Figure 7 in the frequency domain. Note that good agreement between simulations and the proposed analytic expressions for the magnitude and phase of the transfer function are achieved, exhibiting a maximum error of 22% and 3.6%, respectively. Also note that at a 5 GHz frequency, the magnitude of the transfer function is near resonance, here described as *quasi-resonance*.

The simulated input and output data signal described in the time domain is shown in Figure 8. Note that the square data waveform is distributed to the far-end, achieving a full rail-to-rail voltage swing. In this example, a "1000101111" bit stream is transmitted at 5 Gbps. Since a buffer is located at the far-end of the link, the output data is inverted, as shown in Figure 8(b). The power consumption per (logic high) bit is 1.17 mW, while the 50% signal delay is 104 psec.

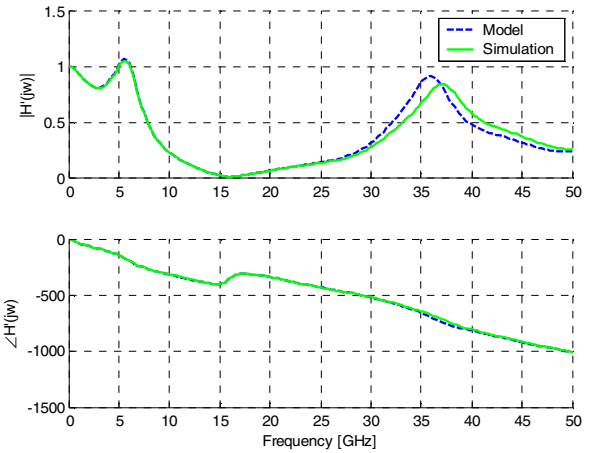

Figure 7. Frequency response of the transfer function: (a) Magnitude, (b) Phase

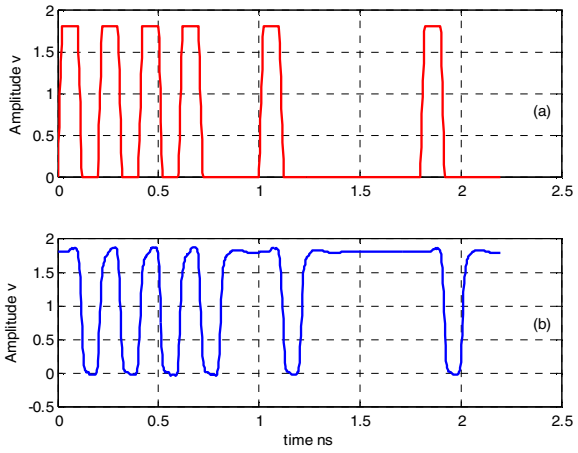

Figure 8. Ten bits data stream example: (a) Input data, (b) Output data

IV. Simulation Results and Comparison

To evaluate the proposed methodology and compare it to a traditional buffer insertion method, a 5 Gbps data signal and 0.5, 1, 3, 5, and 10 mm length interconnects are considered, as listed in Table 1. Note that in a 0.18 µm CMOS technology, it is a challenge to design repeaters to drive long interconnects at frequencies as high as 5 GHz. Hence, signal integrity in this repeater insertion case has been compromised for the sake of this comparison. From Table 1, the average reduction in power consumption and delay is 94.8% and 72.8%, respectively. The

performance improvement is due to the repeater-less nature of the quasi-resonant interconnect.

A comparison between the proposed methodology and other approaches in the literature are listed in Table 2. Interestingly, a maximum reduction in power consumption of 98.5% and a 60% delay reduction occurs as compared to optoelectronic links [3]. The power consumption overhead in [3] is due to the edge emitting laser modulator at the transmitting edge and the photodiode and signal level restorer at the receiving end of the optical link. This example may suggest that using novel signaling schemes incorporating electrical interconnects outperforms optoelectronic solutions. These results are obtained despite the optical link transmitting a slower signal (3 Gbps) as compared to the resonant link (5 Gbps). As listed in Table 2, the proposed quasi-resonant interconnect methodology outperforms other approaches described in the literature in both power and latency.

Table 1. Comparison of power consumption and delay

Length [mm]	This work		Repeater insertion		Improvement	
	Power [mW]	Delay [ps]	Power [mW]	Delay [ps]	Power %	Delay %
0.5	0.48	39	5.92	104	91.9	62.5
1	0.57	41	10.79	160	94.7	74.4
3	0.75	76	16.87	255	95.6	70.2
5	1.17	104	25.20	368	95.4	71.7
10	1.82	158	51.20	1100	96.4	85.6

Table 2. Performance comparison of quasi-resonant method with different approaches

	Tech-nology	Speed [Gbps]	Length [mm]	Power [mW]	Delay [ps]
This work	180 nm	5	3	0.75	76
Pulsed current [8]	180 nm	8	3	27.12	280
Improvement				97.2%	72.8%
This work	180 nm	5	17	3.7	231
Signal modulation [9]	180 nm	1	20	16	300
Improvement				76.9%	23.0%
This work	180 nm	5	5	1.17	104
Optics (edge emitting) [3]	250 nm	3	5	78	260
Improvement				98.5%	60.0%
This work	180 nm	5	5	1.17	104
Optics (VCSEL) [3]	250 nm	3	5	66	300
Improvement				98.2%	65.3%
This work	180 nm	5	15	3.07	212
Loss compensation [13]	180 nm	3	14	6	140
Improvement				48.8%	-34%

V. CONCLUSIONS

A methodology is described in this paper for designing quasi-resonant interconnect networks. An accurate model is presented based on transmission line theory and a lumped model of an on-chip spiral inductor to represent high frequency effects. The high accuracy of the model enables the design of low power, low latency resonant communication links. The methodology can be used to determine the inductance L_s, insertion point l_d, and driver resistance R_d that minimizes power consumption.

From the comparison listed in Tables 1 and 2, quasi-resonant interconnects outperform other technologically aggressive approaches. For buffered lines, an average reduction of 94.8% and 72.8% is obtained in power consumption and delay, respectively. As compared to optical links, a reduction of 98.5% and 60% is observed in power consumption and delay, respectively (excluding the transmitter and receiver circuits). These results show that quasi-resonant interconnects exhibit superior performance, suitable for high performance, high complexity integrated circuits.

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