Substrate Noise Reduction Based On Noise Aware Cell Design

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***Abstract*— A substrate biasing methodology is introduced based on modifying standard cells by inserting dedicated substrate contacts in those cells behaving as aggressive digital noise generators. These contacts are connected to a dedicated ground network. The proposed approach reduces two primary noise injection mechanisms: ground coupling and source/drain junction coupling. Limitations of the Kelvin biasing scheme are removed while achieving more than a 60% (9 dB) reduction in substrate noise at the cost of a 12% increase in area.**

I. INTRODUCTION

The integration of digital, analog, and RF circuits has become ubiquitous in modern integrated circuits to achieve higher performance and reduced cost. A major obstacle of these mixed-signal systems is substrate noise coupling. The common substrate forms a conductive path between the noisy digital circuit and the sensitive analog/RF circuit, degrading performance. Signal isolation between the digital and analog/RF circuits is, therefore, a challenging task.

Three primary mechanisms exist for injecting noise into the substrate: coupling from the digital ground and power rails, coupling from the junction capacitances of the devices, and impact ionization [1], [2], [3]. For complex integrated circuits, coupling from the ground and power rails is the dominant noise generation mechanism [4], [5].

Simultaneous switching noise caused by the parasitic inductance (di/dt noise) and transient IR drops caused by the resistance of the ground network directly affect the substrate through the substrate contacts. Employing a dedicated substrate bias by separating the ground network of the contacts reduces substrate noise coupling [4], [6], [7]. This technique, known as Kelvin biasing, reduces substrate noise at the cost of lower device reliability, increased power/ground noise, and additional metal resources. These limitations make the use of Kelvin biasing impractical.

An alternative substrate biasing methodology is introduced in this paper based on modifying the design of the standard cell library. Standard cells with dedicated substrate contacts are proposed for those cells that generate significant noise. These dedicated contacts are connected to a separate ground to provide isolation from the noisy ground network. The proposed methodology achieves more than a 60% reduction in substrate noise while removing the limitations of the Kelvin biasing scheme.

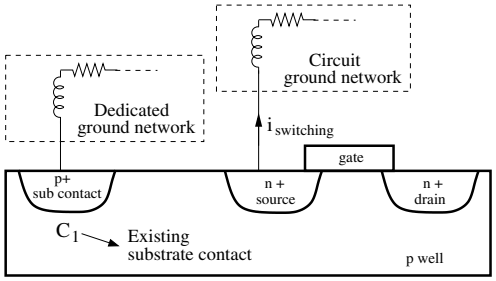

Fig. 1. Kelvin biasing scheme to reduce substrate noise. The substrate contacts are connected to a dedicated ground network rather than the ground network of the digital circuit to prevent ground noise coupling into the substrate.

The primary drawback of the proposed technique is the increased area due to the additional contacts and the separate ground network. This increased area, however, is minimized because these modified cells are only used in the primary noise generating blocks within a circuit. The additional ground network and contacts are therefore only required in these blocks.

The rest of the paper is organized as follows. The substrate biasing schemes are reviewed in Section II. The proposed methodology is described in Section III. Simulation results are presented in Section IV. These results are discussed and compared with Kelvin biasing in Section V. Some conclusions are drawn in Section VI.

II. SUBSTRATE BIASING SCHEMES

In a mixed-signal circuit, several different techniques exist to bias the substrate. The conventional approach is to connect the substrate contacts to the ground network of the digital circuitry. This technique, however, injects significant noise into the substrate since the digital ground suffers from simultaneous switching noise.

Kelvin biasing, as illustrated in Fig. 1, has been proposed to reduce noise injection by biasing the substrate with a dedicated ground network. This technique removes the resistive

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connection of the substrate with the noisy digital ground, thereby reducing substrate noise. Kelvin biasing, however, has significant limitations. Since the substrate is biased separately, the devices suffer from the body effect which can have a significant effect on high performance circuits. Another drawback is the increased power/ground noise since the n-well capacitance cannot be exploited as a decoupling capacitance. A reduction by a factor of three in the total decoupling capacitance is reported in [6] if Kelvin biasing is employed.

While reducing ground coupling into the substrate, Kelvin biasing is ineffective in reducing source/drain junction coupling. The overall reduction in substrate noise is, therefore, limited. Furthermore, Kelvin biasing requires an additional ground network, making the technique impractical in terms of the required metal resources.

Another technique to bias the substrate is a backside contact, which increases the cost and requires specialized packaging. The use of an analog ground rather than a digital ground has also been suggested to bias the substrate [6]. If an analog ground is used, however, substrate noise can couple into the analog ground network, degrading performance.

III. PROPOSED METHODOLOGY

The design of a standard cell with a dedicated substrate contact is explained in Section III-A. An analysis of the substrate noise reduction mechanism using these standard cells is described in Section III-B.

A. Standard Cell with a Dedicated Substrate Contact

In the design of a digital integrated circuit, the placement of the substrate contacts is usually achieved after the place-and-route phase of the design flow is completed. The latch-up design rules determine the minimum distance among the contacts.

A standard cell design approach is proposed in this paper where each cell in the library has a dedicated substrate contact. This dedicated substrate contact is placed in close proximity to the cell, as determined by technology based design rules. Conventional and *aggressor* standard cells are illustrated in Fig. 2. Note that these aggressor cells are in addition to existing conventional cells in the library, where the choice between a conventional and aggressor cell is made depending upon several factors such as the switching activity of the digital block and the physical distance between the digital and sensitive analog blocks within a circuit.

The physical representation of a cell with a dedicated substrate contact is shown in Fig. 3. C_1 represents an existing substrate contact placed according to the latch-up design rules and C_2 represents the dedicated substrate contact of the cell. Note that C_1 is connected to the ground network of the digital circuit; a separate ground network, however, is required for the dedicated contacts in order to isolate these contacts from the noisy ground network. Noise reduction is achieved through the low impedance path between C_1 and C_2. The injected noise from the noisy contact C_1 is filtered through C_2 rather than propagated into the substrate.

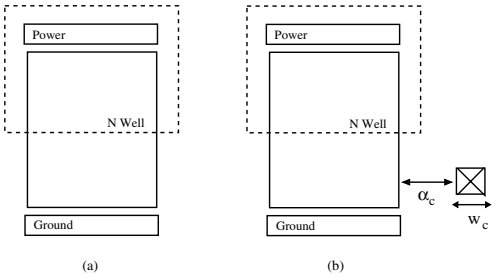

Fig. 2. Standard cell: (a) conventional cell, (b) aggressor cell with a dedicated substrate contact. α_c is the minimum distance between the contact and the diffusion, and w_c is the width of the contact.

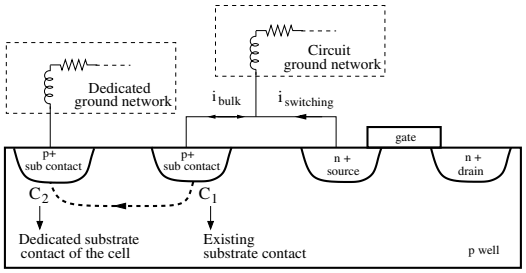

Fig. 3. The effect of the dedicated contact on reducing substrate noise. The injected noise from the noisy contact C_1 is filtered through the dedicated contact C_2 rather than propagated into the substrate.

The drawback of providing a dedicated substrate contact is an increase in circuit area. This increase in area can be expressed as

$$\Delta A = L(\alpha_c + w_c)n, \tag{1}$$

where L is the length of the standard cell, α_c is the minimum distance between the n-type and p-type diffusion regions, w_c is the width of the contact, and n is the number of aggressor cells with a dedicated substrate contact. Note that these types of cells are only used in aggressor digital blocks that are identified as major noise sources. The number n, therefore, is usually a small fraction of the total number of cells, lessening the increase in area.

B. Analysis of Noise Reduction Mechanism

The dedicated contacts connected to a separate ground network significantly reduce the noise current propagating through the substrate. This reduction is due to the change in the impedance seen by the switching current.

Equivalent circuit models to analyze substrate noise through ground coupling are shown in Fig. 4. A circuit model for conventional substrate biasing is shown in Fig. 4(a). The switching current is divided based on the impedance of the ground and substrate networks. For Fig. 4(a), the noise voltage at sense node S_1 is

$$v_{s1}(\omega) = \frac{I_s|Z_1(\omega)|}{R_{cs1} + R_{sg} + |Z_1(\omega)|} R_{sg}, \tag{2}$$

where I_s is the switching current, $Z_1(\omega)$ is the ground network impedance, R_{cs1} is the substrate resistance between contact C_1 and the sense node S_1, and R_{sg} is the substrate resistance between the sense node and ground, which is usually the analog ground of the circuit.

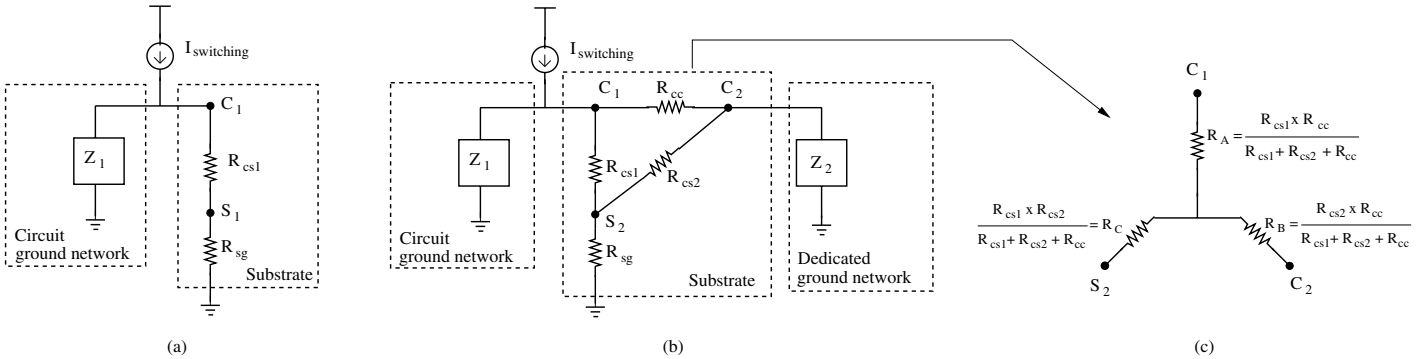

Fig. 4. Equivalent circuit models to analyze substrate noise through ground coupling: (a) Circuit model for the conventional scheme. I_s is the switching current of the circuit. C_1 is the conventional substrate contact, Z_1 is the ground network impedance, and S_1 is the substrate location where the noise is analyzed, (b) Circuit model for the proposed scheme. C_2 is the dedicated substrate contact of the standard cell and Z_2 is the impedance of the additional ground network to which the dedicated contacts are connected, (c) Transformation of the mesh formed by the contacts C_1 and C_2, and node S_2.

A circuit model for the proposed substrate biasing scheme is shown in Fig. 4(b). The dedicated substrate contact C_2 is connected to a separate ground network with impedance Z_2. Note that the mesh formed by the contacts C_1 and C_2, and node S_2 can be transformed using resistances R_A, R_B, and R_C, as illustrated in Fig. 4(c). After this transformation, the noise voltage at the sense node S_2 can be expressed as

$$v_{s2}(\omega) = \left[\frac{I_s|Z_1(\omega)|}{[(R_C+R_{sg})\backslash\backslash(R_B+|Z_2(\omega)|)]+R_A+|Z_1(\omega)|}\right] x \left[\frac{R_B+|Z_1(\omega)|}{R_{sg}+R_C+R_B+|Z_2(\omega)|}\right] R_{sg}, \quad (3)$$

where I_s is the switching current, $Z_1(\omega)$ is the impedance of the circuit ground network, $Z_2(\omega)$ is the impedance of the dedicated ground network, and R_A, R_B, and R_C are the substrate resistances after transformation of the mesh.

For practical values of substrate resistances and assuming $Z_1 = Z_2$, the noise voltages predicted by (2) and (3) are illustrated as a function of frequency in Fig. 5. The solid lines represent the noise voltage for a conventional scheme and the dashed lines represent the noise voltage for the proposed scheme. More than a 50% reduction in noise voltage is predicted according to an analytic analysis based on equivalent circuit models.

IV. SIMULATION RESULTS

A noise generator circuit, as shown in Fig. 6, has been designed in a 90 nm double-well CMOS technology with a bulk type (non-epi) substrate. The circuit consists of four chains of scaled buffers driven by input signals with 70 ps rise and fall times.

Three different versions of the circuit are realized. The first circuit represents the conventional technique where regular cells are used and the substrate contacts are placed according to the latch-up constraints of the technology. The second circuit utilizes a Kelvin biasing technique where the contacts of the first circuit are connected to a separate ground network, as shown in Fig. 1. The third circuit utilizes the proposed methodology where each cell has a dedicated substrate contact, assuming all cells are aggressors. These dedicated contacts are connected to a separate ground network as shown in Fig. 3. Note that the contacts of the first circuit remain the same for the third circuit.

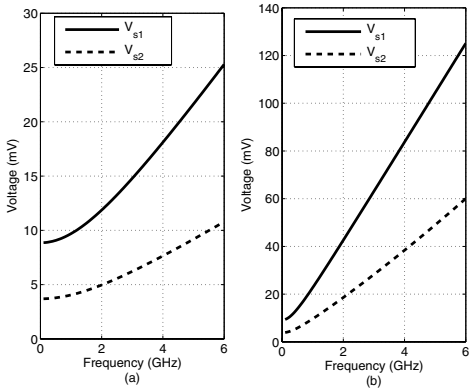

Fig. 5. Analytic predictions of the noise voltages V_{s1} and V_{s2} with: (a) a flip-chip package, (b) a bond-wire package.

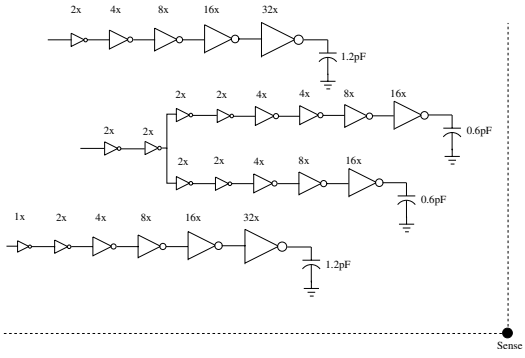

Fig. 6. Noise generator circuit consisting of four chains of scaled buffers to evaluate the proposed substrate biasing methodology.

The layout and substrate impedances of the three circuits are extracted, respectively, using Assura RCX [8] and SubstrateStorm [8], while the overall netlist is simulated using Spectre [8]. For each circuit, the substrate noise voltage is examined at the sense node which is located 25 μm away from the closest contact, as shown in Fig. 6.

TABLE I

COMPARISON OF PEAK-TO-PEAK SUBSTRATE NOISE VOLTAGE FOR THE CONVENTIONAL, KELVIN, AND PROPOSED TECHNIQUES. ON-CHIP INTERCONNECT PARASITIC IMPEDANCES: $R = 3\ \Omega$ AND $L = 160$ pH. FLIP-CHIP PARASITIC IMPEDANCES: $R = 0.1\ \Omega$ AND $L = 60$ pH. BOND-WIRE PARASITIC IMPEDANCES: $R = 0.2\ \Omega$ AND $L = 1$ nH.

On-chip interconnect / package type	Peak-to-peak substrate noise (mV)			Noise reduction over conventional	Noise reduction over Kelvin
	Conventional	Kelvin	Proposed		
R only / flip-chip	32	20	9	72%	55%
RL / flip-chip	47	29	16	66%	45%
R only / bond-wire	116	58	39	66%	33%
RL / bond-wire	129	61	42	67%	31%

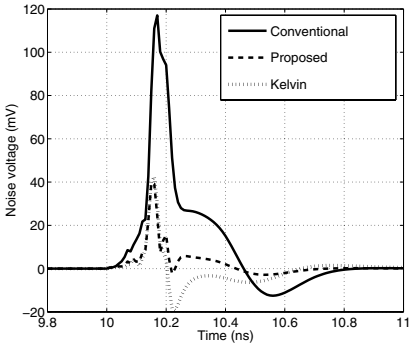

Fig. 7. Substrate noise voltage at the sense node for the conventional, Kelvin, and proposed schemes.

The substrate noise voltage waveforms for the conventional, Kelvin, and proposed techniques are shown in Fig. 7. The ground network has a distributed parasitic impedance of $R = 3\ \Omega$ and $L = 160$ pH with a bond-wire package exhibiting a lumped parasitic impedance of $R = 0.2\ \Omega$ and $L = 1$ nH.

The peak-to-peak substrate noise voltage for the three techniques are listed in Table I for different ground network impedances and package types. Significant noise reduction over conventional and Kelvin biasing schemes is achieved using the proposed methodology. The drawback is the increase in area due to the additional contacts. For this example, the additional required area is 82 μm^2, corresponding to a 12% increase.

V. DISCUSSION

The proposed methodology achieves a greater reduction in noise as compared to Kelvin biasing. This result occurs because Kelvin biasing only reduces the ground coupling noise generation mechanism. The proposed technique, however, reduces both ground and the junction coupling mechanisms. The greater reduction in noise as compared to the Kelvin technique with a smaller ground parasitic impedance, as listed in the last column in Table I, supports this conclusion.

In addition to a greater reduction in noise, the proposed methodology removes the limitations of Kelvin biasing. The voltage difference between the source and body of the transistors for Kelvin biasing is as large as 160 mV. For the proposed technique, this voltage difference is several millivolts. The body effect is, therefore, smaller and the likelihood of latch-up is reduced.

The proposed scheme exploits the n-well capacitance as a decoupling capacitance to reduce power/ground noise. Kelvin biasing, however, cannot exploit the n-well capacitance because the circuit and the substrate have separate bias networks.

Another major limitation of Kelvin biasing is the requirement for an additional ground network, making this approach impractical considering limited metal resources. Alternatively, the proposed methodology only requires an additional ground network for the aggressor cells with a dedicated contact.

VI. CONCLUSIONS

A substrate biasing scheme is presented in this paper based on modifying the design of a standard cell library. Cells with dedicated substrate contacts are proposed for the noise generating digital blocks within a circuit. The substrate is biased with the ground network of the digital circuit through existing substrate contacts. The dedicated substrate contacts within the aggressor cells, however, are connected to a separate ground network. A low impedance path in the substrate is thereby created between the noisy contacts and the dedicated contacts. Simulation results show, on average, a reduction in substrate noise of 68% (9.87 dB) over the conventional technique and 41% (4.71 dB) over the Kelvin biasing scheme. Furthermore, the limitations of Kelvin biasing are removed using the proposed methodology. The impact of the relative location of the dedicated and existing contacts with respect to the sense node, and identifying the aggressor blocks in a mixed-signal circuit remain as future work.

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