Input Port Reduction for Efficient Substrate Extraction in Large Scale IC's

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***Abstract*— A methodology is proposed to improve the efficiency of the substrate impedance extraction process for a large scale circuit by exploiting the circuit activity. Similarly biased regions of the substrate short-circuited by the ground network are identified to reduce the computational complexity of the extraction process. Each of these *voltage domains* is represented by a single equivalent input port to the substrate, merging the remaining ports within that domain. An algorithm is presented to determine these domains and generate an equivalent port for each domain. The parasitic impedance of the ground network is updated to maintain accuracy. A reduction of more than two orders of magnitude in the number of extracted substrate resistances is demonstrated while introducing 15% error in the rms value of the substrate noise voltage at the sense node.**

I. INTRODUCTION

The integration of diverse functionalities such as digial, analog, and RF circuits onto the same die increases at a growing pace due to the desire for enhanced performance and reduced cost. Furthermore, the physical distance among these blocks shrinks as the technology improves, making substrate coupling a primary concern in mixed-signal systems. The accurate and efficient estimation of the substrate coupling noise, and functional verification of the circuit in the presence of this noise has become an important design issue.

Digital circuits with high switching activity inject noise into the substrate through substrate contacts, source/drain junction capacitances, and impact ionization (which is negligible as compared to the first two mechanisms) [1]. The noise propagates through the substrate and reaches the boundary of the sensitive analog/RF block, degrading signal precision. Estimating the substrate coupling noise at the boundary of a sensitive block in a large scale circuit is a challenging task due to the high computational complexity of the substrate extraction process [2], [3].

A methodology is proposed in this paper to reduce the computational complexity of the substrate extraction process by reducing the number of input ports. The number of input ports is reduced by exploiting similarly biased regions within the substrate where each region represents a voltage domain. These regions are identified through differences in the transient voltage among the substrate contacts. An algorithm is introduced to determine these domains, reduce the number of ports, and create an equivalent port for each domain.

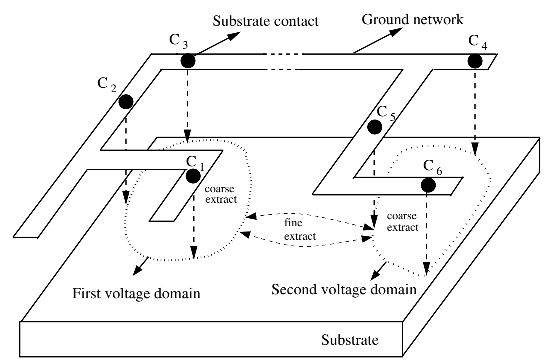

Fig. 1. Identification of voltage domains within the substrate. Assuming $V_{C1} \approx V_{C2} \approx V_{C3}$ and $V_{C4} \approx V_{C5} \approx V_{C6}$, two voltage domains are created by the first and last three contacts. A coarse extraction is performed within each domain to reduce the computational complexity, followed by a fine extraction of those domains where the dominant current flow occurs.

The rest of the paper is organized as follows. Relevant background and existing extraction schemes are summarized in Section II. The proposed methodology and algorithm are described in Section III. Simulation results are presented in Section IV, and the paper is concluded in Section V.

II. EXISTING EXTRACTION SCHEMES

Two primary approaches exist that discretize the substrate into a 3-D *RC* mesh to determine the substrate impedances: finite difference method (FDM) [4], [2] and boundary element method (BEM) [5], [6]. FDM discretizes the substrate in differential form, resulting in a huge, but sparse matrix. Alternatively, the substrate is discretized in integral form by BEM, resulting in a significantly smaller, yet highly dense matrix. For BEM, only the ports into the substrate are discretized, making the computational complexity a strong function of the number of input ports.

Another method to model the substrate is to use macromodels to represent the impedance between two ports on the substrate [7], [8]. Although computationally less expensive as compared to FDM and BEM, only limited accuracy can

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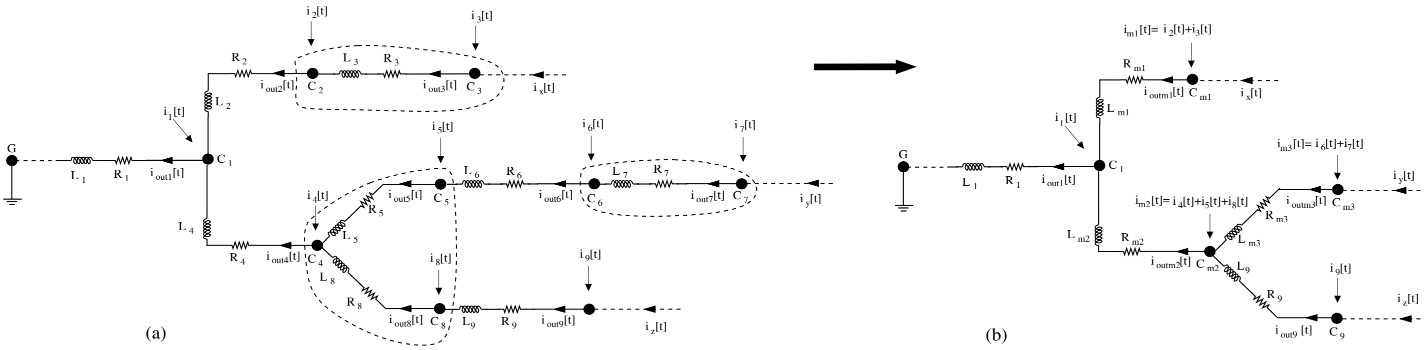

Fig. 2. Illustration of contact merging to reduce the number of input ports for substrate extraction process. The original ground network (a) contains nine substrate contacts. Three voltage domains are identified by merging C_2 and C_3, C_4, C_5, and C_8, and C_6 and C_7. The reduced network (b) has five substrate contacts.

be achieved. Other limitations are the requirement to obtain process-dependent fitting parameters and scaling these models for different geometries.

Several techniques have been proposed to improve the efficiency of these approaches [9], [10], [11], focusing on the efficient solution of the algebraic equations obtained after the substrate is discretized by either FDM or BEM. The main limitation of both of these approaches, however, is the increase in computational complexity with circuit size, prohibiting the analysis of large scale circuits. A methodology is proposed in this paper to improve the complexity *before* the substrate is discretized. This improvement is achieved by reducing the number of ports for the extraction process, as described in the next section.

III. Input Port Reduction

The concept of voltage domains on the substrate is introduced in Section III-A. The algorithm to determine these domains and generate an equivalent port for each domain is described in Section III-B.

A. Voltage Domains on the Substrate

In a mixed-signal circuit, a common approach to bias the substrate is to use substrate contacts connecting the substrate to the digital ground network. The parasitic resistance and inductance of the ground network produce $IR + L\,\partial i/\partial t$ voltage bounces at each contact. If this voltage difference among several contacts is sufficiently small, the corresponding area on the substrate is effectively short-circuited, as illustrated in Fig. 1.

In Fig. 1, C_1, C_2, and C_3 produce the first voltage domain, and similarly, C_4, C_5, and C_6 determine the second voltage domain. The dominant current flow occurs among the domains since the voltage variations within a domain is sufficiently small. These voltage domains can be exploited by reducing the number of ports to the substrate within a domain, allowing a coarse extraction, thereby improving the computational complexity. This reduction is achieved by merging all of the contacts into one equivalent contact within a domain. This equivalent contact is placed at the geometric mean of the merged contacts and the corresponding parasitic resistance and inductance of the ground network are updated to maintain accuracy, as described in the next section.

```
REDUCE-PORTS(extracted ground network, V_lim)
for each node
    for each child of the node
        calculate V_diff(child)
    end
    identify bigChild
    if V_diff(bigChild) ≤ V_lim
        merge the children and parent
        update R, L, and I[t]
    end
end
```

Fig. 3. Simplified pseudo-code to merge the substrate contacts on the ground network based on spatial transient voltage differences to reduce the number of ports to the substrate.

B. Algorithm to Reduce the Number of Ports

The extracted ground network of the aggressor circuit is represented as a tree data structure where each substrate contact is a node and the root of the tree is an ideal ground. For each node (or contact) C_i, the algorithm requires the resistance R_{ci} and inductance L_{ci} of the ground network between the node and parent of the node, and the transient switching current $I_{ci}[t]$ injected into the node during a specific time window. For a large digital block, these current profiles can be obtained by pre-characterizing each standard cell within a library followed by a behavioral simulation of the circuit to extract the switching time of each cell. The current injected by those cells located between two contacts is shifted to the previous contact to prevent overly optimistic results.

An example is shown in Fig. 2 to illustrate the inputs and outputs of the algorithm. The original ground network contains nine substrate contacts where each contact has a switching current profile $I_{ci}[t]$, and a resistance R_{ci} and inductance L_{ci} between the contact and parent of the contact. Simplified pseudo-code of the algorithm is provided in Fig. 3.

The algorithm evaluates the voltage difference $V_{diff}(child)$ between the contact and each child of the contact. The child with the greatest voltage difference is identified as *bigChild*. If this voltage difference is smaller than a user specified voltage V_{lim}, the parent and all of the children are merged into one equivalent contact, creating a voltage domain. This equivalent contact is placed at the geometric mean of the merged contacts. In Fig. 2, three voltage domains are determined by merging C_2

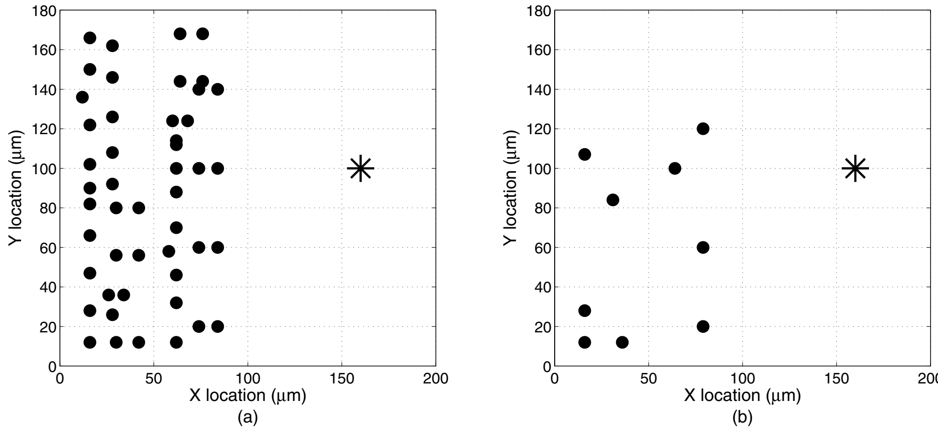

Fig. 4. Physical location of the substrate contacts (represented by the circles) and the sense node (represented by the star sign) where the substrate noise is observed: (a) original 48 contacts before merging (b) nine equivalent contacts after merging when $V_{lim} = 0.1$ volts.

and C_3; C_4, C_5, and C_8; and C_6 and C_7. The reduced network is composed of five substrate contacts.

The resistance, inductance, and switching current of the equivalent contact are updated to maintain the original absolute voltage with the least error. The updated current is equal to the summation of the currents of the merged contacts. The resistance and inductance are updated based on *bigChild* for only the peak points of the transient current waveforms. For example, for C_{m2}, this update is achieved as shown in (2), (3), and (4), assuming C_5 is *bigChild*, *e.g.*, $V_{diff}(c5)$ is greater than $V_{diff}(c8)$.

$$I_{m2}[t] = I_4[t] + I_5[t] + I_8[t], \tag{1}$$

$$I_{outm2}[t] = I_4[t] + I_{out5}[t] + I_{out8}[t], \tag{2}$$

$$R_{m2} = R_4 + R_5 \frac{max(I_{out5}[t])}{max(I_{out4}[t])}, \tag{3}$$

$$L_{m2} = L_4 + L_5 \frac{max(\partial(I_{out5}[t])/\partial t)}{max(\partial(I_{out4}[t])/\partial t)}. \tag{4}$$

Note that for C_{m1} and C_{m3}, the resistance and inductance are updated based on, respectively, C_3 and C_7 since C_2 and C_6 have a single child.

IV. SIMULATION RESULTS

The algorithm has been evaluated on an aggressor circuit consisting of a 4-bit carry select adder, a control unit, and scaled buffers at the output, designed in a 0.18 μm CMOS technology on a bulk type substrate.

The ground network of the circuit consists of the first two metal layers, and originally contains 48 substrate contacts. The current profile for each contact is obtained from a transistor level simulation for a specific time window. The parasitic resistance between each contact is determined from the sheet and via resistances. The sheet resistances are 95 mΩ and 80 mΩ for the first and second metal layer, respectively, and the via resistance is 2 Ω.

The REDUCE-PORTS algorithm is performed to identify the voltage domains on the substrate. Four different values (0.05 volts, 0.1 volts, 0.25 volts, and 0.4 volts) are used for

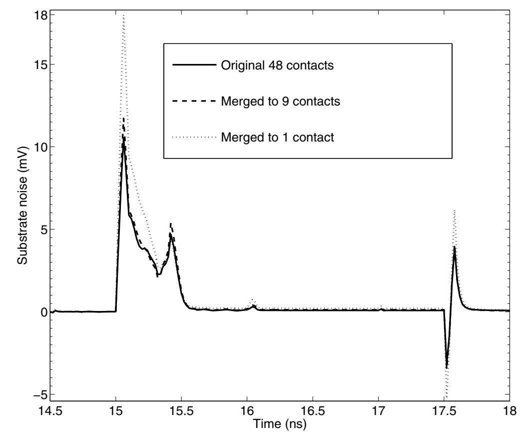

Fig. 5. Comparison of the substrate noise at the sense node before and after merging. The solid line represents the original circuit with 48 substrate contacts. The dashed and dotted lines represent, respectively, the reduced network with nine substrate contacts ($V_{lim} = 0.1$ volts) and a single substrate contact ($V_{lim} = 0.4$ volts).

V_{lim} to investigate the complexity versus accuracy tradeoff. For $V_{lim} = 0.1$ volts, nine voltage domains are identified. Each of these domains is represented by an equivalent substrate contact placed at the geometric mean of the merged contacts. The original physical location of the 48 substrate contacts and nine equivalent contacts after merging when $V_{lim} = 0.1$ volts are illustrated in Fig. 4.

The substrate is extracted for the pre- and post-merging cases using SubstrateStorm. The noise is observed using Spectre at the sense node located 60 μm from the nearest substrate contact, as shown in Fig. 4. Note that the parasitic resistance between the substrate contacts on the ground network and the current profile of each contact are updated after merging based on the REDUCE-PORTS algorithm. The time domain noise waveforms observed at the sense node before and after merging are compared in Fig. 5. The waveform shape and peak magnitude of the substrate noise at the sense node after merging into nine contacts match the original noise voltage with a peak-to-peak error of 11% in the noise voltage. Note that the error increases to 70% if V_{lim} is increased to 0.4 volts,

TABLE I

REDUCTION IN THE NUMBER OF EXTRACTED SUBSTRATE RESISTORS, SUBSTRATE NOISE AT THE SENSE NODE, AND THE CORRESPONDING ERROR IN THE SUBSTRATE NOISE FOR DIFFERENT VALUES OF V_{lim}.

	Number of substrate contacts	Number of extracted substrate resistors	Reduction	Noise at the sense node			Error at the sense node		
				Peak-to-peak	RMS	At 200 MHz	Peak-to-peak	RMS	At 200 MHz
Original	48	1225	–	11.6 mV	0.68 mV	-60 dB	–	–	–
$V_{lim} = 0.05$V	15	136	9x	10.5 mV	0.61 mV	-60.9 dB	9.5%	10.3%	0.9 dB
$V_{lim} = 0.1$V	9	55	22.3x	12.9 mV	0.72 mV	-59.6 dB	11.2%	5.9%	0.4 dB
$V_{lim} = 0.25$V	3	10	122.5x	15.3 mV	0.78 mV	-58.9 dB	31.9%	14.7%	1.1 dB
$V_{lim} = 0.4$V	1	3	408.3x	19.7 mV	0.87 mV	-58.4 dB	69.8%	27.9%	1.6 dB

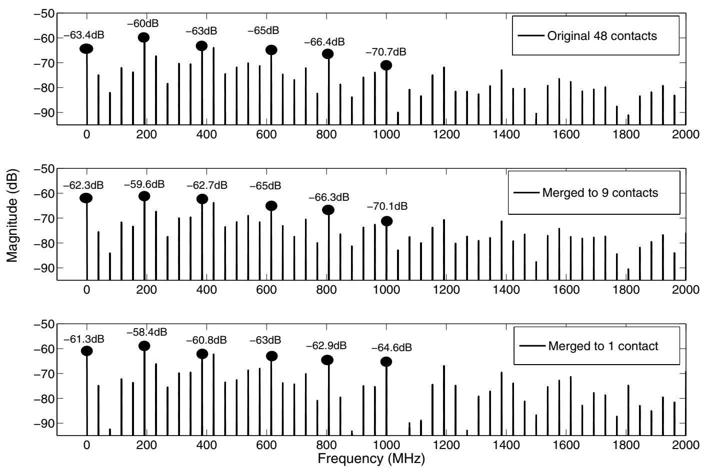

Fig. 6. Comparison of the spectrum of the substrate noise at the sense node before and after merging into nine contacts ($V_{lim} = 0.1$ volts) and a single contact ($V_{lim} = 0.4$ volts).

merging all 48 contacts into a single contact. The error in the rms noise over one period is 6% for nine contacts and increases to 28% for a single contact.

The frequency domain characteristics are illustrated in Fig. 6. The average error at the fundamental frequency (200 MHz) and four higher harmonics is 0.42 dB when $V_{lim} = 0.1$ volts (the number of contacts is reduced to nine). For $V_{lim} = 0.4$ volts (where the number of contacts is reduced to one), the average error increases to 2.9 dB. Note that in this case, the error increases at the higher harmonics, for example, 6 dB at 1 GHz.

Considering the number of substrate resistances, SubstrateStorm extracts 1225 resistors in the original system with 48 substrate contacts. Alternatively, when the number of contacts is reduced to nine, the number of extracted substrate resistances is 55, corresponding to a 20X reduction. The reduction in the number of extracted substrate resistors, and the corresponding error (peak-to-peak, rms, and at the fundamental frequency) in the substrate noise are listed in Table I for four different values of V_{lim}, demonstrating the accuracy versus complexity tradeoff.

V. CONCLUSIONS

A methodology is proposed to improve the efficiency of the substrate impedance extraction process for large scale circuits. Similarly biased regions on the substrate are identified through the transient voltage difference among substrate contacts, where each region represents a voltage domain. An algorithm is presented to determine these domains and generate an equivalent port for each domain, merging the remaining ports within that domain to improve the computational complexity of the extraction process. The impedance of the ground network is updated to maintain the original transient voltage after merging. A reduction of more than two orders of magnitude in the number of extracted substrate resistances is demonstrated with an error of less than 15% in the rms value in the time domain and around 1 dB error at the fundamental frequency of the substrate noise at the sense node.

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