Minimizing Noise via Shield and Repeater Insertion

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***Abstract*—Two techniques, shield and repeater insertion, are simultaneously investigated. Based on resource optimization, the relationship among noise, power, and delay is investigated. Coupling noise as a function of power dissipation is shown to behave parabolically. Due to this parabolic behavior, the minimum noise can be established. The resulting design expressions are compared with SPICE simulations, exhibiting good agreement. A design case is compared with only shielding and only repeater insertion techniques, exhibiting enhanced performance for different resources.**

I. Introduction

Further increases in integrated circuit (IC) scaling requires more efficient devices, circuits, and systems in terms of power, delay, noise, and area. To achieve this capability, many different design techniques are used. In many cases, only one technique is implemented; however, two or more techniques applied simultaneously may provide higher performance. A methodology that considers multiple design objectives while satisfying system requirements typically utilizes lower resources. Optimization processes and related design techniques applied to high performance ICs are the topic of this paper.

IC development can be functionally separated into two major layers, the design layer and the support layer. The design layer includes the architecture, circuit, and interconnect. The power supply system, clock distribution network, and substrate are related to the support layer. In the literature, a number of local optimization techniques have been published for each separate group of layers. For interconnect, low swing interconnects [1], cascaded buffers [2], repeater insertion [3], shielding [4], differential signaling [5], active regeneration [6], intentional skewing [7], bus swizzling [8], and tapered interconnects [9] are well known design techniques. Each technique trades off power, delay, noise, and area differently. Delay, bandwidth, and power for *RC* and *RLC* interconnects have been investigated in [10]; however, only one design technique, repeater insertion, is used. By combining some of these techniques, more efficient results may be achieved. In [11], two methods, shield and repeater insertion, have been combined to reduce noise within a standard optimization process.

Two different techniques that provide immunity to coupled noise, shield and repeater insertion, have been combined based on resource optimization to exemplify this process. Each of the techniques exhibits different power, delay, noise, and area resource characteristics.

The paper is organized as follows. Shielding, repeater insertion, and coupling noise under resource based optimization are discussed in Section II. Parabolic noise behavior is established and summarized in Section III. In Section IV, simultaneous shield and repeater insertion techniques are compared with only shielding and only repeater insertion. The paper is concluded in Section V.

II. Shield And Repeater Insertion

Placing a shield beside and inserting repeaters along a victim line are chosen to exemplify the resource based optimization process. The width of the shield line, and the number and size of the repeaters that minimize coupling noise on the victim line need to be determined while satisfying power, area, and delay requirements. Repeater insertion, shielding, and related resource expressions are described in the following section. As compared to [11] where a *cost* function is used, this work is based on resource optimization. In [11], the noise is modeled based on Devgan's metric [12], while in this paper the shielded noise model is based on [13].

A. Repeater Insertion

Repeater insertion is a well known design technique to reduce the delay required to propagate a signal along a line [3]. The objective is to divide the interconnect into smaller sections, reducing the quadratic delay dependency on length to a linear dependency, thereby reducing the overall delay [14]. If the number of repeaters is too small, the delay due to the interconnect will dominant. If the number of repeaters is too large, the repeater delay dominates. The optimal number of repeaters that minimizes the overall delay has been presented in [3], [10], and [14].

An additional advantage of repeater insertion is reducing the coupled noise from adjacent interconnects. It is impractical, however, to insert excessive repeaters due to delay, power and area constraints.

B. Shielding

Shielding inserts an additional line between a victim line and an aggressor line. A shield line is connected to the power/ground network, filtering the noise from the aggressor away from the victim line. The technique is highly effective, although significant area is required.

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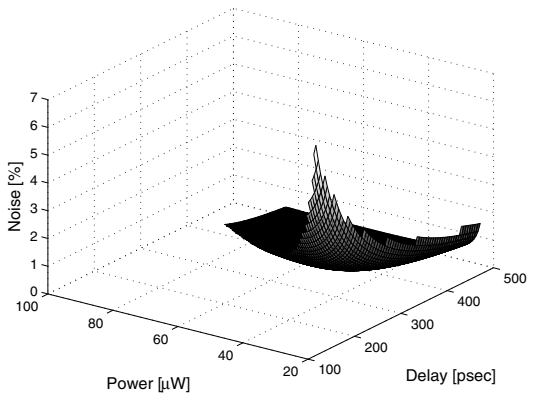

Fig. 1. Noise as a function of power and delay in a system with shields and repeaters.

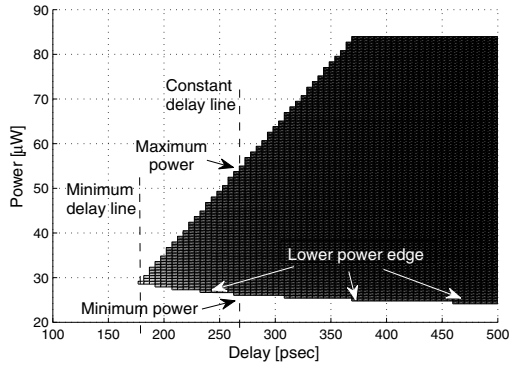

Fig. 2. Top view of Fig. 1. The lighter color represents a larger amount of noise.

C. Coupling Noise with Resource Based Optimization

The resource models are summarized in (1) to (4) and expressed in terms of the resources and variables,

$$power = f_1(h,k), \tag{1}$$

$$delay = f_2(h,k), \tag{2}$$

$$area = f_3(w_{sh},h), \tag{3}$$

$$noise = f_4(w_{sh},k), \tag{4}$$

where k, h, and w_{sh} are, respectively, the number of inserted repeaters along the victim line, ratio between the final and minimal transistor widths, and the width of the shield line. Inverting (1)-(3) and substituting into (4),

$$noise = f_4(area, power, delay), \tag{5}$$

where the noise is expressed as a function of power, area, and delay. The complete form of the analytic expression is presented in [15].

III. Simulation Results

A case study with inserted repeaters and a shielded victim line is considered. The area, power, delay, and noise are evaluated for this system. By increasing the area, the noise is reduced since wider shield lines and additional repeaters are possible. The noise monotonically decreases as a function of area; therefore, the area is set to a constant practical value.

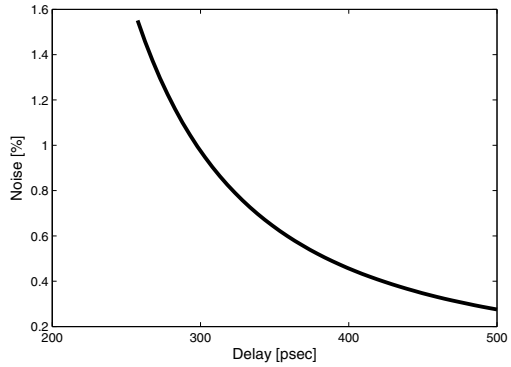

Fig. 3. Noise as a function of delay at a constant power and maximum allowed area.

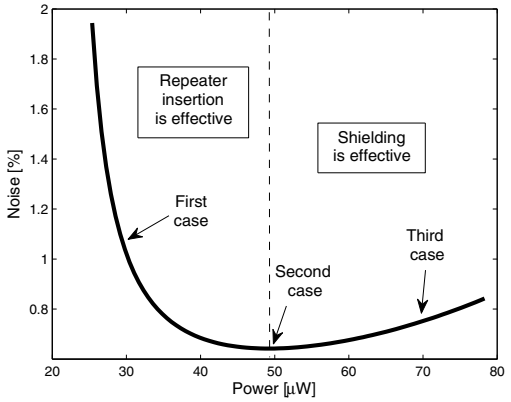

Fig. 4. Noise as a function of power at the maximum allowed delay and area.

A graph presenting *noise* as a function of *power* and *delay* is illustrated in Fig. 1. Note the relationship among power, delay, and noise, generating a tradeoff surface, permitting different tradeoffs to be made. The top view of the graph illustrated in Fig. 1 is shown in Fig. 2, where the lighter region indicates a higher noise. For this design case, a 180 psec delay is the minimum delay, as depicted in Fig. 2. This delay is not the same as determined in [3], [10] and [14], since power, noise, and area are also considered. The lower edge of the power curve, illustrated in Fig. 2, saturates to a minimum power level. This curve does not reach zero due to the minimum power required to charge the line capacitance.

In Fig. 3, noise is presented as a function of delay at a constant power and maximum allowed area. An increase in delay will reduce the coupling noise, since more repeaters or wider shield lines are available. The exponentially increasing curve, illustrated in Fig. 3, indicates the noise penalty from choosing a value close to the minimum delay. Note that by relaxing the delay constraint, the coupling noise is significantly smaller.

Noise as a function of power at the maximum allowed delay and area is illustrated in Fig. 4. The graph consists of two different regions. The noise is reduced by increasing the power

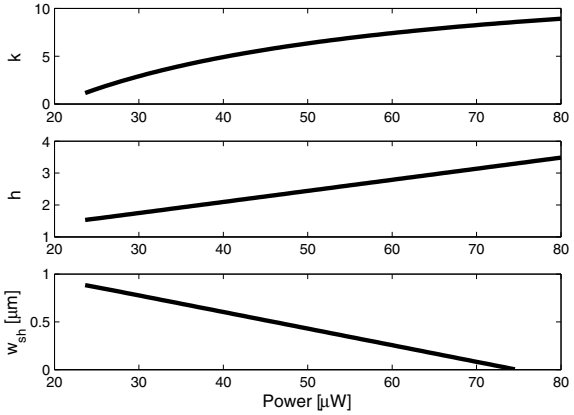

Fig. 5. k, h, and w_{sh} as a function of power at the maximum delay and area.

TABLE I
THREE DESIGN CASES SHOWN IN FIG. 4 EVALUATED IN SPICE

	k (number of repeaters)	h·0.5 (width of the repeaters)	w_{sh} (width of the shield line)
First case	2	0.8 μm	0.8 μm
Second case	6	1.2 μm	0.5 μm
Third case	8	1.5 μm	0.1 μm

and the noise increases at a higher power. This parabolic noise behavior can be exploited to determine the minimum noise for this circuit. To motivate these results, three cases, depicted in Fig. 4, have been evaluated. The first case, at a power of 29 μW, produces a 1.1% noise (normalized to V_{dd}). The noise voltage in this case is 21 mV. The noise for the second case located at a power of 49 μW is 0.65% (or 11.5 mV). The final case at a power of 70 μW produces 0.8% (or 14 mV) noise. The 20 mV noise difference between the first and second case exemplifies the tradeoff. The noise difference between the second and third case is smaller, but significant.

The effects of k (number of repeaters), h (width of the repeater), and w_{sh} (width of shielding line) as a function of power are illustrated in Fig. 5. The area and delay are maintained at maximum values. With an increase in the power, the number and width of the repeaters increase at a different rate, maintaining a constant delay. Simultaneously, the width of the shield lines decreases, providing more space for larger repeaters while maintaining a constant area. The larger number of repeaters reduces the noise; however, the reduction in the shield width increases the noise. Adding repeaters at lower power levels reduces the noise more than adding repeaters at higher power levels. Hence, at lower power levels, the most efficient noise reduction technique is repeaters, while at higher power levels, the most efficient noise reduction technique is shield lines, as illustrated in Fig. 4. Both of these techniques reduce the noise, exhibiting a parabolic noise behavior, allowing the minimum noise design to be determined. In this case, the minimum noise is 49 μW total power and contributes only 0.65% (or 11.5 mV) noise.

This concept is evaluated on a system composed of a victim interconnect with several repeaters and a shield line. Three design cases, listed in Table I, are considered. The power, delay, and noise are determined from SPICE simulations. The analytic model and SPICE results are compared in Fig. 6 and

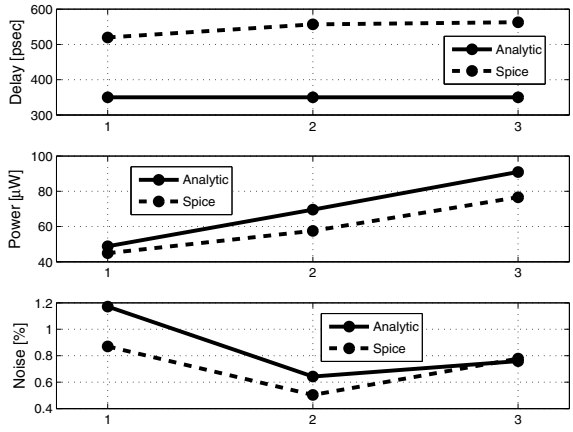

Fig. 6. Delay, power, and noise for three different design cases. Analytic and SPICE results are compared.

Table II for three design cases, listed in Table I and depicted in Fig. 4. In Table II, the change in delay, power, and noise is determined relative to the minimum noise design case (second case). In the analytic model, the delay is maintained constant; however, small changes in the delay are noted from SPICE. The power resulting from the analytic model and SPICE is similar. The noise evaluated from SPICE also exhibits good agreement with the analytic model. The SPICE results demonstrate the same parabolic noise behavior when simultaneously applying shield and repeater insertion. The noise is lower in the second design case than the first and third design cases, confirming the parabolic noise behavior. The minimum noise is achieved with simultaneous shield and repeater insertion, while satisfying power, area, and delay constraints.

IV. Comparison Of Shield And Repeater Insertion Techniques

A comparison of simultaneous shield and repeater insertion with only shielding (without repeater insertion) and only repeater insertion (without shielding) is discussed in this section. The same resources are compared: power, delay, area, and noise. A constant area is assumed.

In only shielding, all of the area except for the victim line and spacing is dedicated to the shield line. The reduction in coupled noise is only due to the shield line, resulting in 0.81% (or 14.5 mV) noise coupling. The power dissipation is minimal, only 22.2 μW, since dynamic power is only dissipated by the line and driver repeater, and a small amount of short-circuit power to switch the driver repeater. The delay, however, increases to 515 psec.

In the repeater insertion case (without shielding), emphasis is placed on achieving a target delay of 350 psec, as in the simultaneous shield and repeater insertion case. Consequentially, minimum noise is targeted. To minimize the noise, the largest number of repeaters is required. To satisfy the target delay and area constraints, the highest number of repeaters is determined to be ten. In this case, all of the area is occupied by the repeaters. The noise achieved is equal to 0.725% or 13 mV. The power consumption for this system is comparably high,

TABLE II
ANALYTIC AND SPICE RESULTS FOR THE THREE DESIGN CASES FROM TABLE I AND FIG. 4

		k	h	w_{sh}	Delay [psec]	Change in Delay [%]	Power [μW]	Change in Power [%]	Noise [mV]	Change in Noise [%]
Analytic	First case	2.04	1.63	0.83	350	0.0	28.9	41.1	21.1	82.5
	Second case	5.91	2.33	0.48	350		49.0		11.6	
	Third case	8.04	3.04	0.13	350	0.0	69.6	42.1	13.7	18.2
SPICE	First case	2	1.63	0.83	520	6.6	44.9	22.0	15.7	73.0
	Second case	6	2.33	0.48	557		57.6		9.1	
	Third case	8	3.04	0.13	563	1.1	76.6	33.1	14.0	54.5

TABLE III
COMPARISON AMONG SHIELDING, REPEATER INSERTION, AND SHIELD AND REPEATER INSERTION TECHNIQUES

	Noise	Area	Power	Delay
Only Shielding	14.5 mV	4.15 nm^2	22.2 μW	515 psec
Only Repeaters	13.0 mV	4.15 nm^2	86.8 μW	354 psec
Simultaneous Shield and Repeater Insertion	11.5 mV	4.15 nm^2	49.0 μW	350 psec

86.7 μW. The results are compared in Table III.

Note in Table III that the noise is similar among all of the cases. A noise advantage of two to three millivolts is determined for the simultaneous shield and repeater insertion case. If the delay is not constrained, the more appropriate technique is shielding only, since minimal power is dissipated in this case. In the cases where delay is also considered, the only repeater insertion technique achieves the target delay with comparable noise performance. The power dissipation, however, is almost twice that of the simultaneous shield and repeater insertion case.

V. CONCLUSIONS

Simultaneous shield and repeater insertion is considered under resource based optimization. The methodology is used to investigate area, power, delay, and noise tradeoffs. The coupled noise as a function of power with maximum allowed delay and area is evaluated, demonstrating a parabolic behavior. This approach permits the minimum noise design to be determined. The analytic model exhibits good agreement with SPICE. Over 50% reduction in coupled noise is demonstrated as compared to three design cases by applying this resource based optimization process. To motivate simultaneous shield and repeater insertion, three cases are evaluated and compared: shielding only, repeater insertion only, and simultaneous shield and repeater insertion. The noise performance is comparable among all of these techniques. In only shielding, however, the delay is higher, while in only repeater insertion, the power is higher. In practical cases where the delay, power, and area are constrained, simultaneous shield and repeater insertion exhibits the best performance.

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