Shielding Methodologies in the Presence of Power/Ground Noise

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***Abstract*— Design guidelines for shielding in the presence of power/ground (P/G) noise are presented in this paper. The effect of noise in the P/G network is analyzed for various line lengths, line widths, and interconnect driver resistances. A 2π RLC model is used to investigate the effect of both coupling capacitance and mutual inductance on the crosstalk noise. For a range of shield lengths and widths, a shield line can degrade signal integrity by increasing the crosstalk noise on the victim line. Different physical spacing and shield insertion methods are compared for various parameters in terms of the coupling noise on the victim line for a 65 nm technology node.**

I. Introduction

In deep submicrometer integrated circuits, crosstalk between adjacent interconnect lines has become a primary design issue. With aggressive technology scaling, the local interconnect has become more resistive and capacitive. The global interconnect has become more inductive. Capacitive and inductive coupling has therefore became a significant design issue in global interconnect [1].

Shielding is widely used in integrated circuits to mitigate crosstalk between coupled lines. Two types of shielding methods are considered, passive shielding [2], [3] and active shielding [4]. In passive shielding, the power/ground (P/G) lines are routed as shield lines between critical interconnect to minimize the noise coupled from an aggressor to a victim line. Inserting a shield line between coupled interconnect significantly decreases the capacitive coupling and moderately decreases the inductive coupling. The effect of shielding on the inductive coupling is limited since inductive coupling is a long range phenomenon. The difficulty in forcing the current return path complicates the inductive shielding process. Alternatively, active shielding uses dedicated shield lines which switch depending upon the switching pattern of the adjacent interconnect lines. Active shielding requires a dedicated logic circuit to determine the switching pattern on a shield line to minimize either capacitive or inductive coupling [4]. The additional logic circuitry naturally requires more area and power.

Although P/G networks mitigate coupling noise, the P/G shield lines themselves can be noisy. This noise is dI/dt noise. With increasing device densities, the P/G noise voltage can be more than 20% of the supply voltage [5]. Since the shield line is often closer to the victim line than the aggressor line, the effect of the P/G noise on the victim line can be more destructive than the crosstalk noise coupled from the aggressor line to the victim line.

Another method to reduce crosstalk is to increase the physical space between the aggressor and victim lines without inserting a shield line. Tradeoffs between the two methods, shield insertion and physical spacing, are discussed in [6] without considering P/G noise on the shield lines. The P/G noise, however, can significantly affect the decision criteria between shielding and spacing as discussed throughout this paper. The objective of this paper is to investigate the effect of P/G noise on the shield lines for a passive shielding methodology. Comparisons between physical spacing and shield insertion techniques are provided. The results of this paper can be used to choose between spacing or shielding methodologies in a noisy environment.

The rest of the paper is organized as follows. A description of the interconnect and P/G noise models is presented in Section II. In Section III, the effects of various design parameters characterizing the interconnect and shield lines in terms of the crosstalk noise occurring on the victim line are investigated. Finally, the paper is concluded in Section IV.

II. Interconnect and Power/Ground Noise Models

A typical interconnect model with a shield line inserted between the aggressor and victim lines is depicted in Fig. 1. The shield line is a P/G line routed between the aggressor and victim lines to mitigate coupling from the aggressor to the victim. The shield line is modeled as a single voltage source at the near end.

The objective is to compare the effect of inserting shield lines and physical spacing on the coupling noise at the far end of the victim line (the sense node). The ratio of the total coupling noise at the sense node with a shield, $V_{sense\_node\_with\_shielding}$, to the total coupling noise with physical spacing, $V_{sense\_node\_with\_spacing}$, is used as a decision criterion. Note that the area is maintained the same for both shield insertion and physical spacing methods.

$$K = \frac{V_{sense\_node\_with\_shielding}}{V_{sense\_node\_with\_spacing}}. \quad (1)$$

If $K < 1$, inserting a shield line between the aggressor and victim lines is preferable because the crosstalk noise at

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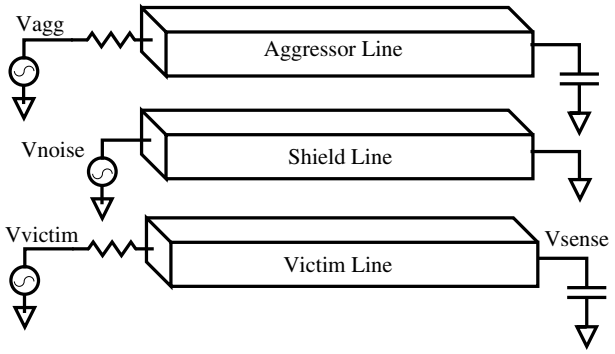

Fig. 1. A global interconnect model with an aggressor line, shield line, and victim line. The aggressor and victim lines are modeled with a driver resistance and load capacitance. The P/G noise is modeled as a single voltage source at the near end of the shield line.

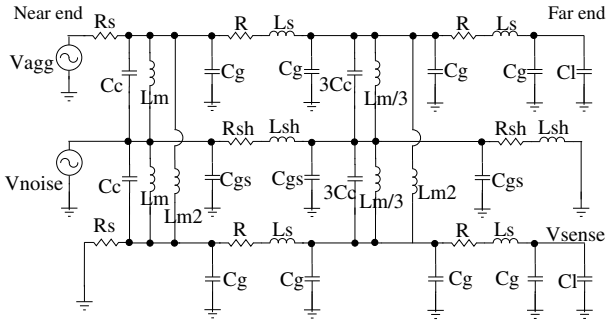

Fig. 2. 2π RLC interconnect model with coupling capacitances and mutual inductances.

the sense node is smaller with a shield than with additional spacing. If $K > 1$, extra space is preferable. $K = 1$ is therefore treated as a design threshold. Spacing is more efficient above the threshold, and shield insertion is more efficient below the threshold.

To accurately investigate the effect of inductive and capacitive coupling, the 2π RLC interconnect model [3] shown in Fig. 2 is used. The aggressor and victim line parameters, R_s, R, C_g, C_c, C_l, and L_s, represent the interconnect driver resistance, line resistance, ground capacitance, coupling capacitance, load capacitance, and line self-inductance, respectively. Additional parameters, R_{sh}, L_{sh}, C_{gs}, L_m, and L_{m2}, represent the shield line resistance, shield line self-inductance, shield line-to-ground capacitance, mutual inductance between the shield line and the aggressor and victim lines, and mutual inductance between the aggressor and victim lines, respectively. These circuit parameters have been extracted using the IBM Electromagnetic Field Solver Suite Tools (EIP) [7] for the 65 nm technology node [8]. The operating frequency is 10 Ghz and the supply voltage is 1 volt.

III. Effects of Design Parameters on the Crosstalk Noise Voltage

The effects of the design parameters on the crosstalk noise voltage is discussed in this section. The effects of the interconnect line length and shield line width on the crosstalk noise are discussed in Sections III-A and III-B, respectively. In Section III-C, the effect of the ratio of the interconnect line resistance R_{line} to the interconnect driver resistance R_s on the coupling noise voltage is explored. The effect of the ratio

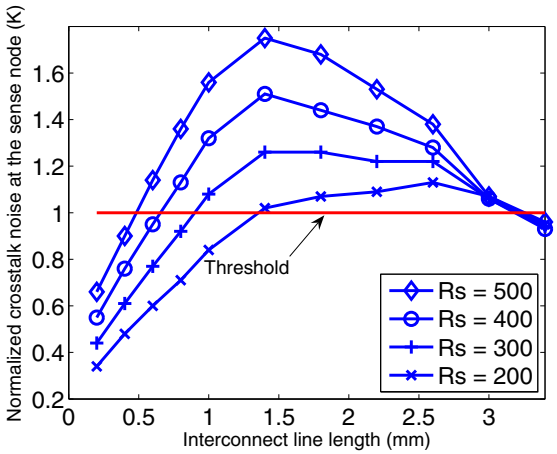

Fig. 3. The effect of interconnect line length on crosstalk noise at the sense node for various driver sizes.

of the ground capacitance to the coupling capacitance on the coupling noise is discussed in Section III-D.

A. Effect of Line Length on the Crosstalk Noise Voltage

The length of the global interconnect increases with technology scaling, producing signal integrity problems. The global interconnect can be longer than 4 mm [9]–[11]. Repeater insertion minimizes the crosstalk noise and delay of the long interconnect. Inserting repeaters along the wide and thick global interconnects, however, can cause wire and via congestion as well as dissipate high power [11]. The wire resistance, ground capacitance, and self-inductance of a wire and the coupling capacitance and mutual inductance between neighboring wires increases with longer line length.

For the interconnect model shown in Fig. 1, the coupling noise voltage at the sense node is compared to shield insertion and physical spacing for different interconnect lengths and driver resistances. These results are illustrated in Fig. 3. The solid line at K=1 is the threshold line. When K=1, the same noise at the sense node occurs for both physical spacing and shield insertion.

The peak value of K occurs at the interconnect length of 1.4 mm. K monotonically increases for interconnect lines shorter than 1.4 mm and monotonically decreases for interconnect lines longer than 1.4 mm. The crosstalk noise occurring at the sense node with physical spacing and shield insertion is shown in Figs. 4a and 4b, respectively. The crosstalk noise at the sense node monotonically decreases with longer interconnect length for physical spacing. The crosstalk noise with shield insertion, however, exhibits a non-monotonic behavior. The cause of the non-monotonic behavior of the crosstalk noise is that for a short interconnect line, the coupling capacitance and mutual inductance between adjacent lines dominate the line resistance. The crosstalk noise at the sense node begins to decrease as shown in Fig. 4b once the distance between the near and far end of the interconnect line is above some length (*i.e.* 1.4 mm for the 65 nm global interconnect). Also note in Fig. 4 that inserting a shield line mitigates the effect of the driver resistance on the crosstalk noise. The effect of the driver resistance is further discussed in Section III-C. As

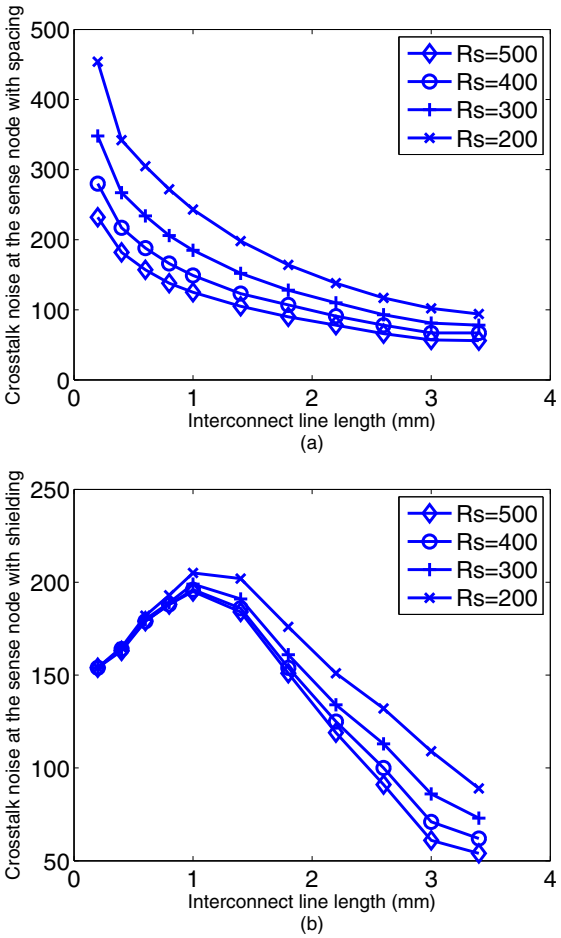

Fig. 4. Crosstalk noise occurring at the sense node for a) physical spacing and b) shield insertion. Note that the behavior of the crosstalk noise with shield insertion is non-monotonic with increasing length.

a result, shield insertion is preferable for shorter lines and spacing is preferable for longer lines.

B. Effect of the Shield Line Width on the Crosstalk Noise Voltage

The effect of the cross-sectional area of the shield line on the coupling noise is discussed in this subsection. As the lines become narrower and thinner, the line resistance increases and the line self-inductance slightly decreases, making the lines more resistive. To determine the effect of the cross-sectional area of the shield line on the reduction in crosstalk noise, the width of the shield line is evaluated for different driver resistances and interconnect lengths. These results are shown in Fig. 5 for a 1 mm interconnect line.

As the width of the shield line increases, the shield line becomes less resistive, the self- and mutual inductances slightly increase, and the line-to-ground shield capacitance increases. The coupling capacitance between the shield line and the adjacent interconnect lines does not significantly change. When the physical space between the aggressor and victim lines is increased without inserting a shield line, the mutual inductance and the coupling capacitance decrease while the line-to-ground interconnect capacitance increases. A comparison of shield

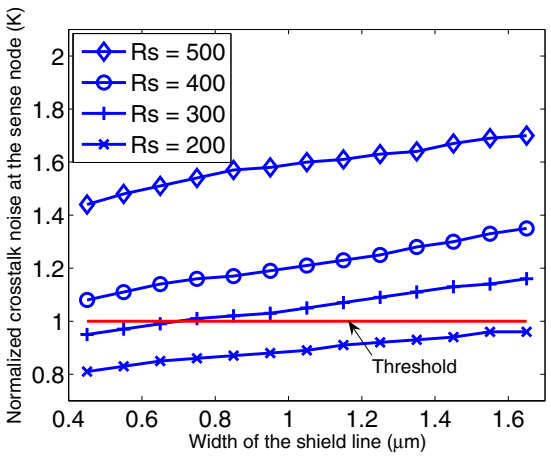

Fig. 5. The effect of shield line width on the crosstalk noise for a 1 mm interconnect line for 0.45 μm $<$ width $<$ 1.65 μm. Note that above the threshold line, inserting a shield line degrades the signal integrity.

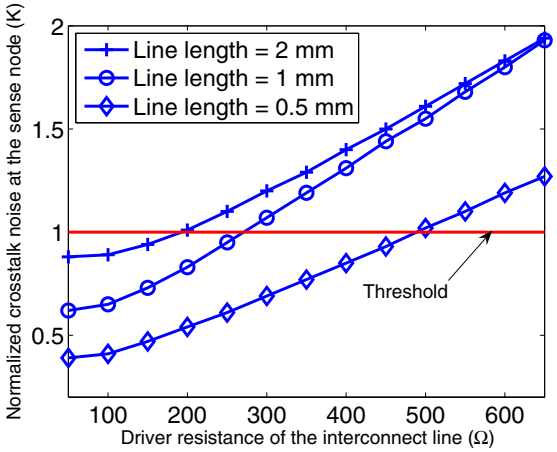

Fig. 6. Effect of R_{line}/R_s on the crosstalk noise voltage. The length of the interconnect line is 0.5 mm, 1 mm, and 2 mm and the driver resistance is evaluated from 50 Ω to 650 Ω.

insertion and physical spacing is shown in Fig. 5. Note that the separation between the aggressor and victim lines remains the same for both the physical spacing and shield insertion methods.

As the width of the shield line increases, shield insertion becomes less effective. Although increasing the width of the shield line mitigates coupling from the aggressor node to the sense node, coupling of the P/G noise to the sense node increases due to the decrease in resistance of the shield line.

C. Effect of R_{line}/R_s on the Crosstalk Noise Voltage

The driver resistance has a substantial effect on the design of the global interconnects. As previously noted, the global interconnect lines are wide and thick, making the line low resistance as compared to the driver resistance of the interconnect lines. The effect of R_{line}/R_s is shown in Fig. 6 for various interconnect line lengths.

The driver resistance is evaluated for different output impedances (50 Ω to 650 Ω). As the driver resistance increases, physical spacing becomes more efficient than shield insertion. When the driver resistance is larger, coupling from the P/G

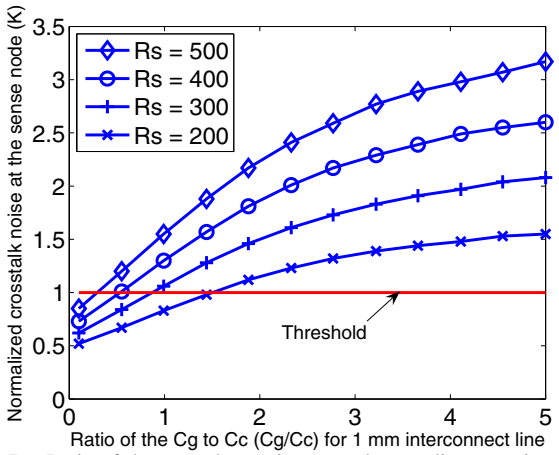

Fig. 7. Ratio of the ground capacitance to the coupling capacitance versus the normalized crosstalk noise when a P/G line is routed as a shield line. The interconnect length is 1 mm.

noise becomes greater than coupling from the aggressor. The reason is that the shield line exhibits no driver resistance so the P/G noise propagates to the sense node along the shield line whereas the aggressor noise voltage is attenuated by the large driver resistance at the near end of the aggressor line. Alternatively, when the driver resistance is small, coupling from the aggressor noise increases and starts to dominate the P/G noise, making shield insertion preferable. Another observation is that the length of the interconnect significantly affects the speed, power, and area characteristics when choosing between spacing and shielding methodologies in a noisy environment. Spacing is preferable when the interconnect line becomes longer whereas shielding is preferable for shorter interconnect lines, as shown in Fig. 6.

D. Effect of the Ratio of the Ground Capacitance to the Coupling Capacitance on the Crosstalk Noise Voltage

The coupling capacitance between adjacent interconnect strongly depends upon the switching activity of the wires [12]. When the signals driving the adjacent lines switch in the same direction, the coupling capacitance is the same as the coupling capacitance between two adjacent quiet lines. When the signals driving the adjacent lines switch in the opposite direction, the coupling capacitance between the adjacent lines is two times the capacitance when only one of the adjacent lines is switching [12], [13]. The effect of the ratio between the line-to-ground capacitance and the coupling capacitance has been evaluated for active and passive shielding structures [14], but without considering P/G noise on the shield lines. The effect of the ratio between the line-to-ground capacitance and the coupling capacitance on the crosstalk noise at the sense node for different driver resistances is depicted in Fig. 7. When the coupling capacitance is greater than the line-to-ground capacitance, shield insertion is more effective than additional spacing. As the line-to-ground capacitance becomes greater than the coupling capacitance, physical spacing becomes more efficient than shield insertion. For example, when R_s is equal to 300 Ω, spacing is preferred when C_g/C_c is greater than 0.9 for a 1 mm line. Shield insertion is more efficient for thicker lines. Alternatively, spacing is preferable for wider lines as the line-to-ground capacitance increases with wider interconnect.

IV. Conclusions

Shielding methodologies in the presence of P/G noise has been introduced since with scaling, P/G noise has become a significant design issue. The noise on the shield line reduces the efficiency of shielding because this noise couples to the victim lines, degrading the signal integrity. Shield insertion and physical spacing between adjacent interconnect lines are compared for various interconnect lengths and shield widths. Extra space is shown to be more efficient for shorter and narrower lines while shield insertion is preferable for longer and thicker lines. The effect of the driver resistance of the interconnect line on the crosstalk noise is also investigated. Shielding is preferable for smaller driver resistances and physical spacing is preferable for higher driver resistances. The ratio of the ground capacitance to the coupling capacitance is explored in terms of mitigating coupling noise. Shield insertion is preferable for those lines with higher coupling capacitance than line-to-ground capacitance.

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