Globally Integrated Power and Clock Distribution Network

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***Abstract*— The global networks within a conventional integrated circuits (IC) consists of three major types: power, ground, and clock networks. These three networks consumes most of the metal resources in the highest metal layers. The signals traversing the power and clock distribution networks are fundamentally different in terms of signal frequency and current flow. Combining the power and clock network into a globally integrated network is therefore possible. In this paper, the general concept of a globally integrated power and clock (GIPAC) system is proposed. The circuitry supporting this GIPAC system is also presented. Simulation results based on a 90 nm CMOS technology demonstrate the potential of GIPAC.**

I. Introduction

Further increases in the density and performance of integrated circuits (IC) require more complicated global interconnects, such as power, ground, and clock networks. On-chip metal resources are limited [1], further constraining the design of these global interconnect networks. These global networks require a large portion of the overall metal resources [2].

The major networks that consume most of the top metal resources are the power, ground, and clock networks. Each network is carefully designed to provide optimal circuit performance. These networks are typically designed independent of each other (power/ground network and clock network) since each network exhibits different characteristics and constraints. This approach results in high utilization of on-chip resources since each network is typically routed to every individual block, circuit, or gate within an IC.

For those circuits where the clock signal is generated off-chip, the clock and power signals may be integrated to eliminate the on-chip global clock distribution network. This combined network is named here as a *globally integrated power and clock* (GIPAC) distribution network. The power and clock signals are later separated from the GIPAC network into two different local networks using passive filters.

Signal splitting is fairly common in electrical and communication systems. Different signals are modulated, simultaneously transferring these signals over a single medium, and later demodulated [3]. A typical home phone system carries power and voice signals over the same network. Filters inside the device demultiplex the signals, routing the signals accordingly. The internet infrastructure also uses phone lines, sharing resources with the global phone network. Broadband communication over the power lines [4] further supports this approach of sharing a common global network.

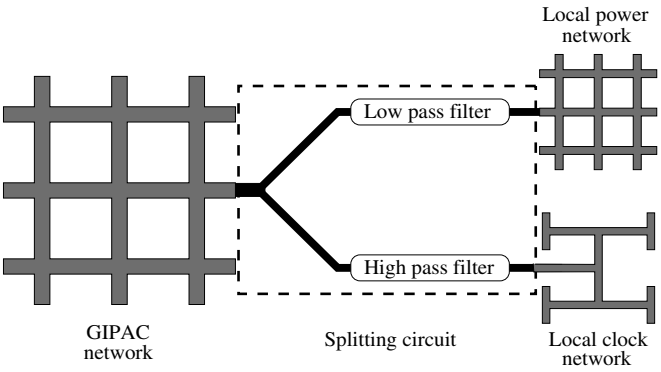

Fig. 1. Globally integrated power and clock (GIPAC) distribution network. A low and high pass filter can be used to separate the GIPAC signal into local power and local clock signals.

TABLE I
Characteristics of power and clock signals.

	Power signal	Clock signal
Frequency	Very low	High
Current	Very high	Medium
Load	Very low resistance	Highly capacitive

The two signals, power and clock, are fundamentally different signals. A primary difference between the power and clock signals is the operating frequency. While the clock signal exhibits a high frequency component, the power signal is ideally DC. These two signals can therefore be separated with a high and low pass filter, as illustrated in Fig. 1. Additionally, the power signal carries high current, while high current is not required for the clock signal. Different characteristics of these two signals, listed in Table I, distinguish the design of the high and low pass filters (the splitting circuit).

Previous research on power and clock networks typically only consider a single network at a time. Focusing on power networks, supply network impedance is a primary issue [5]. The size and placement of the decoupling capacitors are

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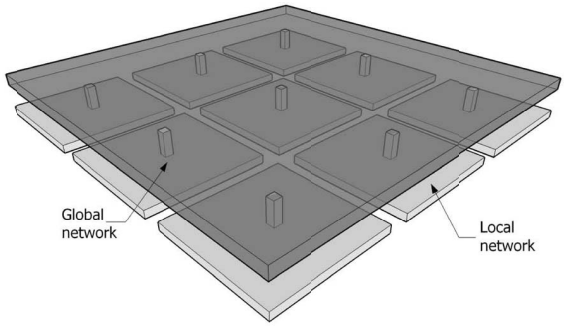

Fig. 2. Integrating the GIPAC network into an SoC. The GIPAC network is represented by the top layer, while the local networks with separate power and clock networks are located on the bottom layer.

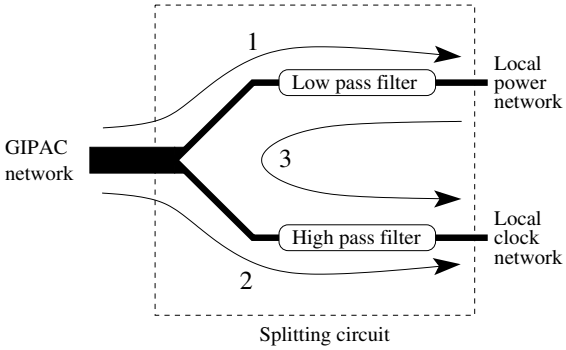

Fig. 3. Noise is the major issue for the GIPAC network. The three noise paths are shown in the figure. The first path represents noise coupling from the GIPAC network into the local power network; the second path indicates noise coupling from the GIPAC network into the local clock network; and the third path is noise injected from the local power network into the clock network.

also important [6]. Different styles have been proposed for designing the power distribution network. The most common are routed [7], mesh [8], planes [9], and interdigitated [10] structures. Each of these structures trades metal resources for performance differently. The design and analysis of power distribution networks are summarized in [1].

For clock network design, the focus is typically on power, skew, and jitter. Clock gating [11] is a widely used technique to reduce power dissipation. To achieve lower skew between two sequentially-adjacent registers, the clock network is often designed as a symmetric structure, such as an H-tree [12]. Different aspects of the clock distribution network are summarized in [13].

In [14], clock and power distribution networks are considered simultaneously to enhance the immunity to power supply noise. However, no research on utilizing the same global network for both power and clock distribution has been described in the literature. Combining these global networks is the focus of this paper.

The paper is organized as follows. The high level design and related issues are discussed in Section II. In Section III, the strategy and related circuits for separating the power and clock signals are described. The circuit is evaluated in Section IV. The paper is concluded in Section V.

II. High Level Design

The GIPAC structure is proposed to efficiently distribute power and clock within a system-on-chip (SoC). In Fig. 2, the GIPAC network is depicted within an SoC, where multiple on-chip domains are characterized as a local network and the entire IC-based system as a global network. In this case, the GIPAC network distributes the integrated power and clock network over the entire circuit, while localized systems produce separate local power and clock networks. The GIPAC structure reduces the requirement for metal resources, yielding higher integration and functionality.

Noise is the primary issue in the design of a GIPAC network. The noise originates from three main sources, as illustrated in Fig. 3:

1) Noise from the GIPAC into the power network
2) Noise from the GIPAC into the clock network
3) Noise from the power network into the clock network

Since the GIPAC network combines the clock and power signals, a fraction of the clock signal that propagates through the low pass filter is treated as noise within the power network. Two strategies exist for reducing these noise sources, a more effective low pass filter or a higher frequency clock signal. The drawback in a more effective low pass filter is increased area. The disadvantage of providing a higher clock frequency is the requirement for higher speed and lower power.

Noise within the GIPAC also affects the clock network; however, only high frequency noise is significant since a high pass filter eliminates low frequency noise. The remaining noise produces jitter in the clock signal.

The third noise path, noise propagation from the power network into the clock network, is also considered. The circuitry powered by the power network switches at the same frequency as the clock signal, creating high frequency noise within the power network which propagates into the clock network. The different current demands from the power network also affect the clock network; a solution is therefore required to eliminate this noise mechanism.

III. Proposed GIPAC Splitting Circuit

A. Theoretical background

The GIPAC splitting circuit, called here a splitter, is the primary component of the integrated power and clock network system. The function of the splitter is to separate the signals while minimizing the noise between the global and local networks. The proposed GIPAC splitter circuit is shown in Fig. 4. Each *RC* pair behaves as a low pass filter, where the resistor is implemented as a polysilicon resistor and the capacitor as an MOS transistor. The circuit is designed assuming a 90 nm CMOS technology. The input signal supplied to the GIPAC network as a function of time t is

$$input(t) = A + \alpha \cdot sin(2\pi f_{clk} t), \quad (1)$$

where A is the supply voltage. α and f_{clk} are, respectively, the amplitude of the signal used to generate the clock signal and

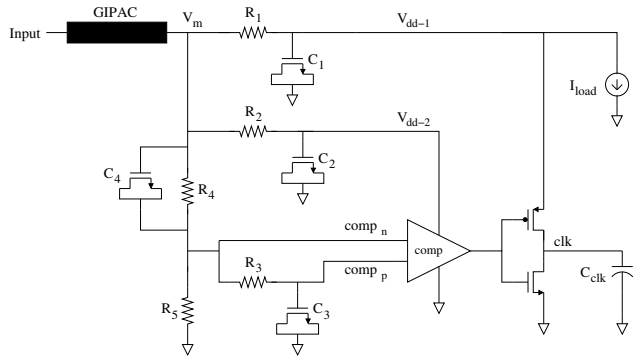

Fig. 4. Proposed GIPAC splitter circuit. Each *RC* pair behaves as a low pass filter. The value of R and C are based on the noise requirements, where the resistors are implemented as polysilicon resistors and capacitors as MOS transistors. C_{clk} and I_{load} are the clock network load and current for the entire circuit, respectively.

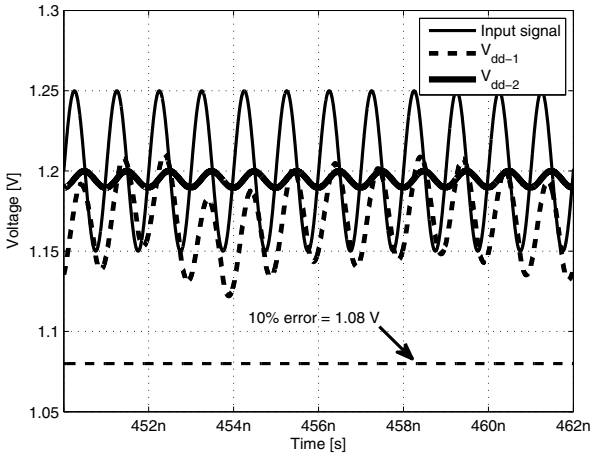

Fig. 5. Transient simulation of the GIPAC input, output V_{dd-1}, and output V_{dd-2} signals. The ripples on the power lines are considered as noise.

the clock signal frequency. The two subsections below describe the generation of the power and clock signals, respectively.

1) Generating the power signal. The input signal propagates through the GIPAC network and arrives at the splitter, as illustrated in Fig. 4. The R_1C_1 filter is a low pass filter that removes the sinusoidal waveform from the input signal, maintaining only the DC portion of the signal. The output signal from this filter is V_{dd-1}. This filter can also be implemented as a higher order filter to improve the quality of the V_{dd-1} signal. Since high current typically propagates through this filter, the R_1 component is of low value, requiring a higher value for C_1. A low value of R_1 is necessary to maintain a high voltage at V_{dd-1}, since a voltage divider is created between R_1 and the local power network.

The R_2C_2 filter is similar to the R_1C_1 low pass filter; however, due to the lower current, R_2 is significantly higher than R_1, permitting C_2 to be smaller. The cut-off frequency for the second filter is lower than the first filter, reducing the noise at the output of the second filter. The output signal of the second low pass filter is called V_{dd-2}. The R_1C_1 and R_2C_2 filters can also be implemented as a single low pass filter, reducing overall area. The switching noise on the power lines however would be injected directly into the clock signal, significantly increasing the clock jitter. Separate *RC* filters are therefore used to reduce the noise coupled from the power network into the clock network (the third noise path depicted in Fig. 3).

2) Generating the clock signal. The clock signal is produced in several stages. The DC component of the signal V_m is initially divided by two (in Fig. 4, labeled as a $comp_n$ signal). The $comp_p$ signal is generated by filtering the $comp_n$ signal with the R_3C_3 low pass filter. This configuration generates two signals with the same DC level; therefore, comparing (or amplifying the difference between) these two signals produces a clock signal with a 50% duty cycle. The C_4 capacitor passes an AC signal to the input of the comparator, creating a voltage divider at node $comp_n$. By increasing C_4, the AC signal is less attenuated; albeit, requiring more area. The buffer at the output of the comparator adjusts the voltage to V_{dd-1}. This buffer can be implemented as cascaded buffers depending upon the load. The comparator utilizes a self-biased structure [15].

B. RC filter values

The R and C values for the low pass filters are based on the DC and AC noise requirements,

$$noise_{dc} = \frac{R \cdot I_{max}}{V_{dd}} \cdot 100, \tag{2}$$

where V_{dd}, I_{max}, and $noise_{dc}$ are the required power supply voltage, maximum current, and per cent of the allowed DC noise on the power network.

$$noise_{ac} = \frac{2\alpha \left| \frac{1}{1+Rj2\pi f_{clk}C} \right|}{V_{dd}} \cdot 100. \tag{3}$$

By increasing C, enhanced noise reduction can be achieved; however, the penalty is the area required to implement the capacitor, producing a tradeoff between noise and area. The output buffer after the comparator is a cascaded buffer structure to drive a large capacitive load.

IV. Simulation Results

The proposed GIPAC network and splitter are designed using a 90 nm CMOS technology, with a power signal at 1.2 volts and a clock signal frequency of 1 GHz. The simulation is evaluated with the current switching with a normal random distribution between 0 and 100 mA. A transient simulation of the input, V_{dd-1} output (to power the entire circuitry), and V_{dd-2} output (to power the clock comparator) are illustrated in Fig. 5. Power signal generation is accomplished by propagating the GIPAC output signal V_m through the first low pass filter. Depending upon the current requirements, the DC level of the power network is shifted due to the resistive voltage drop across the filter. The second low pass

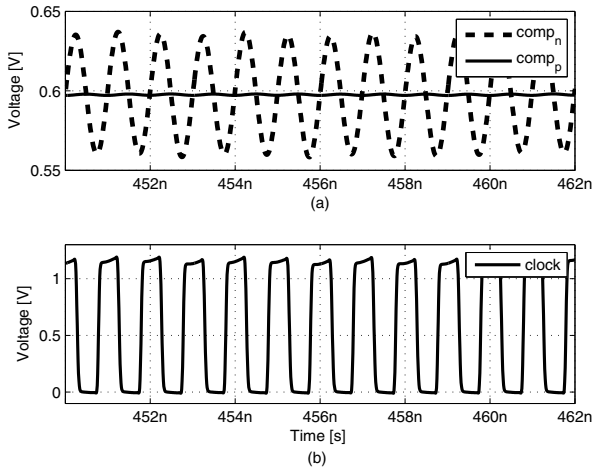

Fig. 6. Transient simulation of the proposed GIPAC splitter circuit. (a) Two signals at the input of the comparator exhibit the same DC level. (b) The generated clock signal drives a 1 pF capacitive load.

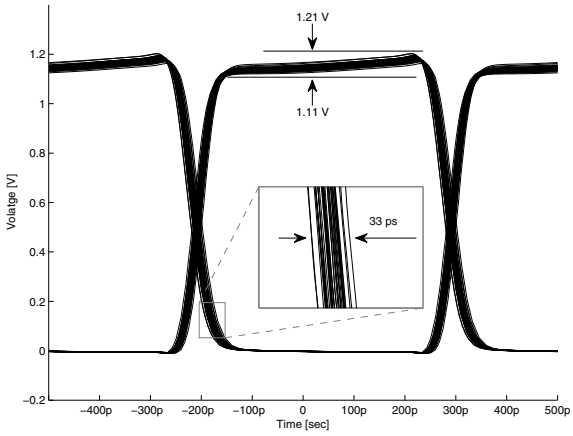

Fig. 7. Eye diagram of the simulated clock signal. The global ground and power networks are assumed to be equal; the difference between the noise on the high and low rails is a product of the GIPAC splitter.

filter generating V_{dd-2} only passes a small current to the comparator, attenuating V_m. The V_{dd-1} signal fluctuates between 1.116 volts and 1.226 volts (110 mV), creating less than 10% error. The V_{dd-2} signal fluctuates between 1.189 volts and 1.201 volts (12 mV), within 1% error.

To generate the clock signal, the GIPAC output signal V_m is divided by two and filtered by the third low pass filter. The two input signals to the comparators are illustrated in Fig. 6(a). The $comp_n$ signal swings between 559 mV and 637 mV, while the $comp_p$ signal only swings between 596 mV and 598 mV due to the third low pass filter. The DC level of both signals is similar, producing a 50% duty cycle clock signal. After the comparator, the signal is amplified by the cascaded buffers, generating the clock signal shown in Fig. 6(b).

An eye diagram of the clock signal is depicted in Fig. 7. The impedance of the global ground and power networks is assumed to be equal; therefore, additional noise on the high rail in the eye diagram is a result of integrating the power and clock signals. As shown in the eye diagram, the voltage fluctuates on the high rail between 1.11 volts and 1.21 volts, producing about 8% error which results in a clock jitter of 33 ps.

V. Conclusions

A general approach for combining the global power and clock networks into a single integrated network is proposed in this paper. Replacing two global networks with one integrated network provides increased integration and functionality. Simulation results, based on a 90 nm CMOS technology, successfully demonstrate splitting the GIPAC output signal into two separate clock and power signals. Noise issues are considered and different tradeoffs are investigated for the proposed integrated power and clock network.

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