Methodology for Multi-Layer Interdigitated Power and Ground Network Design

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Abstract— **Higher operating frequencies and greater power demands have increased the requirements on the power and ground network. Simultaneously, due to the larger current loads, current densities are increasing, making electromigration an important design issue. The optimal wire width for an interdigitated power and ground network is based on the resistive and inductive (both self- and mutual) impedance. In this paper, a methodology for optimizing a multi-layer interdigitated power and ground network is presented, reducing the current density and impedance of a network. Based on 65 nm, 45 nm, and 32 nm CMOS technologies, the optimal width as a function of metal layer is determined for different frequencies, suggesting important trends for interdigitated power and ground networks.**

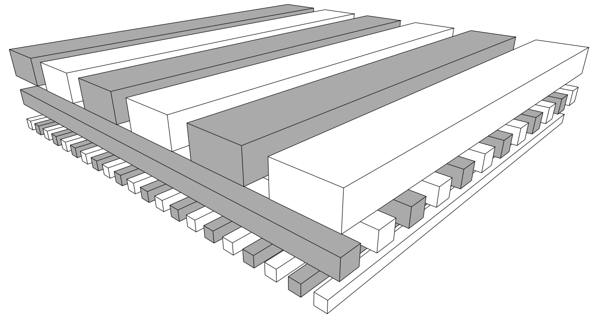

Fig. 1. Global interdigitated P/G distribution structure. The darker and lighter lines represent, respectively, the power and ground lines.

I. INTRODUCTION

With high operating frequencies and scaled geometries, the power and ground (P/G) distribution network requires greater design optimization to effectively provide higher current flow. These higher currents increase voltage losses within the P/G network, while the power supply voltage is decreasing with advanced technologies, providing lower noise margins.

With flip-chip packaging, the package inductance is reduced [1], making the on-chip inductance more significant. Since voltage variations within a P/G network are due to *IR* [2] and $L\frac{di}{dt}$ [3] voltage drops, the effective resistance and inductance are the primary foci of the optimization process. At higher frequencies, the inductive impedance is dominant, requiring accurate estimation of the effective inductance.

An interdigitated P/G distribution network structure where a few wide lines are replaced by a large number of narrow lines is often used to reduce the inductive effect [4], [5]. Different P/G structures have been compared in [6], where the interdigitated structure is shown to achieve the greatest reduction in inductance.

An interdigitated P/G distribution structure is typically located on several metal layers. Each layer consists of interdigitated power and ground wires, where the direction of the wires is perpendicular to the direction of the wires in the previous layer, as depicted in Fig. 1. Routing flexibility and reduced inductance are two primary advantages of an interdigitated P/G distribution structure. With advancements in technology, additional metal layers are provided, permitting the dedication of several metal layers to the P/G network. Due to electromigration, the maximum current is limited; therefore, a larger number of metal layers passes higher current to the system under the same electromigration constraint.

In this paper, the width that minimizes the impedance of a single metal layer is determined, considering the resistance and inductance (including mutual) of the P/G network. Simultaneously, the current density is reduced for each layer, requiring fewer metal layers for the P/G network.

Several algorithms and techniques to optimize the P/G distribution network have been reported, focusing only on the resistive component [7]. More advanced algorithms based on different optimization techniques have been developed; however, only the package inductance is considered [8], neglecting the on-chip inductance. To consider on-chip inductance in power/ground networks, a technique to simplify the mesh model of the *RLC* power/ground network is proposed [9], assuming the loads are treated as identical current sources. The significance of the on-chip inductance within paired and interdigitated power/ground network structures is described in [10], where the inductance is treated as a local effect. In [11], the inductance model considers the mutual inductance between close and distant power/ground wires for interdigitated structures. Based on this model, a closed-form expression characterizing an interdigitated P/G network structure is determined,

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permitting the optimal width of a power/ground network that minimizes the network impedance to be determined. Based on the optimum width of the power/ground lines, a methodology to lower the impedance and current density for a multi-layer metal system is described in this paper.

The paper is organized as follows. A closed-form expression describing the optimal width for minimum impedance of a single metal layer is presented in Section II. In Section III, a methodology to lower the current density across multiple metal layers is described. Further discussion is provided in Section IV. The paper is concluded in Section V.

II. Single Metal Layer Characteristics

An interdigitated P/G distribution network is typically allocated over an entire upper metal layer, where the network is designed for lowest impedance. The effective resistance of a single layer is

$$R_{eff} = \frac{4l^2\rho\,(w+s)}{Atw}, \tag{1}$$

where ρ, A, t, w, l, and s are the metal resistivity, area, thickness, width, length, and spacing of the specific metal layer within the interdigitated power and ground network.

For constant area, according to (1), wider power and ground wires reduce the effective resistance. With multiple thin lines, large area is consumed by the line-to-line spacing, increasing the effective resistance of the network. From [11], the effective inductance (including the mutual inductance) of a single layer is

$$L_{eff} = \frac{2l^2\mu_0\,(w+s)}{A\pi}\left[ln\left(\frac{w+s}{w+t}\right)+\frac{3}{2}+ln\left(\frac{2}{\pi}\right)\right], \tag{2}$$

where μ_0 is the permeability of a vacuum. The inductance under a constant area constraint behaves opposite as compared to the effective resistance since the mutual inductance is dominant in an interdigitated P/G distribution structure. A greater number of lines increases the mutual inductance, reducing the effective inductance, as described by (2).

Since the effect of the resistive and inductive impedance behaves inversely with increasing width, the objective is to minimize the overall impedance at a specific frequency. The absolute value of the effective impedance as a function of line width is

$$|Z_{eff}(w)| = \sqrt{R^2_{eff}(w)+4\pi^2 f^2 L^2_{eff}(w)}. \tag{3}$$

Since the effective inductance in (2) is a transcendental function of width, no analytic solution can be determined for the wire width that minimizes the effective impedance. A numerical solution based on the Newton–Raphson method is utilized to determine the optimal width,

$$w_{opt} = w_{init} - \frac{|Z_{eff}(w_{init})|\prime}{|Z_{eff}(w_{init})|\prime\prime}, \tag{4}$$

where w_{init} is an initial estimate of the optimal wire width. The initial estimate is determined for an interdigitated structure where the spacing between the power and ground wires is equal to the thickness of the metal. Solving for the root of the derivative of (3), $\frac{\partial|(Z_{eff}(w))_{s=t}|}{\partial w} = 0$, a closed-form solution for the wire width that produces the lowest impedance for $|(Z_{eff}(w))_{s=t}|$ (or the initial estimate of the optimal wire width for $|Z_{eff}(w)|$) is

$$w_{init} = \sqrt[3]{0.91\frac{s\rho^2}{\mu_o^2 t^2 f^2}}. \tag{5}$$

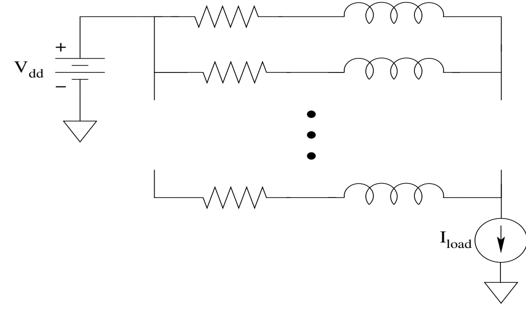

Fig. 2. Multi-layer P/G distribution network model. Each resistance and inductance represent, respectively, the effective resistance and inductance of a single layer within a P/G network.

III. Multi-Layer Optimization

Multi-layer systems can be approximated by the network shown in Fig. 2, where the resistance and inductance is, respectively, the effective resistance and inductance of a single layer within a P/G distribution network [12]. This model treats the system as worse case since all of the current is assumed to flow through the entire layer. Electromigration should also be considered when optimizing a multi-layer system.

The current density CD of an arbitrary layer m is

$$CD_m = \frac{abs(i_m)}{CroSec_m}, \tag{6}$$

where i_m and $CroSec_m$ are the current and cross section of layer m, respectively. The skin effect is considered in determining the cross-section of the layer,

$$CroSec_m = \begin{cases} N_m w_m t_m & 2\delta > w \quad (7)\\ N_m w_m t_m & 2\delta > t \quad (8)\\ 2\delta\,[N_m(w_m+t_m)-2\delta] & \text{otherwise}, \quad (9)\end{cases}$$

where δ is the skin depth. The skin depth is defined as

$$\delta \equiv \sqrt{\frac{1}{\pi f \mu_0 \sigma}}, \tag{10}$$

where σ is the conductivity of the material.

The limiting current density is the highest current density among the layers. The current density among the layers is maintained equal, minimizing the limiting current density of a P/G network. A lower limiting current density enhances the reliability of a multi-layer system. Based on the current density, two layers, m and n, provide the same current density when

$$|Z_m|\,CroSec_m = |Z_n|\,CroSec_n, \tag{11}$$

where Z_m and Z_n are the impedance of layer m and n, respectively.

While the width of a single metal layer is optimized for minimum impedance, the width of the remaining metal layers

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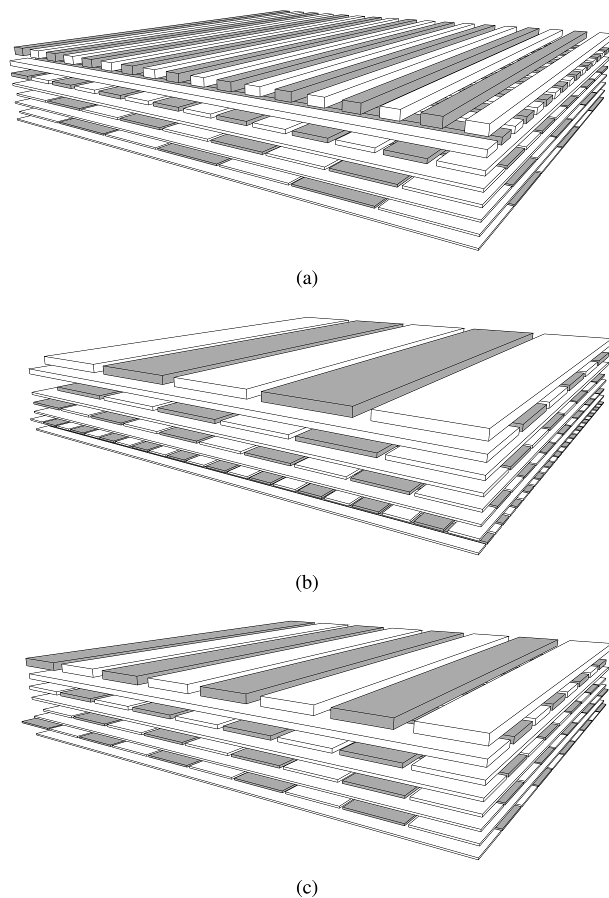

Fig. 3. Three P/G structures; (a) *pyramid* (proposed) structure - the width decreases with higher metal layers, (b) *inverted pyramid* (standard) structure - the width increases with higher metal layers, and (c) *equal width* structure - the width is maintained equal among all of the metal layers.

is chosen to maintain equal current density, as described by (11). Based on the proposed methodology, an eight layer P/G distribution network is described for a 65 nm CMOS technology. To evaluate the proposed methodology, all of the metal layers are assumed to be available for P/G distribution, although in practical cases some metal layers are used for the signals, clock network, and shield lines.

Based on a 65 nm CMOS technology [13], a width of 1.66 μm is initially determined from (4) for the top (eighth) metal layer to minimize the impedance of a single metal layer. The width of the additional metal layers is based on maintaining equal current density according to (11). Due to the increase in inductance and decrease in resistance in the higher metal layers, the lines should be wider in the lower metal layers. This structure is therefore called a *pyramid* structure.

Two additional P/G network structures are compared with the proposed *pyramid* structure. These three structures are illustrated in Fig. 3. The *pyramid* (proposed) structure is shown in Fig. 3(a). Note in the *pyramid* structure, the power and ground lines in the lower metal layers are wider. In conventional metal systems, the power and ground lines are wider in the higher metal layers, as illustrated in Fig. 3(b). For this structure, the width of the metal layers is the opposite of the *pyramid* structure, and is therefore called the *inverted*

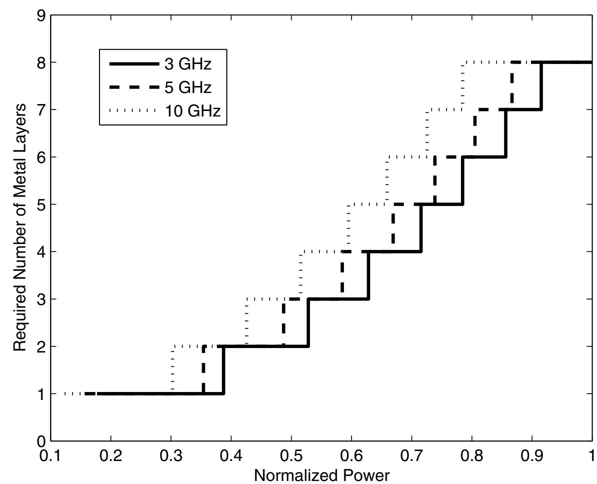

Fig. 4. Required number of metal layers for a P/G network as a function of normalized power evaluated at three different frequencies.

pyramid (standard) structure. In Fig. 3(c), the width of each metal layer is maintained constant at 5.5 μm; therefore, this structure is referred to as the *equal width* structure. The width, number of interdigitated pairs, effective impedance, and limiting current density for these three structures are listed in Table I. For the current density evaluation, the metal layers are extracted individually using FastHenry.

In the *pyramid* structure, the current density is maintained equal among all of the layers, lowering the limiting current density. Since the thickness decreases with lower metal layers, the lines are wider, maintaining a constant current density. In the *inverted pyramid* structure, the higher metal layers are wider, permitting greater routing flexibility. The reliability of the metal, however, decreases since the limiting current density is 82% higher as compared to the *pyramid* structure. In the *inverted pyramid* structure, most of the current flows in the higher metal layers increasing the effective impedance of the overall system. The impedance is 50% higher than in the *pyramid* structure. The *equal width* structure exhibits a higher effective impedance and current density of 24% and 36%, respectively, as compared to the *pyramid* structure. This trend is consistent with the change in importance of the inductance as compared to the resistance at higher frequencies.

IV. Discussion

The required number of metal layers for the specified power levels is depicted in Fig. 4. The technology parameters are chosen based on a 65 nm CMOS technology with an area of 1 mm x 1 mm. The results are evaluated at three different frequencies, indicating that an additional metal layer is required at higher frequencies.

The optimal width as a function of the number of metal layers at 3 GHz and 10 GHz is illustrated in Fig. 5 for a 65 nm, 45 nm [14], and 32 nm [15] CMOS technology. The optimal width is determined from application of the Newton-Raphson method, as described in (4). At higher frequencies, the optimal width is thinner since the inductive impedance is greater. The optimal width increases with thinner, less

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TABLE I

THREE STRUCTURES ARE COMPARED FOR EQUAL CURRENT DENSITY. THE THICKNESS, SPACING, WIDTH, AND NUMBER OF INTERDIGITATED PAIRS PER METAL LAYER FOR EACH STRUCTURE ARE LISTED.

Metal Layer	Thickness [μm]	Spacing [μm]	*Pyramid* structure		*Inverted pyramid* structure		*Equal width* structure	
			Width [μm]	Number of pairs	Width [μm]	Number of pairs	Width [μm]	Number of pairs
8	0.975	0.540	1.7	227	9.0	52	5.5	82
7	0.650	0.360	2.4	183	8.1	59	5.5	85
6	0.430	0.240	3.6	131	7.7	63	5.5	87
5	0.300	0.165	5.1	94	6.1	79	5.5	88
4	0.250	0.140	6.1	79	5.1	95	5.5	88
3	0.200	0.110	7.7	64	3.6	136	5.5	89
2	0.190	0.105	8.1	61	2.4	202	5.5	89
1	0.170	0.105	9.0	54	1.7	280	5.5	89
Effective Impedance [mΩ]			30.6		46.0		38.2	
Limiting Current Density [mA/μm^2]			0.766		1.400		1.044	

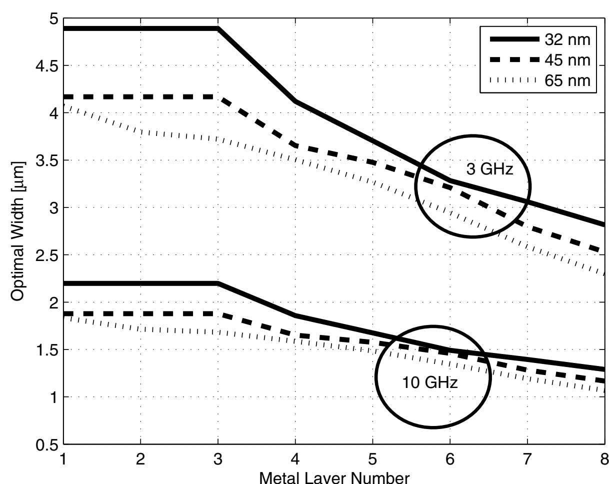

Fig. 5. Optimal width to minimize the effective impedance of each metal layer based on a 65 nm, 45 nm, and 32 nm CMOS technology for two different frequencies.

inductive metal layers to satisfy the minimum impedance constraint. With technology scaling, the metal thickness typically decreases, requiring wider lines to compensate for the increase in resistivity.

V. CONCLUSIONS

The impedance of a single layer within an interdigitated P/G network structure is minimized, permitting an efficient and accurate estimate of the optimal width of the power and ground wires. For 65 nm, 45 nm, and 32 nm CMOS technologies, the optimal width of each metal layer for minimum effective impedance is determined. The effect of the physical dimensions of the metal and the signal frequency on the optimal width is also discussed.

Considering the current density, a multi-layer interdigitated P/G distribution network is evaluated. *Pyramid* (proposed), *inverted pyramid* (standard), and *equal width* P/G structures are considered. The proposed methodology for equal current density improves the effective impedance and limiting current density by 50% and 82%, respectively, as compared with the *inverted pyramid* conventional structure. This behavior is due to the relative change in importance of the inductance as compared to the resistance in high frequency systems.

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