An Area Efficient Fully Monolithic Hybrid Voltage Regulator

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***Abstract*— A hybrid voltage regulator module for an on-chip DC-DC voltage converter is proposed in this paper. The circuit is appropriate for point-of-load voltage regulation due to an ultra area efficient architecture. The proposed voltage regulator is a hybrid combination of a switching DC-DC voltage converter and a low-dropout regulator exploiting active circuitry rather than bulky passive devices within the filter structure. The proposed circuit can supply over 100 mA current while generating 0.9 volts from a 1.2 input voltage, exhibiting a high current efficiency of greater than 99%. The on-chip area is 0.026 mm^2 which is 500 times smaller than a monolithic buck converter and four times smaller than an LDO. The proposed regulator provides a means for distributing multiple local power supplies across an integrated circuit while providing high current efficiency.**

I. Introduction

With the continuous scaling of technology, the design of on-chip power distribution networks has become a significant issue [1]–[3]. Noise sensitive circuit blocks requiring a clean supply voltage are distributed throughout an integrated circuit (IC). The power/ground (P/G) noise is increasing relative to the voltage supply. Delivering a clean and robust on-chip power supply voltage has therefore become increasingly difficult. Several techniques are used to supply a robust voltage to the noise sensitive blocks. One method is to use decoupling capacitors to reduce the impedance of the power distribution network over a wide frequency range [1], [2]. Since the active devices switch at high frequencies, the decoupling capacitors require sufficient time to recharge before the next switching event [4]. The efficacy of the decoupling capacitors depends upon the distance from the decoupling capacitor to the power supply. On-chip power supplies would therefore naturally improve on-chip P/G integrity [3]–[5]. On-chip voltage regulators provide charge not only to the load circuitry but also to the locally distributed decoupling capacitors, enhancing the efficiency of the overall system. Noise due to the package parasitic impedance is also eliminated by the monolithic implementation of the voltage regulator. An area efficient voltage regulator is required to realize a distributed system of on-chip voltage regulators.

Both off-chip and on-chip DC-DC voltage converters are generally used to supply power to modern ICs [3], [5]. Conventional DC-DC converters can be grouped into three categories. Switching, switched capacitor, and linear DC-DC converters [3]. A typical switching DC-DC converter (also known as a buck converter) is shown in Fig. 1. A pulse width modulator (PWM) generates a switching signal which drives tapered buffers which drives large NMOS and PMOS transistors (see Fig. 1). The PMOS and NMOS transistors generate a switching signal at Node$_1$. The passive inductor/capacitor (LC) filter removes the high frequency harmonics of this switching signal, generating a DC output voltage Vdd_2,

$$Vdd_2 = Vdd_1 \left(D - \frac{t_r - t_f}{2T} \right), \tag{1}$$

where D, t_r, t_f, and T are the duty cycle, rise time, fall time, and period of the switching voltage, respectively [3]. When the rise and fall times of the switching signal are the same, the output voltage is

$$Vdd_2 = DVdd_1. \tag{2}$$

The PWM detects any deterioration in the generated signal, tuning the output of the PWM to compensate for changes in Vdd_2. When the duty cycle of the switching signal increases, the output DC level also increases. The primary drawback of a buck converter, however, is that the passive LC components require large on-chip area, generally requiring these passive elements to be placed off-chip.

The most commonly used linear regulator is a low-dropout (LDO) regulator [6]–[8]. LDO regulators are more area efficient as compared to buck converters and generally can be on-chip. These regulators, however, require a large output capacitance to maintain stability [7]. This output capacitor is generally implemented off-chip. Some capacitorless techniques have been proposed for fully monolithic LDO regulators [6], [8]. These techniques, however, require additional circuitry, increasing the on-chip area of the regulator. LDO regulators provide fast load regulation as compared to buck converters.

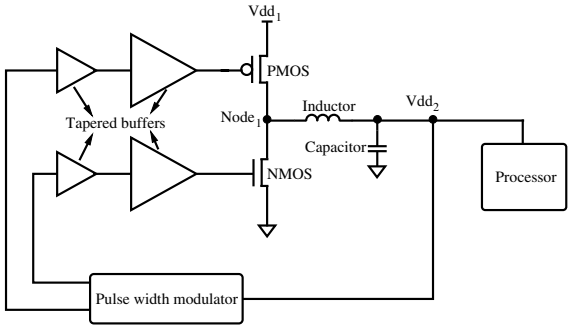

Fig. 1. Conventional buck converter circuit. The inductor and capacitor are typically implemented off-chip due to the large area requirement.

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The power efficiency, however, unlike a buck converter is limited to V_{out}/V_{in}.

Switched capacitor DC-DC converters utilize non-overlapping switches to charge the capacitors to transfer charge from the input to the output. These regulators dissipate a significant amount of power through the resistive switches. Furthermore, the feedback circuitry required to maintain a stable output voltage is difficult to implement [3].

A hybrid combination of a switching and linear voltage regulator is proposed in this paper. This circuit provides a means for distributing multiple power supplies across an integrated circuit with fast load regulation and small area. The passive LC filter in a buck converter is replaced with an active filter. The concept of replacing the passive filter with an active filter was first proposed in [9]. In this paper, emphasis is placed on evaluating speed, power, and area tradeoffs of several active filter topologies. Feedback paths within the proposed voltage regulator are also exploited for enhanced stability.

The rest of this paper is organized as follows. The proposed circuit with different active filter topologies and types are discussed in Section II. In Section III, simulation results for several output current demand characteristics are addressed. Finally, the paper is concluded in Section IV.

II. Active Filter-Based Switching DC-DC Converter

The passive LC filter in a conventional buck converter is replaced with an active filter structure and the tapered buffers are replaced with smaller buffers, as shown in Fig. 2. The current delivered to the load circuitry is supplied by an operational amplifier (op-amp). Small buffers are therefore sufficient to drive the active filter. Replacing the tapered buffers with smaller buffers significantly decreases the power dissipated by the input stage. Alternatively, the output buffers within the op-amp dissipate power within the proposed converter. Additionally, the feedback required for line and load regulation is satisfied with separate feedback paths, as shown in Fig. 2. Feedback$_1$ is generated by the active filter structure and provides load regulation whereas feedback$_2$ is optional and can be used to control the duty cycle of the switching signal for line regulation. In most cases, feedback$_1$ is sufficient to guarantee fast and accurate load regulation. When only one feedback path is used, the switching signal is generated by simpler circuitry (*e.g.*, a ring oscillator) and the duty cycle of the switching signal is compensated by a local feedback circuit (a duty cycle adjustor). The primary advantage of a single feedback path is smaller area since feedback$_1$ is provided within the active filter and no additional circuitry is required to implement the compensation structure.

Active filters have been well studied over the last half century [10], [11]. The objective of this section is to review those properties of active filters which affect the design of the proposed voltage regulator while providing relevant background material. Active filter configurations and topologies are briefly reviewed in Section II-A. The design of the op-amp is discussed in Section II-B,

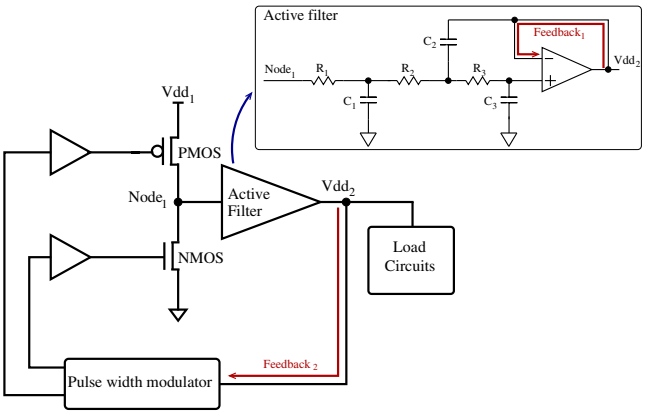

Fig. 2. Proposed DC-DC converter. The bulky LC filter is replaced with an active filter and the large tapered buffers are replaced with smaller buffers. Note that two different feedback paths exist which separate the line and load regulation.

A. Active Filter Design

Active filters have no passive inductors. Capacitors, resistors, and an operational amplifier, however, are utilized to implement the filtering function. Certain design considerations are considered when utilizing an active filter as a voltage regulator since the appropriate active filter topology depends upon the application [11]. For a voltage regulator, the on-chip area, sensitivity of the active filter to component parameter variations (due to aging, temperature, and process variations), and the power dissipated by the active components should be low. Two topologies are popular for implementing an integrated low pass active filter, multiple feedback and Sallen-Key [10]. Multiple feedback low pass filters use capacitive and resistive components within the feedback path from the output to the input. A DC current path therefore exists between the input and output nodes due to this resistive feedback, dissipating power. Multiple feedback active filters are therefore less suitable for an on-chip voltage converter due to the high power dissipated by the resistive feedback. Alternatively, Sallen-Key low pass filters only use capacitive feedback. Hence, the static power dissipation of the Sallen-Key topology is significantly lower than the multiple feedback topology.

A third order low pass unity-gain Sallen-Key filter topology is shown in the top right part of Fig. 2. The first section, R_1 and C_1, forms a first order low pass RC filter. R_2, R_3, C_2, C_3, and the op-amp form a second order Sallen-Key low pass filter. No DC current path exists between the input and output. The transfer function of the active filter, shown in Fig. 2, is

$$\frac{V_{out}}{V_{in}} = \frac{1}{a_1 s^3 + a_2 s^2 + a_3 s + a_4}, \tag{3}$$

where

$$a_1 = R_1 R_2 R_3 C_1 C_2 C_3, \tag{4}$$

$$a_2 = R_1 C_1 C_3 (R_2 + R_3) + R_3 C_2 C_3 (R_1 + R_2), \tag{5}$$

$$a_3 = R_1 C_1 + C_3 (R_1 + R_2 + R_3), \tag{6}$$

$$a_4 = 1. \tag{7}$$

TABLE I

SENSITIVITY ANALYSIS FOR A THIRD ORDER SALLEN-KEY FILTER. PER CENT CHANGE IN CUTOFF FREQUENCY AND Q FACTOR WHEN INDIVIDUAL PARAMETER VALUES ARE INCREASED BY 1%.

	R1	R2	R3	C1	C2	C3
Q	0	-0.4	0.4	0	-0.5	0.5
Cut-off frequency	-1	-0.5	-0.5	-1	-0.5	-0.5

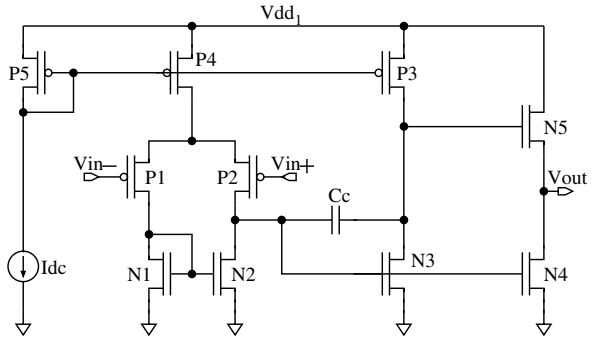

Fig. 3. Three stage op-amp. The PMOS input transistors are used in the first differential input stage. The second stage is a common-source gain stage and the third stage includes the output buffer which supplies current to the load.

A Chebyshev filter type is chosen due to the steep roll-off factor as compared to those filter structures which do not require resistive components connected to ground to implement finite zeros. Larger passive components are required to implement the filter when the cutoff frequency is shifted to a lower frequency. Since a Chebyshev filter exhibits a steeper slope, the component values are smaller than other filter types while providing the same stop-band frequency response. A third order Chebyshev type I low pass Sallen-Key filter is therefore an appropriate filter topology for the proposed application.

The parameters, a_1, a_2, and a_3, are selected from Chebyshev filter tables [11]. The per cent change in the cutoff frequency and the Q factor of the third order Sallen-Key filter shown in Fig. 2 are listed in Table I with the parameter values individually increased by 1%.

B. Op-amp Design

The performance of an active filter depends upon the performance of the op-amp. The gain-bandwidth (GB) product of the op-amp determines the bandwidth of the active filter. Most of the power loss is within the op-amp structure. The current supplied to the output load is from the op-amp output stage. Hence, the op-amp provides hundreds of milliamps to the load. A three stage differential-input single-ended CMOS op-amp structure, shown in Fig. 3 [12], is used. The overall three stage gain is 50 dB with a phase margin of 51°.

The primary element of an op-amp operating within a power supply is the output stage which supplies current to the load circuitry. The width of the transistors, N_4 and N_5, in the output source follower stage can be increased when a higher output voltage or current is required. N_5 acts as a current source supplying current to the output node while also regulating the current depending upon the transient current requirements of the load circuitry.

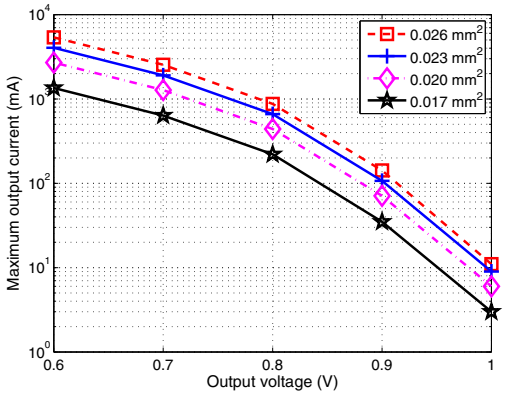

Fig. 4. Maximum current delivered to the load circuitry for different output voltages. The maximum current for a particular output voltage can be increased by adding more parallel output stages within the op-amp.

III. SIMULATION RESULTS

The proposed active filter-based DC-DC voltage converter has been designed in a 90 nm CMOS technology. The input switching signal frequency is 100 MHz. A modified ring oscillator[1] supplies the switching signal to the input. Since there is no need for large tapered buffers, the power dissipated by the ring oscillator and output buffers is relatively small. The on-chip area of the proposed regulator depends upon the target output voltage and load current characteristics, as illustrated in Fig. 4. The total on-chip area is approximately 0.026 mm^2 which is $\sim$ 500 times smaller than a conventional on-chip switching DC-DC converter with passive filter components (12.6 mm^2) [5]. The area is also approximately four times smaller than a recently proposed fully monolithic LDO [6], as listed in Table III. Unlike other linear regulators, no capacitor is connected at the output node, making the proposed circuit convenient for point-of-load voltage regulation.

The circuit generates 0.9 volts from a 1.2 volt input voltage. The duty cycle of the input switching signal is 75%. The transient response of the output voltage to changes in the output current demand is shown in Fig. 5. The simulation results are summarized in Table II. An advantage of the proposed circuit is that the output voltage settles at the desired voltage level regardless of the output current demand. That is, the current demand from the load circuitry does not produce a significant DC voltage shift in the output voltage. Additionally, the amplitude of the voltage spikes at the output is less than 9% of the output voltage despite abrupt changes in the output current demand (*e.g.*, 10 A/μs slope).

The proposed regulator dissipates 0.38 mA quiescent current and can deliver over 140 mA current to the load circuitry. The current efficiency is greater with increasing current demand. When the output current demand is more than 40 mA, the current efficiency exceeds 99%. A limitation on the maximum output voltage exists due to the NMOS transistors within the output stage of the op-amp. When the output voltage is

[1]Ring oscillator with an adjustable duty cycle.

TABLE II

SIMULATION RESULTS OF THE PROPOSED VOLTAGE REGULATOR

Output current transition slope		Fall transition	Rise transition
1 A/μs	Response time (ns)[a]	57	55
	Amplitude of voltage spike (mV)	21	-14
	% of voltage spike	2.33%	1.56%
10 A/μs	Response time (ns)	47	20
	Amplitude of voltage spike (mV)	66	-73
	% of voltage spike	7.33%	8.11%

[a]Response times are recorded when the amplitude of the voltage spikes is less than 1% of the generated voltage.

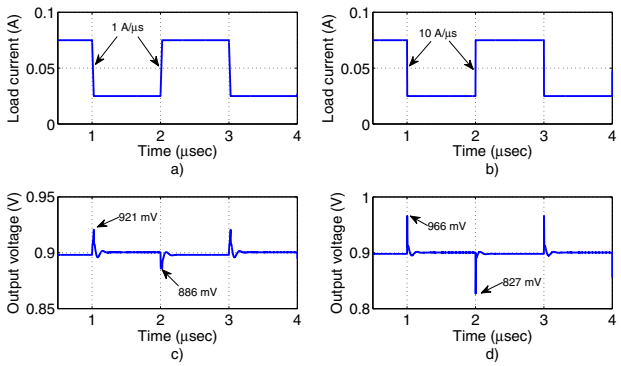

Fig. 5. Load regulation of the proposed circuit. The output voltage is plotted for different transient current demand characteristics. The output current ranges between 25 mA and 75 mA with rise and fall transition slopes of (a) 1 A/μs and (b) 10 A/μs. The output voltage waveforms for a generated voltage of 0.9 volts are shown in (c) for 1 A/μs and (d) for 10 A/μs transition slopes. Note that a faster transition in the output current induces a larger voltage spike at the output.

TABLE III

PERFORMANCE OF THE PROPOSED CONVERTER CIRCUIT

	[5]	[6]	[7]	This work
Year	2003	2005	2007	2009
Technology (nm)	80	90	350	90
V_{in} (V)	1.2	1.2	2.0 - 5.5	1.2
V_{out} (V)	0.9	0.9	1.8 - 3.15	0.9
I_Q (mA)	N/A	6	0.02	0.38
I_{max} (mA)	9500	100	200	140
Current efficiency (%)	N/A	94.3	99.8	99.5
Response time (ns)	87	0.54	270	57
On-chip area (mm^2)	12.6	0.098	0.264	0.026
Output DC shift (mV)	100	90	54	9

larger, the effective voltage across N_5 is smaller, limiting the maximum current that N_5 can supply to the load circuitry.

A performance comparison of the proposed circuit with other switching and LDO regulators is listed in Table III, where [5] is an on-chip buck converter and [6] and [7] are LDO regulators. Note that the on-chip area required by the proposed circuit is significantly less than all of these regulator circuits. Furthermore, the DC shift in the generated voltage is around 1% of the output voltage, which is significantly smaller than the other example regulator circuits.

IV. CONCLUSIONS

A hybrid combination of a switching and linear voltage regulator appropriate for distributed point-of-load voltage regulation is proposed in this paper. The bulky passive LC filter within a buck converter is replaced with an active filter structure to minimize on-chip area while realizing distributed point-of-load voltage regulation. Design requirements and tradeoffs of both an active filter and the op-amp are reviewed. The area required for the proposed active filter power supply is approximately 500 times smaller than a conventional switching DC-DC converter [5] and about four to six times smaller than a low area LDO regulator [6]. The amplitude of the voltage spikes at the output is less than 2.5% of the target output voltage when the output current transitions with a slope of 1 A/μs. When the output current transitions at 10 A/μs, the amplitude of the voltage spikes is less than 9% of the desired output voltage. The current efficiency is over 99% when the output current demand is greater than 40 mA. The need for an off-chip capacitor or advanced circuit techniques to maintain stability and performance is eliminated in the proposed circuit. This converter circuit provides a means for distributing multiple power supplies across an IC, providing high current efficiency within a small area.

REFERENCES

[1] L. Smith *et al.*, "Power Distribution System Design Methodology and Capacitor Selection for Modern CMOS Technology," *IEEE Transactions on Advanced Packaging*, Vol. 22, No. 3, pp. 284–291, August 1999.

[2] M. Popovich, A. V. Mezhiba, and E. G. Friedman, *Power Distribution Networks with On-Chip Decoupling Capacitors*, Springer, 2008.

[3] V. Kursun and E. G. Friedman, *Multi-Voltage CMOS Circuit Design*, New York: Wiley, 2006.

[4] M. Popovich, M. Sotman, A. Kolodny, and E. G. Friedman, "Effective Radii of On-Chip Decoupling Capacitors," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 16, No. 7, pp. 894-907, July 2008.

[5] V. Kursun, S. G. Narendra, V. K. De, and E. G. Friedman, "Analysis of Buck Converters for On-Chip Integration with a Dual Supply Voltage Microprocessor," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 11, No. 3, pp. 514–522, June 2003.

[6] P. Hazucha *et al.*, "Area-Efficient Linear Regulator with Ultra-Fast Load Regulation," *IEEE Journal of Solid-State Circuits*, Vol. 40, No. 4, pp. 933–940, April 2005.

[7] M. Al-Shyoukh, H. Lee, and R. Perez, "A Transient-Enhanced Low-Quiescent Current Low-Dropout Regulator with Buffer Impedance Attenuation," *IEEE Journal of Solid-State Circuits*, Vol. 42, No. 8, pp. 1732–1742, August 2007.

[8] K. N. Leung and P. K. T. Mok, "A Capacitor-Free CMOS Low-Dropout Regulator with Damping-Factor-Control Frequency Compensation," *IEEE Journal of Solid-State Circuits*, Vol. 38, No. 10, pp. 1691–1702, October 2003.

[9] C. H. Wu, L. R. Chang-Chien, and L. Y. Chiou, "Active Filter Based On-Chip Step-Down DC-DC Switching Voltage Regulator," *Proceedings of the IEEE International TENCON Conference*, pp. 1–6, November 2005.

[10] P. R. Sallen and E. L. Key, "A Practical Method for Designing RC Active Filters," *IRE Transactions of Circuit Theory*, Vol. CT-2, pp. 74–85, March 1955.

[11] G. Daryanani, *Principles of Active Network Synthesis and Design*, Wiley, 1976.

[12] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, Wiley, 1997.