Digitally Controlled Wide Range Pulse Width Modulator for On-Chip Power Supplies

Selçuk Köse
Department of Electrical Engineering
University of South Florida
Tampa, Florida 33620
kose@usf.edu

Inna Vaisband and Eby G. Friedman
Department of Electrical and Computer Engineering
University of Rochester
Rochester, New York 14627
{vaisband, friedman}@ece.rochester.edu

***Abstract*— A digitally controlled current starved pulse width modulator is described in this paper. The current from the power grid to the ring oscillator is controlled by a header circuit. By changing the header current, the pulse width of the switching signal generated at the output of the ring oscillator is dynamically controlled, permitting the duty cycle to vary between 50% and 90%. A duty cycle to voltage converter is used to ensure the accuracy of the system under process, voltage, and temperature (PVT) variations. The accuracy and performance of the proposed digitally controlled pulse width modulator is evaluated with 22 nm CMOS predictive technology models under PVT variations. The proposed pulse width modulator is appropriate for dynamic voltage scaling systems due to the small on-chip area and high accuracy under process, voltage, and temperature variations. Although the frequency of the switching signal is affected by changes in the duty cycle, the frequency variations are typically negligible.**

I. Introduction

Voltage controlled oscillators (VCOs) are widely used to generate a switching signal where certain characteristics of this signal can also be controlled. Two types of VCOs are primarily used in high performance integrated circuits (ICs); inductor-capacitor (LC) oscillators and ring oscillators. LC oscillators can operate at high frequencies and exhibit superior noise performance. Alternatively, ring oscillators occupy significantly smaller on-chip area with a wider tuning range. Due to these advantages, ring oscillators have found widespread use in modern ICs [1]–[3].

A conventional ring oscillator consists of an odd number of inverters where the output of the last inverter is fed back to the input of the first inverter, as shown in Fig. 1. The delay provided by each inverter in this chain produces a phase shift in the switching signal. The sum of these individual delays (*i.e.*, phase shifts) and the feedback from the last to the first inverter produce a total phase shift 2π that causes the circuit to oscillate. The frequency of this oscillation depends upon the sum of the inverter delays within the chain [4].

The duty cycle of the generated switching signal is typically 50% for conventional ring oscillators where the PMOS and NMOS transistors within the inverters provide the same rise and fall transition times. The duty cycle of a ring oscillator can be changed by controlling the transition time of the inverters within the ring oscillator. Header and footer circuits are widely used to control the current supplied to the PMOS and NMOS transistors within the ring oscillator inverter chain. Although the header and footer circuits are typically used to control the frequency, these circuits can also control the duty cycle of a ring oscillator.

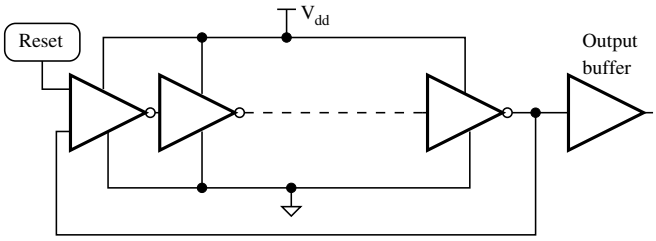

Fig. 1. Conventional ring oscillator. Note that an odd number of inverters is in the chain to permit the system to oscillate.

In this paper, a digitally controlled pulse width modulator (PWM) which comprises a header circuit, a ring oscillator, and a duty cycle to voltage (DC2V) converter is described. The header circuit controls the amount of current delivered to the PMOS transistors within the ring oscillator. Since the target specification is to vary the duty cycle between 50% and 90%, no footer circuitry is used to control the current of the NMOS transistors. Contrary to conventional header circuits, where the header is connected to all of the inverters within the ring oscillator chain, the proposed header circuit is connected to every other inverter stage to dynamically control the pulse width of the output signal. This header circuit provides high granularity duty cycle control with a step size of 2% of the period. Additionally, a DC2V converter, based on the frequency to voltage converter proposed in [5], maintains the accuracy of the PWM under process, voltage, and temperature (PVT) variations. Under PVT variations, the maximum change in the duty cycle is less than 1.5% of the period.

Owing to the small on-chip area, fast control circuitry, high accuracy under PVT variations, and dynamic duty cycle control, the proposed PWM is an effective circuit to dynamically change the duty cycle of the input switching signal for on-chip voltage regulators. This circuit enables high granularity dynamic voltage scaling (DVS) at runtime and reduces the response time from milliseconds to nanoseconds.

The rest of the paper is organized as follows. The proposed

This research is supported in part by the New York State Office of Science, Technology and Academic Research to the Center for Advanced Technology in Electronic Imaging Systems, and by grants from Qualcomm, Cisco Systems, and Samsung.

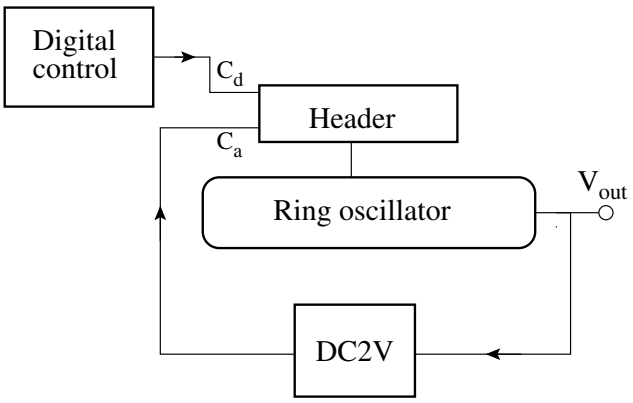

Fig. 2. The proposed pulse width modulator. The header circuitry has two input control signals, digital control (C_d) and analog control (C_a). C_d is used to dynamically change the individual transistors to provide high granularity duty cycle control whereas C_a maintains a constant current from the header to the ring oscillator under PVT variations.

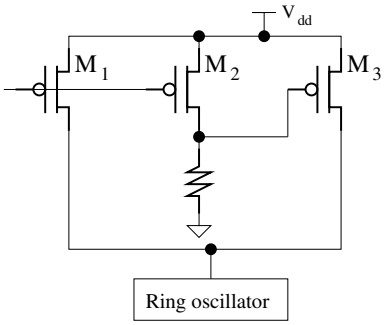

Fig. 3. An addition based current source used as a header circuit [7].

PWM architecture is described in Section II, where the working principle of the header circuitry and DC2V converter is explained. In Section III, the functionality and accuracy of the proposed circuit under PVT variations are validated with predictive technology models at the 22 nm technology node. Some concluding remarks are offered in Section IV.

II. Description of the Proposed PWM Architecture

A schematic of the proposed PWM is shown in Fig. 2. A header circuit is connected to the ring oscillator to current starve every other stage in the ring oscillator chain. A digital controller provides multiple digital control signals (C_d) to dynamically change the duty cycle, and a DC2V converter ensures the accuracy of the duty cycle by providing an analog signal to the header circuit under PVT variations. The working principles of these circuits are explained in the following subsections.

A. Header Circuitry

An addition based current source, as shown Fig. 3, was proposed in [6]. This circuit is used as a header in [7] to compansate for temperate and process variations by maintaining a constant total current. Note that this header circuit has one input voltage that controls the gate voltage of M_1 and M_2. By controlling this gate voltage, the sum of the current is maintained constant over a wide range of temperature and process variations [7].

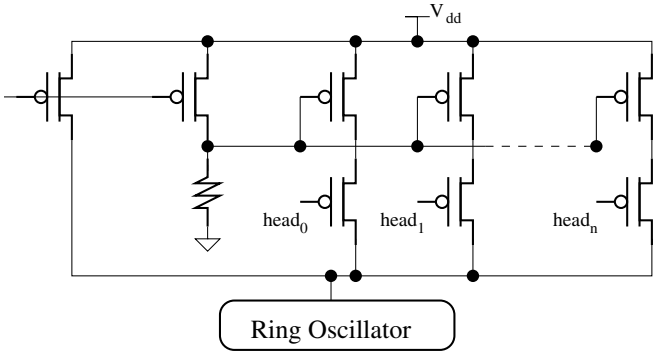

Fig. 4. Parallel PMOS transistors replace M_3 to improve the granularity of the current control as well as switch transistors to turn on and off different sections of the header circuitry.

Alternatively, in this paper, a modified version of this header circuit, as depicted in Fig. 4, is introduced to control the duty cycle of the ring oscillator output by changing the transition time of the PMOS transistors at every other inverter stage within the ring oscillator. As opposed to a single transistor M_3 whose gate is connected to the resistor, multiple parallel PMOS transistors are added in place of M_3 in the proposed header circuit. All of these transistors have the same gate-to-source voltage, but the voltage at the drain terminals is controlled by other switch transistors. Additional PMOS transistors are connected in series with these transistors as switch transistors. The gate voltage of these switch transistors is controlled by a digital controller to turn on and off the individual header stages. Turning on all of the header stages passes the maximum current to the ring oscillator which minimizes the duty cycle. The first two transistors in the header circuits are comparably large to minimize any mismatches. A minimum channel length of 150 nm is used for these two input transistors as opposed to 40 nm for the other transistors.

B. Duty Cycle to Voltage Converter

The frequency to voltage converter proposed in [5] is used as a DC2V converter. A circuit schematic of this DC2V converter is shown in Fig. 5. There are primarily three different phases of this circuit. During the first phase, capacitor C_1 is charged through transistor P_1. In the second phase, transistors (*i.e.*, switches) N_2 and N_3 are turned on to allow charge sharing between C_1 and C_2. At the last phase, C_1 is discharged through N_1. The charge time of C_1 depends upon the duty cycle of the input switching signal. A signal with a greater duty cycle causes more charge to accumulate on C_1, increasing the output voltage of this DC2V converter. A more complete explanation of the working principles of this circuit as well as the logic controller block is available in [5].

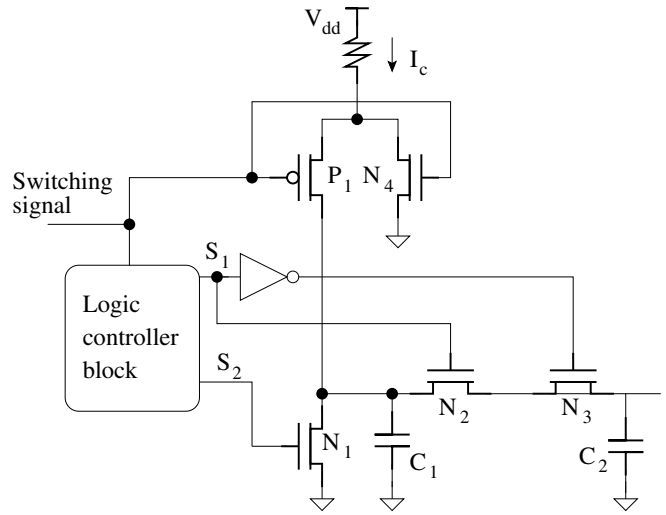

Fig. 5. The frequency to voltage converter proposed in [5] used as a duty cycle to voltage converter.

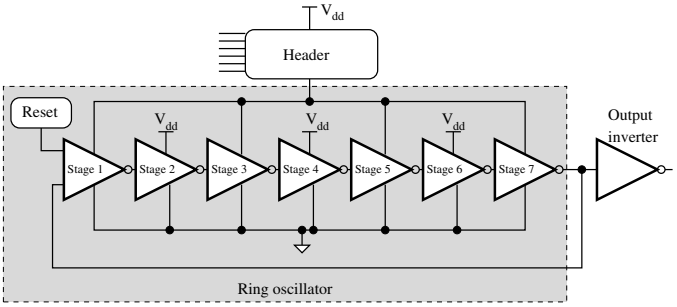

Fig. 6. Proposed ring oscillator where the header circuit is connected to every other stage to improve the dynamic range of the duty cycle.

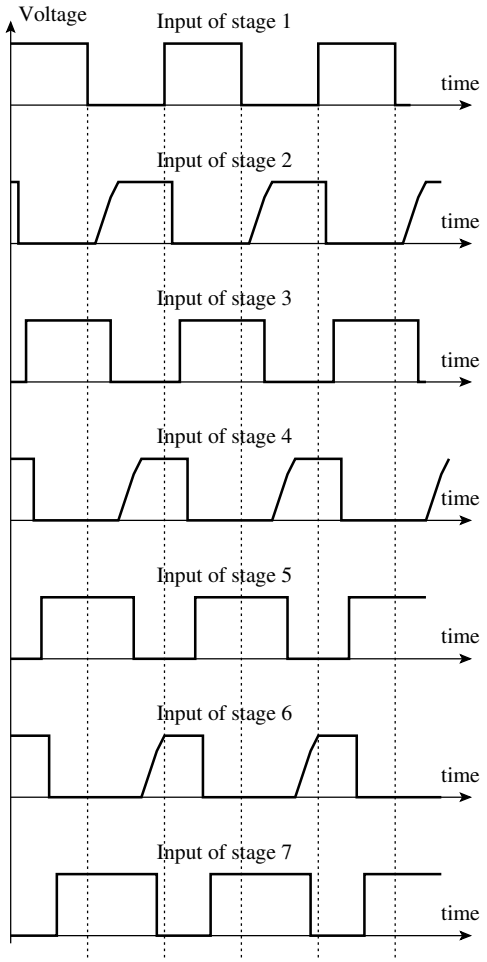

Fig. 7. Timing diagram of the proposed ring oscillator. Note that each stage connected to the header changes the transition time, and each stage directly connected to the supply voltage regulates the transition time.

C. Proposed Ring Oscillator Topology

A conventional ring oscillator with balanced rise and fall transition times and without a header exhibits a 50% duty cycle. Driving all of the stages by the same header current affects the rise and fall times equally, maintaining a 50% duty cycle. The inverters at every other stage generate the same logic function with a phase shift. A seven stage ring oscillator is used in this proposed circuit. The inverters in the first, third, fifth, and seventh stages are connected to the header circuit and the remaining inverters are connected directly to V_{dd}, as shown in Fig. 6. The header circuit connected to every other stage in the proposed ring oscillator increases the charge time at the output of these stages. The rise time at the output of the corresponding stage becomes greater with a longer charge time, as depicted in Fig. 7, for the proposed circuit. Additionally, the signals generated at the output of the inverters, which are not connected to the header circuit, have faster transition times due to the higher current delivered to the PMOS transistors within these inverters.

III. Simulation Results

The proposed circuit is designed in a 22 nm CMOS predictive technology model (PTM) [8]. Some of the related parameters in the technology model file are modified based on [9] to include process corners such as typical-typical (TT), slow-slow (SS), and fast-fast (FF).

The effect of the current, which is provided by the header circuit to the ring oscillator, on the duty cycle of the ring oscillator output is analyzed by replacing the header circuit with an ideal current source. A simplified schematic of this circuit is shown in Fig. 8. When the header current changes from 2 μA to 50 μA, the duty cycle of the switching signal at the output of the ring oscillator changes from 93% to 25%. Although the relationship between the header current and the duty cycle is not linear, as shown in Fig. 9, this relationship can be controlled by the digital control block.

The accuracy of the proposed PWM has also been analyzed for different duty cycle ratios under PVT variations. The per cent deviation of the different duty cycle ratios is listed in Table I, where the supply voltage varies $\pm$5% from the nominal 0.95 volts and the temperature varies from 27° C to 80° C. The simulations have been performed for TT, SS, and FF process corners. The deviation of the duty cycle under PVT variations is less than 1.5% of the total period of the

TABLE I

CHANGE IN THE DUTY CYCLE OF THE PROPOSED PWM UNDER PVT VARIATIONS FOR 22 NM PREDICTIVE CMOS MODELS [8] WHERE TYPICAL, FAST, AND SLOW CORNERS ARE, RESPECTIVELY, ABBREVIATED AS T, F, AND S. NOTE THAT THESE CORNERS HAVE BEEN GENERATED BY MODIFYING THE RELATED PARAMETERS IN THE MODEL FILES [9].

Vdd	Process	Temperature	Duty cycle (50%)	Duty cycle (60%)	Duty cycle (70%)	Duty cycle (80%)	Duty cycle (90%)
1	TT	27	50	60	70	80.1	90.82
1	TT	80	50	60.1	70.1	80.2	90.78
1	FF	27	49.9	60	70.2	80.4	91.63
1	FF	80	49.9	60.1	70.3	80.1	90.43
1	SS	27	50.2	60.3	70.2	80.3	90.2
1	SS	80	50.2	60.2	70.1	80.1	90.1
0.9	TT	27	50	60.2	70.3	80.4	91.3
0.9	TT	80	50	60.1	70.3	80.5	91.4
0.9	FF	27	49.8	60	70.4	80.7	91.5
0.9	FF	80	49.8	60	70.6	81	91.4
0.9	SS	27	50.3	60.5	70.6	80.7	90.5
0.9	SS	80	50.2	60.3	70.4	80.5	90.5

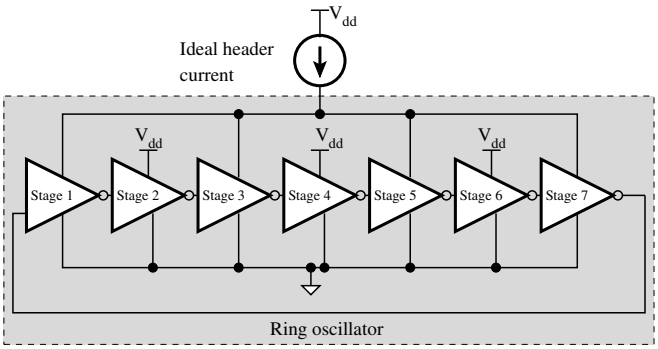

Fig. 8. An ideal current source replaces the header circuit to investigate the effects of the header current on the duty cycle.

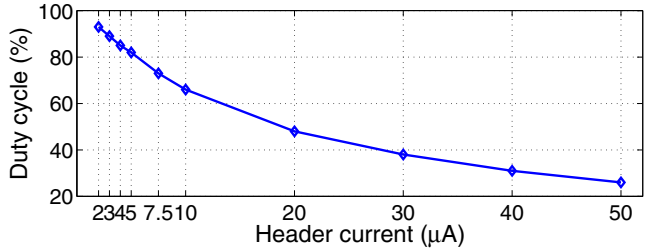

Fig. 9. The duty cycle varies between 25% to 93% when the header current changes from 50 μA to 2 μA.

switching signal. The transistors with a narrower gate width are more sensitive to PVT variations than the wider transistors. The narrower transistors within the header circuitry turn on if a switching signal with a greater duty cycle is required. The effect of PVT variations is therefore more prominent on those signals with a wider duty cycle. This trend can be observed in Table I, where the deviation for signals with a 50% duty cycle is smaller than for those signals with a 90% duty cycle.

IV. CONCLUSIONS

A digitally controlled PWM with a wide pulse width range of 50% to 90% is proposed in this paper. A header circuit based on a previously published addition based current source is proposed to provide a greater range of header current. The proposed header circuit is connected to every other stage of the ring oscillator to significantly improve the dynamic range of the pulse width of the output signal. A DC2V converter samples the duty cycle of the output signal and generates an analog voltage to control the header current. The PVT variations are compensated by the feedback loop generated by this DC2V converter. Under PVT variations, deviations in the pulse width are less than 1.5% of the switching signal period. The proposed pulse width modulator provides a means for dynamically changing the voltage in adaptive systems using fast control circuitry, which provides high accuracy under PVT variations and dynamic duty cycle control.

REFERENCES

[1] B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill, 2001.

[2] B.H. Calhoun and A. Chandrakasan, "Ultra-Dynamic Voltage Scaling Using Sub-Threshold Operation and Local Voltage Dithering in 90nm CMOS," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 300–599, February 2005.

[3] T.D. Burd, T.A. Pering, A.J. Stratakos, and R.W. Brodersen, "A Dynamic Voltage Scaled Microprocessor System," *IEEE Journal of Solid-State Circuits*, Vol. 35, No. 11, pp. 1571–1580, 2000.

[4] S. Docking and M. Sachdev, "A Method to Derive an Equation for the Oscillation Frequency of a Ring Oscillator," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 50, No. 2, pp. 259–264, February 2003.

[5] A. Djemouai, M. Sawan, and M. Slamani, "High Performance Integrated CMOS Frequency to Voltage Converter," *Proceedings of the International Conference on Microelectronics*, pp. 63–66, December 1998.

[6] A. M. Pappu, X. Zhang, A. V. Harrison, and A. B. Apsel, "Process-Invariant Current Source Design: Methodology and Examples," *IEEE Journal of Solid-State Circuits*, Vol. 42, No. 10, pp. 2293–2302, October 2007.

[7] X. Zhang and A. B. Apsel, "A Low-Power, Process and Temperature Compensated Ring Oscillator with Addition Based Current Source," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 58, No. 5, pp. 868–878, May 2011.

[8] NIMO Group, "Predictive Technology Model (PTM)," [Online]. Available from: http://www.eas.asu.edu/~ptm, Arizona State University.

[9] Y. Cao, *Predictive Technology Model for Robust Nanoelectronic Design*, Springer, 2011.