Field Driven STT-MRAM Cell for Reduced Switching Latency and Energy

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***Abstract*—A field driven approach to STT-MRAM switching is proposed as a method for reducing the switching latency of an MTJ in high performance caches. An MRAM array model is presented to characterize the switching energy and maximum achievable reduction in energy using the field driven approach. The switching latency per bit is reduced by more than a factor of ten. The resultant switching energy per bit is reduced by 82% as compared to a standard STT-MRAM.**

I. Introduction

Spin torque transfer magnetoresistive RAM (STT-MRAM) is an emerging CMOS compatible memory technology with the potential to replace on-chip memory. Key features of STT-MRAM are non-volatility and unlimited write endurance. An issue constraining the use of STT-MRAM, however, is the long switching latency of the magnetic tunnel junction (MTJ) within each memory cell. The long latency causes the switching energy of an MTJ to be much greater than traditional CMOS SRAM.

To address these issues, the classic first generation MRAM field topology is utilized with an STT-MTJ where an additional field current destabilizes the MTJ prior to switching, thereby reducing the switching latency. An analytic framework for assessing and optimizing field driven writes in STT-MRAM arrays is described in this paper. Building on this framework, it is shown that the switching latency and energy can be reduced by amortizing the additional field current over many cells, leading to a significant reduction in energy consumed per bit.

Background on STT-MRAM and classical MRAM is provided in Section II. The field driven approach is compared with classical MRAM approaches in Section III, while a model of a memory cell is presented in Section IV. A model of an MRAM array is reviewed in Section V. Some conclusions are offered in Section VI.

II. MTJ operation

Magnetic tunnel junctions are two terminal resistive elements that operate on the principle of spin dependant conduction through magnetic domains [1]–[3]. The device is a stack of ferromagnetic metal on both sides of a tunneling oxide spacer. One of these layers has a fixed magnetization direction. The alternate ferromagnetic layer can flip between two opposite polarities, one polarity parallel to the fixed layer and the other polarity anti-parallel. These two states influence the electrons that pass through the oxide barrier, changing the resistance. From a circuit perspective, an MTJ acts as a bistable resistor. After switching is triggered, the resistance either settles to a high (R_{off}) or low (R_{on}) resistance and will remain at that resistance until another switching event.

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In first generation MRAM circuits, the two large orthogonal currents generate magnetic fields within the free layer between adjacent metal lines. These fields are sufficiently strong to induce a torque on the magnetization, which eventually induces a reversal in polarity.

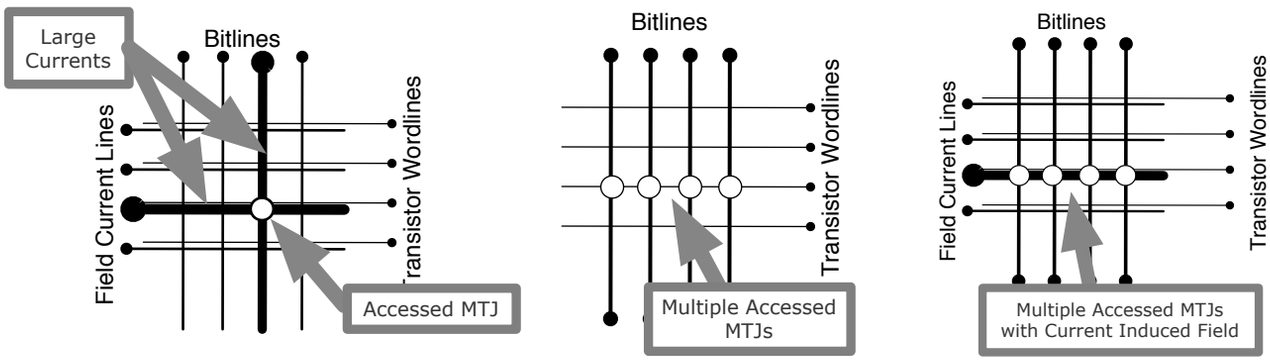
In modern spin torque transfer MTJs, the internal ferromagnetic layers generate a torque on the magnetization. The larger fixed ferromagnetic layer is capable of spin polarizing the incoming current, *i.e*, electrons from the incoming current attain spin. Electrons that pass through the fixed layer exhibit a net spin oriented with the fixed layer, while those electrons that reflect off the fixed layer exhibit a net anti-parallel spin. By controlling the direction of the current applied across the MTJ, either the reflected or passed electrons will contact the free layer and exert a torque on the magnetization.

III. Field driven STT-MRAM Cell

Since the spin transfer torque effect was first incorporated into MTJ switching [1], MRAMs have exclusively used this effect for writing. The STT effect, however, can complement the field driven excitation of the magnetic free layer within an MTJ. Classical MRAM approaches use two perpendicular currents with a single selected MTJ at the intersection to create a magnetic field that acts on the free layer of an MTJ (see Fig. 1(a)). This approach suffers from several problems: (1) the use of two currents to switch a single bit consumes a large amount of energy as compared to DRAM, (2) the MTJs in adjacent columns and rows are half-selected by the high fields caused by the write currents, potentially inducing erroneous writes, and (3) a checker read operation [4] is required to ensure that the correct state is written into the device. These issues have limited the scalability of classical MRAM devices.

The STT effect overcomes these problems by using a single current that passes through the MTJ. This technique enables many MTJs to be written in parallel, as illustrated in Fig. 1(b). Moreover, the direction of the applied current corresponds to the final state of the MTJ, *i.e.*, a forward bias exclusively sets the device to "1," whereas a reverse current exclusively sets the device to "0." The switching current is much lower than in classical MRAM, eliminating the half select problem. The write latency, however, remains significantly longer than the read latency, and the switching energy is also significantly greater than DRAM. Supplying a sufficiently large write current requires a large access transistor, which reduces the density of the circuit.

The approach proposed herein combines an STT-based current with a field-generating current used in classical MRAM circuits. In this approach, the field current produces an additional magnetic field that destabilizes the MTJs across a row. Each MTJ is biased with an STT current that controls the switching direction of the MTJs in each column. Use of a field current in this manner has two beneficial effects: (1) the



(a) (b) (c)

Fig. 1. Current biasing scheme for a) classical MRAM, b) standard STT-MRAM, and c) the proposed STT-MRAM

alignment of the field with respect to the MTJ can destabilize the device, which reduces both the write latency and energy, and (2) the field current is shared across the row, ensuring that the energy consumption of the field current is amortized across all of the cells within a row. This technique ensures that the energy consumption per bit is less than standard STT-MRAM.

A proof of concept for field-assisted switching was first demonstrated in [5] specifically for high-density, off-chip main memories. Andre *et al.* presented a similar structure that utilizes a field current to set the MTJ device to an initial reset state (either R_{on} or R_{off}) prior to writing the device. This method enables the uni-directional cells and the use of diodes to select the individual memory cells [6]. The approach presented here requires CMOS transistors for bipolar switching, and utilizes magnetic fields to enhance the dynamic behavior of the switching process to reduce the energy of a write, while sharing the field current to amortize the energy across multiple rows. The device is not reset to a stable state but rather an additional torque is applied dynamically to enhance the switching process. The approach presented here explores the design and memory sizing aspects associated with utilizing a field assisted approach and a relevant context for using these methods.

IV. Model of MRAM memory cell

The MTJ element is modeled using the classical Landau-Lifshitz-Gilbert single domain model and the simulation tool M^3 [7]. The MTJ free layer parameters are selected to ensure that the thermal stability factor (Δ) provides ten year retention of the device state ($\Delta = 40$). The MTJ parameters for resistance and TMR (from ITRS [8]) are listed in Table I. The critical switching current of the MTJ is dependent on the geometric and material properties of the free layer, permitting the current to be determined from the free layer geometry. The resultant critical current agrees with the switching current targeted by the ITRS.

The predictive technology model (PTM) is used to characterize the cell access transistor [9]. A low threshold transistor is used for the selection device and is modeled with a 20% reduction in threshold voltage. The word line is bootstrapped to $V_{DD} + V_{th}$. The cell transistor width is set to provide a switching current 1.5 times greater than the critical switching current. This width is selected to ensure that the device operates in precessional mode [10], while allowing the access transistor to be small. The parameters are listed in Table II.

TABLE I. MTJ Parameters

Saturation Magnetization (M_s)	$8 \text{ x } 10^5 A/\text{m}$
Easy Axis	80 nm
Hard Axis	20 nm
Thickness	2.9 nm
R_{on}	5 kΩ
TMR	150%
I_{crit}	39.4 μA

TABLE II. Memory cell Parameters

Technology	22 nm
Supply Voltage (V_{DD})	0.8 V
NMOS (W)	68.2 nm
NMOS (L)	22 nm
Field current line spacing	21 nm
Cell length	161 nm
Cell width	167 nm
Nominal switching current	59.1 μA
Nominal switching latency	6.45 ns

Durlam *et al.* present a classical MRAM cell and memory. Measurements of the field observed by the free layer are demonstrated at a distance of $0.3\ \mu\text{m}$ in a $0.6\ \mu\text{m}$ process. Simple linear scaling of this dimension is not sufficient as the MTJ dimensions are proportionally larger than a classical MRAM. To compensate, the MTJ dimensions are scaled linearly and the thickness of the MTJ stack is assumed to occupy an additional 10 nm. This thickness is typical of many demonstrated STT-MTJ stacks [11], [12].

The cell layout is based on 45 nm FreePDK design rules and scaled to 22 nm, as shown in Fig 2. The cell area is $55.5F^2$. This cell has a relatively large cell density since the layout design rules originate from a logic process. In prior work, the area of a conventional 1T-1MTJ cell is shown to be $49.9F^2$ with the same logic process rules, indicating that the area overhead of the metal line supporting the additional field current is small [13]. Note that a standalone memory process uses tighter design rules and provides greater density.

The magnetic field through a current loop can be approximated by the Bio-Savart's law [14],

$$B = \frac{\mu_0 I_{field}}{2\pi d}. \quad (1)$$

The current through the MTJ induces a spin torque on the

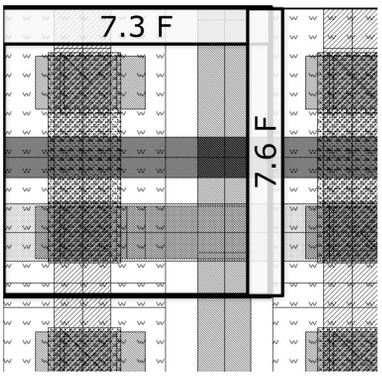


Fig. 2. Layout of a classical MRAM cell

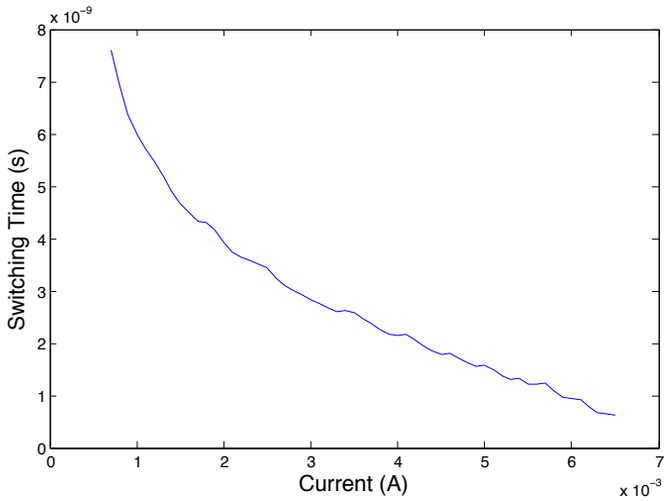


Fig. 3. Switching latency of a field driven classical MRAM cell. The STT switching current is 59.1 μA

free layer, generating a magnetic field that adds linearly to the magnetic field generated by the field current. The magnetic field produced by the STT is assumed to be negligible for two reasons. The STT current is almost two orders of magnitude smaller than the field current, making the field generated by the STT current fairly small. Secondly, the field current is applied to the MTJ before the STT current is applied, ensuring that the free layer magnetization is in an unstable state prior to application of the STT current. As a result, the magnetic field of the STT current does not affect the destabilization process.

The switching latency with increasing field current is shown in Fig. 3. For a 59.1 μA STT current, the MTJ switching latency is depicted as a function of increasing field current. The application of a field current is shown to dramatically reduce the switching time of the cell. Application of a 2 mA current reduces the nominal switching latency from 6.45 ns to 3.93 ns. A maximum applied current of 6.5 mA further reduces the switching latency to 617 ps.

V. Model of MRAM Array

Optimizing the energy consumed by an MRAM array with a field assisted write produces a tradeoff between the size of the array and the current bias that minimizes the switching time of an MTJ. The parasitic impedances of the array, extracted from the cell layout, are listed in Table III [9].

TABLE III. Memory Array Parameters

	Base cell	Wide field lines
R_{flcell} (Ω)	1.7	0.7
C_{flcell} (aF)	13.1	28.8

The array is biased using a field current that traverses the entire row. As the size of the row increases, the energy associated with the field current is amortized over the entire row.

The energy associated with the field current is the sum of the dynamic energy to charge the line as well as the static current to generate the magnetic field. Expression (2) quantifies this dependance, where R_{flcell} and C_{flcell} describe the per cell parasitic resistance and capacitance, N describes the number of cells in a row, R_{access} describes the resistance of the access transistor, V_{DD} represents the supply voltage, $t_{switching}$ is the MTJ switching latency, and I_{field} is the generated field current of the line. The dynamic component is a function of the array width and the DC voltage on the bitline during a write.

$$E_{field} = R_{flcell}C_{flcell}N\frac{NR_{flcell}}{NR_{flcell}+R_{access}}V_{DD} + V_{DD}I_{field}(t_{switching}) \quad (2)$$

The energy of the static current is a function of the field current, supply voltage, and switching time of the MTJ. The static component is independent of array size as the supply voltage is constant and the voltage drop is across the peripheral write drivers and the array. The array field current is also constrained by the resistance of the field line,

$$I_{field}R_{flCell}N \leq V_{DD}. \quad (3)$$

The energy to switch a single MTJ (E_{switch}) is

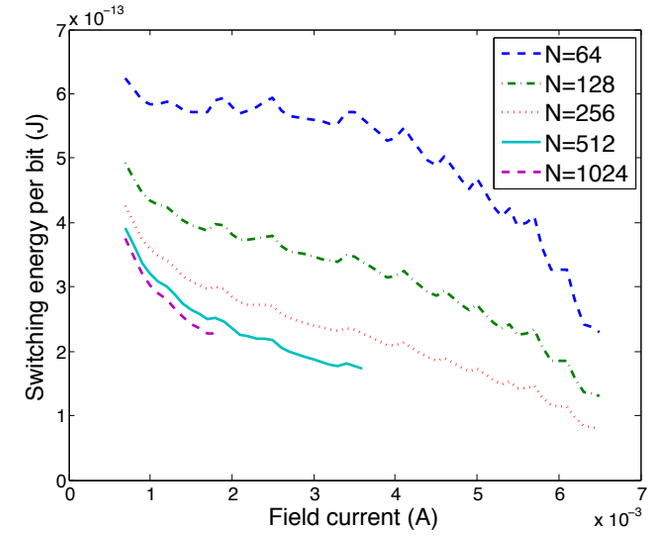
$$E_{switch} = I_{STT}V_{DD}t_{switching}, \quad (4)$$

where I_{STT} is the spin torque switching current. E_{switch} is dependent on the switching time of the MTJ. The total energy per bit is

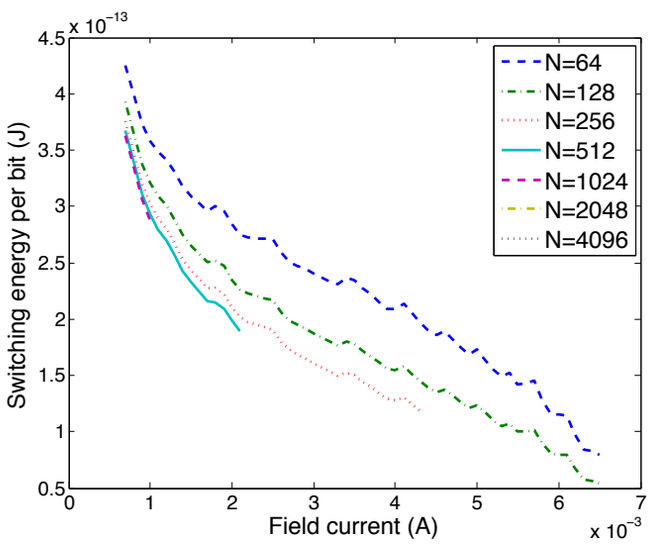
$$E_{total} = E_{switch} + \frac{E_{field}}{N}. \quad (5)$$

The switching energy is shown in Fig. 4(a). For comparison, the minimum energy to switch a nominal MTJ, as described by (4) for a non-field driven MRAM cell, is 0.3 pJ per bit. As illustrated in Fig. 4(a), the number of cells per row at which the field driven approach begins to reduce energy as compared to a nominal MTJ is approximately 64. For larger arrays, the resistance of the bitline constrains the amount of current that passed through the array. Despite this constraint on the maximum field current, the switching energy is reduced to 0.08 pJ per bit for a 64 cell wide array, a 73% reduction in switching energy.

While maintaining the same area and cell density, the metal lines used to generate the magnetic field can be increased to support a larger current. The resistance and capacitance of this



(a)



(b)

Fig. 4. Switching energy of a field driven classical MRAM cell with a) minimum metal pitch, and b) maximum allowed metal pitch

wide field current line are listed in Table III. The switching energy of the cell is further reduced to 0.054 pJ per bit (see Fig. 4(b)) with a corresponding switching latency of 617 ps. Due to the bitline resistance, larger rows support a maximum field current at a specific supply voltage. A sufficiently high field cannot be generated to reduce the switching latency of the MTJ, ensuring that the energy consumption is higher than with a shorter row. An optimum row length therefore exists that minimizes the overall switching energy of an array during a write. In the wide field line case, the optimum row length is 128 cells (see Fig. 4(b)).

VI. Conclusions

This proposed field-driven approach for enhancing latency and power in STT-MRAM is particularly useful for on-chip caches that require low latency, such as L1 caches, and register files within a pipeline. A high thermal stability factor is also required to provide a ten year state retention time. As demonstrated in [15], the retention time can be further reduced to lower the switching current. A reduced thermal switching factor, however, increases the likelihood of a half select problem [16].

The field driven approach utilized in classical MRAM cells is used to reduce the switching latency of an STT-MTJ. An array model is presented that is used to characterize the switching energy and energy consumption for different field currents and array sizes. It is shown that the per bit switching latency can be reduced by a factor of ten. As compared to nominal STT-MRAM, an 82% reduction in switching energy per bit is achieved. The reduction in both switching energy and latency provides significant performance enhancement for embedded high performance STT-MRAM based memories and enables the use of STT-MRAM in write latency critical applications.

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