Inductive Coupling Effects in Large TSV Arrays

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***Abstract*—The effects of inductive coupling among TSVs within large TSV arrays are investigated in this paper. A comparison of the equivalent inductance of a paired TSV model and arrayed TSV macromodel is presented for three TSV distribution topologies, grouped, lined, and uniform, within the power network. Modified closed-form expressions are proposed to determine the equivalent inductance of a TSV in these large TSV arrays. Simulation results show that this method achieves hundred times speed improvement as compared to an electromagnetic field solver while maintaining accuracy within 7%.**

Keywords—through slilicon vias (TSVs); 3-D integrated circuits (3-D ICs); inductive coupling; equivalent inductance

I. Introduction

Three-dimensional integrated circuits (3-D ICs) exploit the vertical dimension, providing a promising technique to extend scaling [1]-[3]. Vertical integration in 3-D ICs yields smaller die area and higher levels of integration. In addition, short vertical TSVs lead to both higher system performance and lower power dissipation. 3-D stacked layers also make heterogeneous integration possible, enhancing the functionality of modern systems. The key technology to achieve the advantageous of 3-D ICs is the through silicon vias (TSVs), the vertical metal connections passing through the silicon wafer between two adjacent layers [3]. In terms of functionality, TSVs can be categorized as signal, thermal, and P/G TSVs. The use of P/G TSVs in 3-D power distribution networks leads to significant challenges in managing power noise in 3-D ICs. The P/G TSVs are the types of TSV considered in this work.

Many models have been proposed to analyze a paired TSV, as shown in Fig. 1 [4]-[8]. In a paired TSV model, only coupling between two adjacent TSVs is considered. These models have been validated by commercial electromagnetic solvers [4]-[8]. A practical structure of a P/G TSV, however, is a large array of tens of thousands of TSVs, as shown in Fig. 2. An example TSV-based 3-D processor-memory system exhibits a physical footprint of 100 mm^2 with a 25 μm pitch between the P/G TSV [9]. The total number of P/G TSVs in a single layer in this system is 160,000, structured within a 400 × 400 array. A paired TSVs model is insufficient to analyze a single TSV within a large array of TSVs. The TSVs surrounding a reference TSV affect the electromagnetic field in dense TSV networks, changing the capacitance and inductance of a specific TSV [10].

II. Analysis of Inductive Coupling Effects

The surrounding TSVs can affect the electromagnetic field within TSV arrays, making coupling among TSVs an issue. There are two types of coupling effects, capacitive and inductive coupling [11]. Due to the computational complexity of inductance and the long range phenomenon of inductive coupling, a computationally efficient and accurate analysis of inductive coupling effects is necessary.

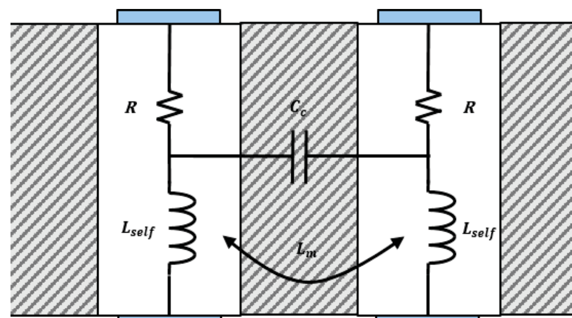

Fig. 1 Electrical parameters in a paired TSV model

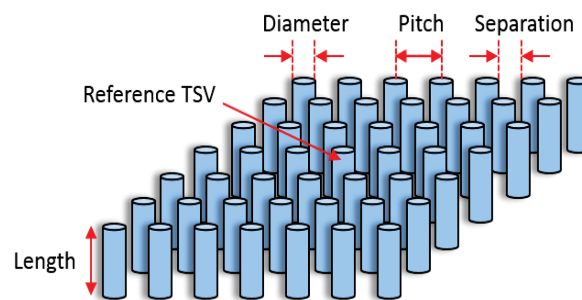

Fig. 2 Large TSV array

A. Long range phenomenon

The electrical parameters characterizing a TSV can be affected by the variation of an electromagnetic field. These parameters include the coupling capacitance C_C between adjacent TSVs, and the equivalent self L_{self} and mutual inductance L_m of a TSV. The resistance of a TSV is determined by the material, geometric, and signal frequency of the reference TSV [12]. Capacitive coupling between TSVs is a short range effect due to the attenuative properties of an electric field. The coupling capacitance therefore does not significantly change between a paired TSV model and an array-based TSV macromodel. Alternatively, inductive effects of a TSV are a long range phenomenon since the inductance behavior of magnetic energy through a magnetic field is a long range phenomenon [13]. In this way, the surrounding TSVs in an array-based TSV

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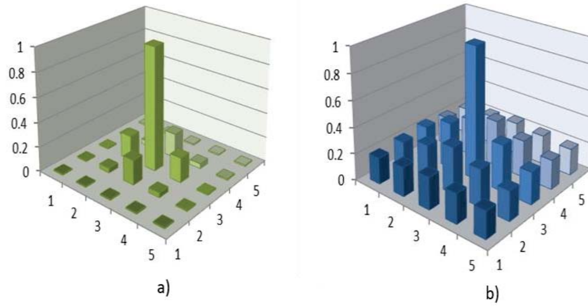


Fig. 3 A 5 × 5 array-based TSV macromodel, a) capacitive effect, and b) inductive effect of surrounding TSVs normalized, respectively, to the equivalent capacitance and inductance of a reference TSV

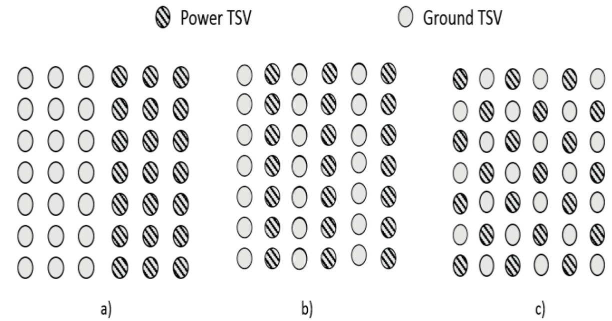


Fig. 4 Three typical power / ground TSV distribution topologies, a) grouped TSV distribution, b) lined TSV distribution, and c) uniform TSV distribution

macromodel have a significant effect on the inductance of a reference TSV.

The effect of the surrounding TSVs on a reference TSV in terms of the capacitance and inductance is shown in Fig. 3, which illustrates the long range property of inductive coupling. The capacitive effects of the surrounding TSVs on a reference TSV are negligible. Long range inductive effects are however considered, as described in the following subsections.

B. Analysis of distribution type of P/G TSVs

The P/G TSV distribution topology is the arrangement and relative position of different P/G TSVs. Three typical distribution topologies are discussed in this paper, grouped, lined, and uniform (see Fig. 4). The grouped distribution is composed of a group of power and ground TSVs on each side of a unit area (see Fig. 4a). The lined distribution consists of lines of power TSVs interdigitated with lines of ground TSVs over the entire surface (see Fig. 4b). Alternatively, the uniform distribution consists of power and ground TSVs regularly spread over the entire surface (see Fig. 4c).

In the analysis of a P/G array-based TSVs macromodel, another phenomenon, called proximity effects, should be considered, particularly when the operating frequency is sufficiently high [13]. The proximity effect describes a phenomenon where the direction of the current within two parallel interconnects affects the current distribution within these two adjacent conductors. This current redistribution phenomenon is due to the effects of the alternating magnetic field caused by a change in direction of the current flow. The proximity effect affects the analysis of an array-based TSV macromodel since the direction of the current in power and ground TSVs is assumed to be opposite. Due to the proximity effect and the long range phenomenon of inductive effects, different distribution topologies of P/G TSVs can affect differently the characteristics of a 3-D power network. Hence, a detailed analysis and assessment of different TSV distribution topologies are necessary.

In the analysis of these three distribution topologies, a similar TSV radius, length, and separation between adjacent TSVs are assumed for each of the topologies. The only difference is the arrangement of the power and ground TSVs. Under this assumption, a negligible difference in resistance or capacitance exists among these three distribution topologies. Alternatively, the inductive effect varies with different distribution topologies. These P/G TSV distribution models have been evaluated by the Ansys Q3D Extractor [14], a quasi-static electromagnetic (EM) solver, to compare the equivalent inductance of each topology.

The equivalent inductance of the three TSV distribution topologies with different array sizes is shown in Fig. 5. Each shade in the histogram refers to a specific TSV distribution topology. As the size of the TSV array increases, the equivalent inductance of the grouped TSV topology becomes larger than the inductance of the other distribution topologies. The equivalent inductance of the lined distribution topology is lower than the inductance of a uniform distribution for a 3 × 3 array and 7 × 7 array. The inductance, however, fluctuates significantly with array size in the lined distribution topology. The uniform distribution exhibits a relatively low and stable equivalent inductance.

The difference between the equivalent inductance of the different TSV distribution topologies can be described by the inductive current loops. A power and ground TSV constitutes a current loop, where the partial inductance of the power TSV decreases due to the mutual effect of the ground TSV. The equivalent inductance of a P/G TSV decreases if the P/G TSV is surrounded by TSVs with current passing in opposite directions (generating a negative mutual inductance, as shown in Fig. 7). Alternatively, the equivalent inductance of a P/G TSV increases if the P/G TSV is surrounded by TSVs with current passing in the same direction (generating a positive mutual inductance). In practical TSV distribution topologies, as illustrated in Fig. 4, both the negative effect and positive effect exist. The contribution of these two effects to the equivalent inductance of the reference TSV therefore depends strongly on the topology of the TSV distribution and the size of the TSV array, explaining why the equivalent inductance varies with different TSV topologies and array sizes.

As important component of on-chip power noise, simultaneous switching noise, is less with a decreasing equivalent inductance. As compared to the grouped and lined TSV distributions, the uniform distribution exhibits a low and relatively constant equivalent inductance. The uniform TSV distribution is therefore a better topology for 3-D power

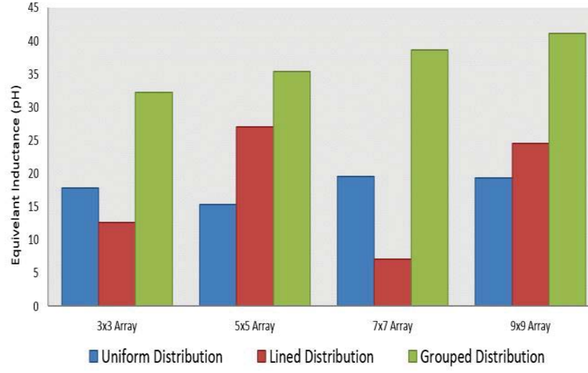
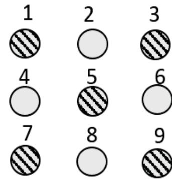


Fig.5 Equivalent inductance of three TSV distribution topologies for different array sizes



$$L_{eq} = L_5 + L_{15} - L_{25} + L_{35} - L_{45} - L_{46} + L_{75} - L_{85} + L_{59}$$

Fig. 7 Partial inductance in a 3 × 3 array-based TSV model

distribution networks from the perspective of lower on-chip power supply noise.

III. TSV Inductance Model of Large Arrays

From the discussion of the three TSV topologies, a uniform TSV distribution is shown to be the most promising topology. In the following analysis, all of the TSV topologies are assumed to be a uniform TSV distribution topology. The equivalent inductance of TSVs in a 3 × 3, 5 × 5, 7 × 7, and 9 × 9 array has been evaluated with Ansys Q3D. A practical P/G TSV array can, however, be as large as 400 × 400 TSVs. Although the equivalent inductance extracted from a quasi-static EM solver is highly precise, the time and memory requirements of Ansys Q3D is intractable with large arrays. A compact model to determine the TSV inductance in a fast and precise manner is therefore highly desirable.

A current loop model is shown in Fig. 6, where a power TSV represents the signal path, and a ground TSV represents the corresponding return path. L_{eq} refers to the equivalent inductance of the power TSV. L_p and L_m are, respectively, the partial inductance of the power TSV and the mutual inductance. The equivalent inductance of a power TSV is $L_{eq} = L_p - L_m$. Note that the relationship between L_p and L_m depends upon the current direction of these two parallel interconnect.

As shown in Fig. 7, the partial inductance is applied to a 3 × 3 array-based P/G TSV model. L_{eq} is $L_5 + L_{15} - L_{25} + L_{35} - L_{45} - L_{65} + L_{75} - L_{85} + L_{95}$, where L_{eq} represents the

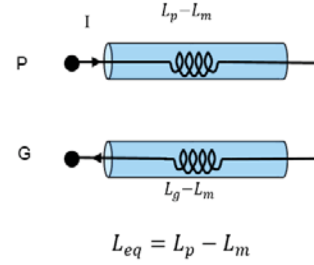


Fig.6 Current loop model represented by a partial inductance

equivalent inductance of the reference TSV, L_5 in Fig. 7. The others terms represent the mutual inductance between the reference TSV and the surrounding TSVs. For example, L_{15} represents the mutual inductance between TSV L_5 and TSV L_1.

A more general uniform TSV distribution array is shown in Fig. 8. The TSV in the center of the array is assumed to be the reference TSV. The 5 × 5 TSV array shown in Fig. 8 is composed of four groups, each group surrounded by a dashed circle with six TSVs. This 5 × 5 TSV array is a centrosymmetric model with the center of symmetry at the reference TSV. All of the groups therefore exhibit the same inductive effect on the reference TSV. Thus, only one group of TSVs is considered here to analyze the inductance of the surrounding TSVs.

For an $m \times n$ case, the equivalent inductance is

$$L_{eq} = L_{self+}$$

$$+4(-1)^{m+n}\beta\frac{\mu_0}{2\pi}\sum_{i=1}^{m}\sum_{j=0}^{n}\left[ln\left(\frac{\frac{L}{P}+\sqrt{\left(\frac{L}{P}\right)^2+m^2+n^2}}{\sqrt{m^2+n^2}}\right)\left(\frac{L}{P}\right)+\right.$$

$$\left.+\sqrt{m^2+n^2}-\sqrt{\left(\frac{L}{P}\right)^2+m^2+n^2}\right]P, \qquad (1)$$

where the individual impedances are described in closed-form expressions [11]. As shown in Fig. 9, the expression (as compared to the EM solver) exhibits a maximum error of less than 7% for 3 × 3, 5 × 5, 7 × 7, and 9 × 9 TSV arrays.

The primary advantage of the proposed expression for determining the equivalent inductance is computational complexity, as listed in Table 1. The run time to evaluate a 9 × 9 TSV array for Ansys Q3D is up to 3 minutes, as compared to less than 1 second using (1). This time difference increases with larger TSV array size. Array sizes of 400 × 400 are intractable with Ansys Q3D. For the closed-form expression, an accurate solution is produced in 105 seconds. Hence, a much faster computational speed is achieved with tolerable (less than 7%) error.

IV. Conclusions

Inductive coupling in large TSV arrays is discussed in this paper. A comparison of the equivalent inductance among three typical distribution topologies of P/G TSVs shows that a uniform distribution is a better topology for 3-D power

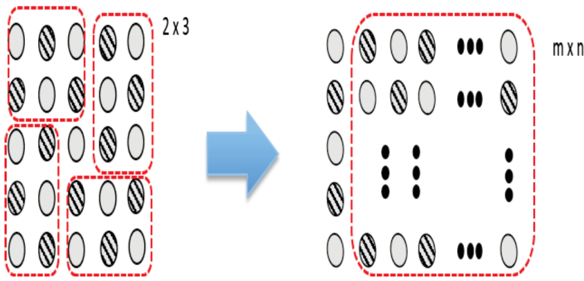


Fig. 8 Equivalent inductance model from a 5 × 5 TSV array to a general uniform TSV distribution

CPU time	3×3 array	5×5 array	7×7 array	9×9 array	400×400 array
Quasi-static solver	5 s	29 s	1 min 29 s	3 min 29 s	—
Algorithm	0.019 s	0.024 s	0.030 s	0.037 s	105 s

Table. 1 Comparison of computational time between closed-form expression and EM solver

distribution networks from the perspective of lower on-chip power supply noise. A closed-form expression is described to calculate the equivalent inductance of a TSV within large TSV arrays. Simulation results demonstrate that the proposed closed-form model achieves significantly faster computational speed than an EM solver while maintaining high accuracy.

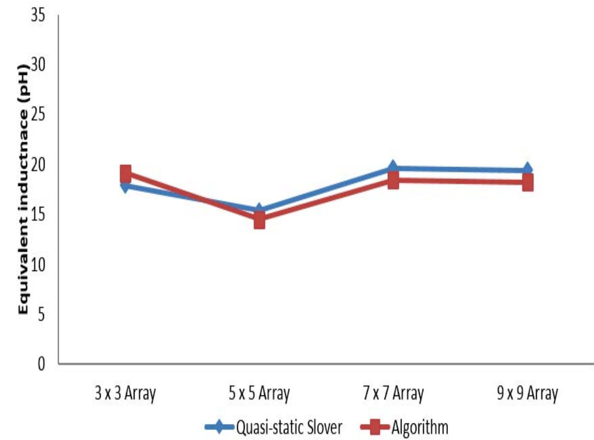


Fig. 9 Accuracy of closed-form expression as compared to EM solver

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