Layer Ordering to Minimize TSVs in Heterogeneous 3-D ICs

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***Abstract*— A layer ordering algorithm to minimize the total number of TSVs within heterogeneous 3-D integrated circuits is described in this paper. Different constraints may complicate the process of ordering the layers within a 3-D system. These constraints are (1) any two layers must be adjacent, (2) a layer must be placed at a specific location, and (3) a layer must be separated from another layer(s). The algorithm generates an optimal layer order given the number of I/Os among all layers. Certain layers can be pre-assigned to specific locations within the 3-D structure. The application of the algorithm to multiple layer 3-D structures significantly reduces the number of TSVs and occupied area as compared to a random layer assignment. The area overhead of a random solution as compared to the optimal solution for unconstrained 3-D systems (without pre-assigned layers) with three to ten layers is, respectively, $\sim 24,090$ μm^2 to $\sim 854,469$ μm^2. In constrained 3-D systems (with pre-assigned layers), the area overhead for an eight layer 3-D system with one to six assigned layers ranges up to $\sim 249,240$ μm^2.**

I. Introduction

With increasing demand for high integration and small form factor, novel integration platforms are required. Systems-on-chip (SoC), systems-in-package (SiP), and 2.5-dimensional platforms have been extensively investigated [1]–[5], and matured into industrial applications [6]. Three-dimensional (3-D) integrated circuits (ICs) are an efficient platform for high integration, where multiple two-dimensional layers are integrated within a single 3-D system. This platform supports heterogeneous circuit integration within a single system [7]. Analog, digital, RF, photonics, and other emerging technologies (*e.g.*, memristors) are types of circuits that can be integrated within a heterogeneous 3-D IC, as illustrated in Figure 1. Each of these layers is manufactured on a different type of substrate and incorporates specialized technologies [8].

3-D ICs are vertically connected using through-substrate-vias (TSVs). These connections are short ($\sim$ 20 μm [9]) vertical interconnects that deliver power, clock, data, and/or remove heat from on-chip hotspots. Three different TSV technologies are currently used: (1) via-first - TSVs are fabricated before the transistors are patterned in silicon, *i.e.*, prior to front-end-of-line (FEOL), (2) via-middle - TSVs are fabricated after FEOL but before the metalization layers are patterned, *i.e.*, prior to back-end-of-line (BEOL), and (3) via-last - TSV formation occurs after the metalization layers are fabricated, *i.e.*, after BEOL [10].

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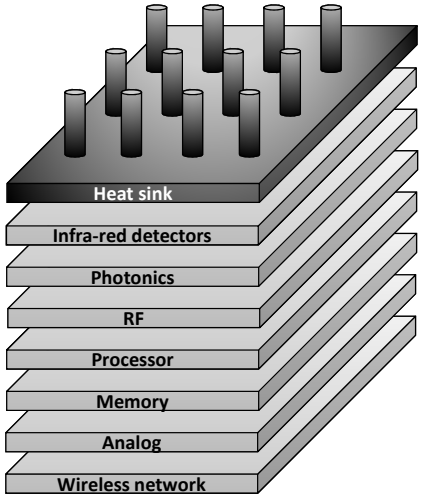

Fig. 1. Heterogeneous 3-D integrated circuit.

Regardless of the TSV technology, the single or bundle of TSVs blocks the substrate, not allowing devices to be placed within that space. The diameter and pitch of modern TSVs are, respectively, 2 to 4 μm and 4 to 8 μm [9]. A design tradeoff therefore arises between the number of TSVs and the area being occupied. To alleviate this issue, an algorithm to minimize the total number of TSVs within a 3-D structure is desirable.

This layer ordering algorithm reduces the number of TSVs within a 3-D IC. Certain constraints however must be considered to ensure high speed, low power, and low thermal coupling. Although the total number of layers within a 3-D system is not excessive [7], the number of possible layer ordering solutions exhibits factorial complexity $O(n!)$. Therefore, despite a small number of layers, a manual solution is impractical. An algorithm to achieve these objectives is therefore presented herein.

The rest of the paper is composed of the following sections. Layer ordering constraints in heterogeneous 3-D ICs are discussed in Section II. An algorithm to minimize the number of TSVs within a 3-D IC using layer ordering and related results on demonstration circuits are introduced in Section III. Some conclusions are offered in Section IV.

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II. Layer Ordering Constraints

Three-dimensional circuits impose different constraints on a layer ordering methodology. Homogeneous 3-D ICs are primarily composed of processor-memory layers and have few constraints. The processor layer is often placed close to the heat sink to ensure efficient heat removal within the 3-D system. Alternatively, in heterogeneous 3-D ICs, the number of constraints on the layers is much greater. Some layers need to be adjacent to specific layers, while other layers can only be placed at specific locations. These constraints are described below.

A. Must be neighbors

An important advantage of 3-D ICs is the short vertical distance between any two adjacent layers, thereby alleviating global signaling issues [7], [11]. To benefit from this advantage, certain layers must be adjacent (neighbors) within a 3-D system, thereby creating a low impedance path between the layers. Satisfying this constraint produces higher speed and lower power circuits.

Some circuits may be divided into several blocks according to different themes (*e.g.,* different voltage domains and active/passive elements). Each of these blocks may be placed on a different layer; therefore, close proximity is important to provide correct functionality. Heterogeneous substrate materials and thicknesses may also require certain layers to be adjacent.

B. Specific location

Thermal congestion is a significant issue in 3-D integrated circuits [7], [8]. The heat becomes trapped within the 3-D structure, and the paths towards the heat sink are high thermal impedance paths [12], [13]. This constraint may drive certain thermally aggressive layers to be placed in close proximity to the heat sink. Mechanical aspects may also place location constraints on different layers. A layer containing optical sensors must be placed at the top of a 3-D structure since optical sensors need to receive incoming light without obstruction. Higher speed and lower power may also constrain layers to certain locations. For example, a sensitive analog circuit may need to be placed close to the power supply.

C. Must not be neighbors

Thermal congestion is an important constraint as thermally aggressive modules need to be separated from thermally sensitive modules [8]. Due to the thermal properties of the different circuits, certain layers should not be adjacent to another layer(s). These layers, therefore, need to be separated by a specific number or type of layer.

Noise coupling from TSVs to the substrate is also an important issue in 3-D ICs. High frequency, high power signals propagating through the TSVs may induce significant noise into the surrounding circuits depending upon the substrate material of the victim layer. The physical separation between the aggressor layers and sensitive victim layers is therefore important.

III. Minimization of Total Number of TSVs

An algorithm to minimize the total number of TSVs within a 3-D IC is introduced in this section. The algorithm generates the optimal order of the layers to reduce the total number of TSVs within a 3-D system. Fewer TSVs translate into smaller on-chip physical area. Application of the algorithm to demonstration circuits is compared to randomly generated layer ordering and the relative area overhead is discussed.

A. Proposed algorithm

Assuming two layers i and j are functionally connected by n I/Os (power/ground, data, control, and thermal TSVs), the number of TSVs required to physically connect layers i and j is

$$N_{TSV} = n \cdot |i - j| \quad . \tag{1}$$

The total number of TSVs in a 3-D system depends upon the order of the layers. The layer ordering algorithm produces a solution with the minimum number of TSVs to realize the I/Os among all layers within a 3-D IC.

The algorithm is illustrated in Figure 2. In the first case, depicted in Figure 2(a), two layers with 1,000 I/Os are placed at locations two and five within the 3-D structure. From (1), the number of TSVs required to physically connect these layers is 3,000. In the second case, depicted in Figure 2(b), the same two layers (with an equal number of I/Os) are placed at locations two and nine within the 3-D structure. From (1), the number of TSVs required to physically connect these layers is 7,000. The additional 4,000 TSVs in the second case do not contribute to the performance of the circuit. On the contrary, these additional TSVs exacerbate coupling noise issues [14] and cause signal degradation due to increased interconnect impedances.

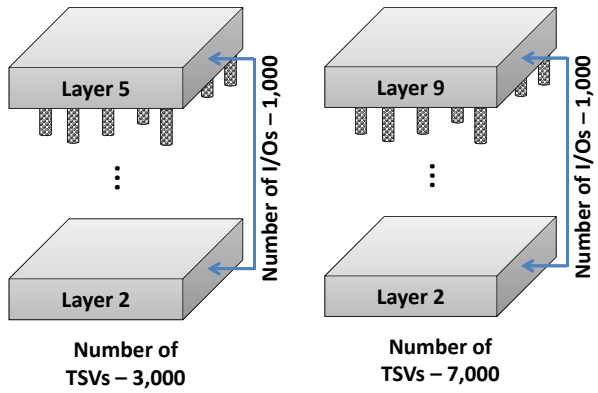

Fig. 2. Number of TSVs between two layers placed at locations (a) 2 and 5, and (b) 2 and 9.

TABLE I

SIMULATION RESULTS FOR THREE TO TEN LAYERS WITHIN A 3-D SYSTEM.

Number of layers	Optimal order	Number of required TSVs	Random order	Number of required TSVs
3	[0 1 2]	3,665	[1 2 0]	5,583
4	[1 0 2 3]	17,452	[3 1 2 0]	20,210
5	[0 1 2 3 4]	43,492	[2 4 3 1 0]	44,547
6	[2 3 0 1 4 5]	48,130	[0 3 5 4 1 2]	62,727
7	[2 0 6 3 5 1 4]	79,976	[4 3 5 2 6 1 0]	89,505
8	[1 0 5 2 4 3 6 7]	120,040	[5 4 2 0 3 1 6 7]	142,959
9	[7 1 6 5 4 2 0 3 8]	166,067	[5 1 7 4 3 2 8 6 0]	219,328
10	[0 4 3 2 1 5 8 9 6 7]	221,658	[7 8 4 0 9 2 3 5 6 1]	289,689

The proposed algorithm accommodates the constraints described in Section II by pre-assigning layers to a specific location within the structure. The order of the remaining unassigned layers is determined by the algorithm, resulting in an optimal solution given the applied constraints. The total number of TSVs in a constrained 3-D structure is greater than the total number of TSVs in an optimized unconstrained 3-D structure.

The algorithm has been implemented in C++ and applies an exhaustive iterative comparison of the cost function, where the cost function is the total number of TSVs. During each iteration, a different order of layers within the 3-D IC is evaluated and the total cost is determined. The order of layers with the smallest cost is recorded and used as a baseline for comparison during the following iterations.

Any layer can be assigned to any location within a 3-D structure prior to the execution of the algorithm. Those layers are fixed during execution; only the remaining, unassigned, layers are reordered during each iteration. In constrained 3-D structures, the applied constraints are evaluated at the beginning of execution of the algorithm to ensure the availability of a valid solution.

The computational complexity of the proposed algorithm is $O(n^2 n!)$. The maximum number of layers (n) within a 3-D system is however not large ($\sim$ ten to twenty layers) [7]. The total runtime of the algorithm for an eight layer 3-D system is 16 msec.

B. Simulation results

An evaluation of the algorithm on three to ten layers is listed in Table I. The results are based on a randomly generated I/O list for each 3-D IC. The I/O list consists of the required connections among all layers within a system. The vertical order within a 3-D IC, the order array, is shown in rectangular brackets from left (bottom of structure) to right (top of structure). The numbers represent the layers, and the locations within the array represent the physical order within the 3-D system. The layer numbers for a 'k' layer 3-D IC are numbered from 0 to k-1. The results exhibit a significant difference between the random solution and the optimal solution. The difference between the number of TSVs for the random and optimal solutions is shown in Figure 3. Note that the increase in TSVs grows rapidly with the number of layers.

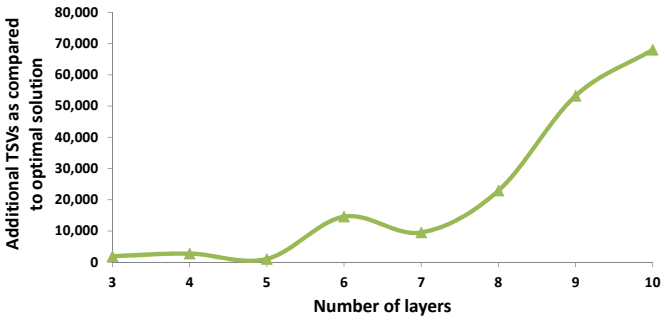

Fig. 3. TSV overhead of random solution as compared to optimal solution.

Assuming a diameter of 2 μm, the area of a TSV is $\pi r^2 = 3.14$ μm^2. The area overhead for a 3-D system with three to ten layers ranges between $\sim 24,090$ μm^2 and $\sim 854,469$ μm^2.

The slope of the curve in Figure 3 has been fitted to the following function: $y = 2101.8x^2 - 18088x + 39492$. This function is second order; therefore, the number of additional TSVs increases quadratically with the number of layers within a 3-D structure.

A more practical application of the proposed algorithm occurs when certain layers are pre-assigned to specific locations within a 3-D IC. A layer is considered pre-assigned when the layer number is fixed to a specific location within the order array, *e.g.*, layer number 2 is considered pre-assigned to the top of the 3-D structure if the number 2 is set to the rightmost place within the order array. Listed in Table II are the evaluation results for an eight layer 3-D system with different combinations of pre-assigned layers (underlined entries in Table II). The number of assigned layers increases from one to six in Table II. The pre-assigned layers are randomly chosen. The remaining unassigned layers are randomly assigned. Each solution is compared to the optimal solution in terms of the total number of TSVs. Note that pre-assigning all layers but one produces similar results for both the random and optimal solutions.

The overhead in the total number of TSVs for a constrained system with a randomly generated order of remaining (unassigned) layers as compared to the optimal order is shown in Figure 4. The area overhead for an eight layer 3-D system

TABLE II

SIMULATION RESULTS FOR A 3-D SYSTEM CONSISTING OF EIGHT LAYERS WITH PRE-ASSIGNED LAYERS (UNDERLINED).

Assigned layers	Optimal order without pre-assigned layers	Total number of TSVs	Optimal order with pre-assigned layers	Total number of TSVs	Random order with pre-assigned layers	Total number of TSVs
[_ _ 5 _ _ _ _ _]	[6 0 4 3 5 1 2 7]	102,628	[7 2 5 1 3 4 0 2]	103,007	[2 0 5 7 3 1 4 6]	122,851
[_ 7 _ _ _ _ 3 _]	[1 6 4 3 2 5 7 0]	119,121	[6 7 2 5 0 4 3 1]	125,414	[2 7 0 1 5 4 3 6]	139,857
[2 _ 6 _ 0 _ _ _]	[0 6 5 1 3 4 7 2]	89,734	[2 4 6 5 0 7 1 3]	113,557	[2 5 6 7 0 3 1 4]	128,263
[_ 1 4 _ 3 _ 6 _]	[0 4 1 5 7 6 3 2]	129,158	[0 1 4 5 3 7 6 2]	135,217	[5 1 4 0 3 7 6 2]	139,023
[3 1 0 _ 4 _ _ 7]	[1 4 6 0 2 3 5 7]	107,842	[3 1 0 5 4 6 2 7]	127,617	[3 1 0 6 4 2 5 7]	130,134
[5 _ 2 3 6 0 4 _]	[0 3 6 5 4 1 7 2]	132,888	[5 7 2 3 6 0 4 1]	157,498	[5 7 2 3 6 0 4 1]	157,498

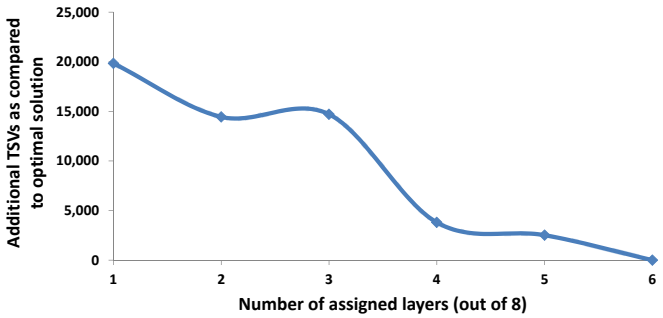

Fig. 4. TSV overhead of random solution as compared to optimal solution, both with pre-assigned layers.

with one to six assigned layers ranges between $\sim 249,240$ µm^2 and zero. The number of degrees of freedom in a highly constrained system, similar to the system represented by the last row of Table II, is low. The total number of TSVs is therefore, for this case, identical for both the random and algorithmically generated solutions.

The slope of the curve in Figure 4 has been fitted to the following function: $y = -4168.5x + 23809$. This function is first order. The number of additional TSVs decreases linearly with the number of pre-assigned layers within the 3-D structure. The benefit of layer ordering is significantly less with an increasing number of constraints.

IV. CONCLUSIONS

A layer ordering algorithm to minimize the total number of TSVs within heterogeneous 3-D integrated circuits is presented in this paper. The relevant constraints posed by layer ordering within 3-D ICs are considered within the proposed algorithm. The algorithm produces the optimal order of layers to minimize the number of TSVs in a 3-D system. The area overhead for a 3-D system with three to ten layers is between $\sim 24,090$ µm^2 and $\sim 854,469$ µm^2. The algorithm has also been evaluated under certain constraints, where different layers are pre-assigned within a 3-D structure. The remaining layers are assigned using the proposed algorithm and compared to a random layer ordering. The area overhead for an eight layer 3-D system with one to six assigned layers is between $\sim 68,929$ µm^2 and $\sim 358,211$ µm^2.

With increasing number of layers within a 3-D system, the area overhead of the TSVs increases quadratically; therefore, managing the order of the layers within a 3-D structure is important. The proposed algorithm is particularly effective in heterogeneous systems that are not highly constrained. The reduction in the number of TSVs in an unconstrained system is approximately forty times better than a 75% constrained 3-D system (for example, six out of eight pre-assigned layers).

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