Design Models of Resistive Crossbar Arrays with Selector Devices

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***Abstract*—Due to recent developments in emerging memory technologies such as MRAM/RRAM, resistive crossbar arrays have gained increasing importance. The size of the crossbar arrays is, however, limited due to challenges brought by the interconnect resistance, sneak path currents, and the physical area of the peripheral circuitry. In this paper, three figures of merit that characterize the limitations of resistive crossbar arrays with selectors, the driver resistance, voltage degradation across the cell, and read margin, are discussed. Models are described that exhibit good agreement with SPICE, exhibiting a maximum error of 6.5% for the worst case voltage degradation during a write operation and 6% during a read operation for voltage ratios above, respectively, 0.5 and 0.25. Furthermore, these models are used to predict device requirements of resistive crossbar arrays with selectors and to project parameter values such as the nonlinearity factor, resistance in the on state, and tolerable interconnect resistance per cell for large scale crossbar arrays.**

I. Introduction

Resistive crossbar arrays originate before the invention of emerging memory technologies such as MRAM, RRAM, and PCM [1]. With the recent development of RRAM devices, resistive crossbar arrays, for use in memory, have gained increasing popularity due to the $4F^2$ density and non-volatility advantages. Existing analyses of resistive crossbar arrays have been primarily simulation based [2]–[4]. In [5], a matrix based solution is presented for solving the voltages and currents of each cell within a crossbar array. This study, however, does not provide intuitive models to support the design of large resistive crossbar arrays due to the complexity of large matrices.

Three challenges in designing resistive crossbar array are considered here; the driver size, voltage degradation across the selected cell, and read margin. For each of these issues, models are described which provide intuition into the design of resistive crossbar arrays while also clarifying device requirements and limitations on array size as interconnects continue to scale.

In Section II, models of the driver size, voltage degradation across the selected cell, and read margin are described and compared to simulation. In Section III, projected device requirements for large arrays are discussed. In Section IV, some conclusions are offered.

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II. Models of Crossbar Array Design Parameters

In this section, expressions that model three important design parameters of resistive crossbar arrays, the driver size, voltage degradation across the selected cell, and read margin, are introduced. For simplicity, an equal number of rows and columns are assumed under worst case conditions. For the write operation, the $\frac{V}{2}$ biasing scheme [6] is considered. For the read operation, the scheme in which a read voltage is applied to the selected row while connecting the remaining portion of the rows to ground and the columns to the sense amplifiers [7] is considered, as shown in Figure 1. In the following sub-sections, the driver resistance, voltage degradation across selected cell, and read margin are discussed.

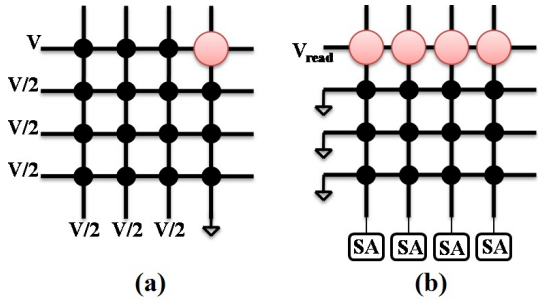

Fig. 1: Biasing scheme for a crossbar array when (a) writing to a cell, (b) reading from a cell.

A. Driver size

An important advantage of a crossbar structure in memory systems is physical density. However, resistive crossbar arrays challenge the peripheral circuits due to the high current required to drive large arrays of closely packed devices. The physical area of a crossbar array is ultimately determined by the devices and the peripheral circuitry as well as the drivers.

The driver resistance depends upon the input resistance of the selected row as well as the voltage drop across the selected cell. Although the lower bound on the resistance of a single memory element could reach tens of kilo-ohms in an RRAM crossbar structure, the effective resistance between the driver at a selected row and selected column(s) drastically decreases with increasing array size. Since the effective resistance is also dependent on the number of selected cells, the driver resistance depends upon whether a read or write operation is executed.

For a write operation, the worst case condition occurs when the selected cell is initially in the on state and switches to the

off state. Since selector devices are in series with the resistive memory elements, a nonlinearity between the full selected cell resistance and the half selected cell resistance is considered. For worst case analysis, the half selected cells are also assumed to be in the on state. With these assumptions, an expression for the driver resistance at the selected row is

$$R_{driver(write)} = \frac{R_{on}(\frac{V_{driver}}{V_{cell}} - 1)}{\frac{N-1}{K_r} + 1}, \quad (1)$$

where R_{on} is the resistance of a cell in the on state, V_{driver} is the driver output voltage when the driver resistance is zero, V_{cell} is the voltage drop across the selected cell, N is the array size (the number of rows and columns), and K_r is the nonlinearity factor, which is the current ratio of the selected cell to the half selected cell. The nonlinearity factor describes to what extent the current flowing into the unselected columns compares to the current flowing into the selected column.

For the case where multiple devices are selected, as in the case of a read operation, the constraint on the driver resistance becomes more stringent. During a single read operation, all of the cells on the selected row are selected. Considering the worst case condition when all of the N selected cells are in the on state, the driver resistance is

$$R_{driver(read)} = \frac{R_{on}(\frac{V_{driver}}{V_{cell}} - 1)}{N}. \quad (2)$$

Assuming negligible selector resistance, the driver resistance during a read operation is independent of the selector devices, and inversely proportional to the size of the crossbar array.

B. Voltage degradation across selected cell

An important limitation on the size of a resistive crossbar array is the interconnect resistance. With interconnect scaling, the resistance per cell has increased drastically, reaching 2.5 Ω for the 22 nm node [8]. It is therefore crucial to consider the effect of parasitic resistance when executing an operation. The worst case selected cell is farthest from the driver on the selected row and farthest from ground on the selected column. For low nonlinearity factors, since the difference in resistance of the half selected cell during the on and off states is significant, the voltage degradation is data pattern dependent. To consider the worst case voltage degradation, all half selected cells and the selected cell are assumed to be in the on state. The cell shown in Figure 1a is an example of a worst case cell for a 4 x 4 crossbar array during a write operation.

A circuit model of a crossbar array during a write operation is considered that includes the interconnect resistance along the selected row and selected column while assuming equal current flowing through the half selected cells between the selected row and the unselected columns. Based on this assumption, the following expression for the voltage across the worst case selected cell is

$$\frac{V_{cell}}{V_{write}} = \frac{1}{\frac{NR_{int}}{R_{on}}(\frac{N-1}{K_r} + 2) + 1}, \quad (3)$$

where R_{int} is the interconnect resistance per cell. As illustrated in Figure 2, (3) agrees with SPICE, exhibiting a maximum error of 6.5% for voltage ratios above 0.5.

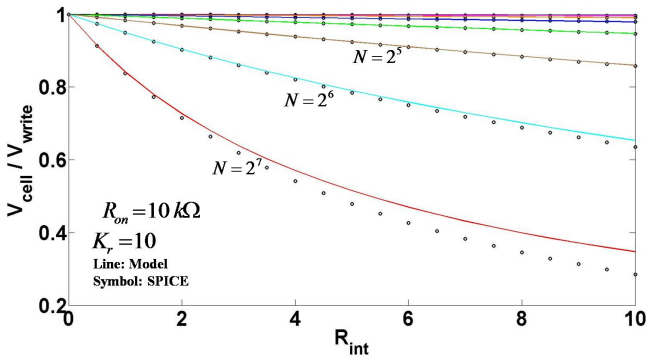

Fig. 2: Ratio of voltage drop across the worst case selected cell to the driver voltage during a write operation.

A circuit model of a crossbar array during a read operation is shown in Figure 3. The worst case cell for the read case is

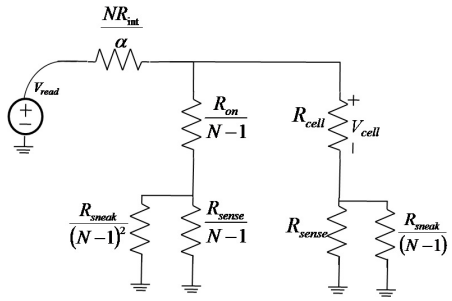

Fig. 3: Circuit model of a crossbar array for the worst case read condition.

farthest from the driver on the selected row, and farthest from the sense amplifiers on the selected columns. Since all of the cells in the same row are selected, the voltage degradation is data pattern dependent. The worst case condition occurs when all of the cells on the selected row are on, including R_{cell}. Based on the circuit model shown in Figure 3, the ratio of the worst case cell voltage to the read voltage is

$$\frac{V_{cell}}{V_{read}} = \frac{1}{(1 + \frac{N^2 R_{int}}{\alpha R_{sel(L)}})(1 + \frac{1}{R_{on}(\frac{1}{R_{sense}} + \frac{N-1}{R_{sneak}})})}, \quad (4)$$

where R_{sense} is the input resistance of the sense amplifier, R_{sneak} is the resistance of the cells between the selected column and unselected rows, α is a fitting parameter, and $R_{sel(L)}$ is

$$R_{sel(L)} = R_{on} + (\frac{R_{sneak}}{N-1} || R_{sense}). \quad (5)$$

The expression in (4) agrees with SPICE, exhibiting a maximum error of 6% for voltage ratios above 0.25 based on the parameter values of R_{on}, α, R_{sense}, and R_{sneak} listed in Table I, as illustrated in Figure 4.

TABLE I: Parameter values for read operation

Parameters	Values
R_{on}	10 kΩ
α	1.5
R_{sense}	100 Ω
R_{sneak}	10 MΩ
R_{off}	10 MΩ

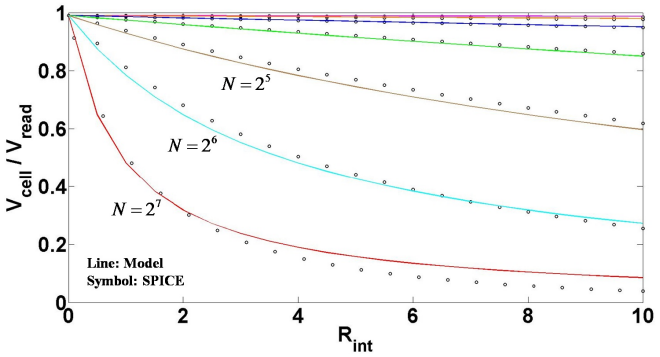

Fig. 4: Ratio of voltage drop across the worst case selected cell to the driver voltage during a read operation.

C. Read margin

An important figure of merit that determines the ability of a sense amplifier to distinguish between two states is the read margin. The read margin is

$$ReadMargin = \frac{(I_{sense(L)} - I_{sense(H)})R_{tran}}{V_{read}}, \quad (6)$$

where R_{tran} is the transimpedance of the sense amplifier matched to R_{on}, $I_{sense(L)}$ is the current flowing into the sense amplifier when the target cell is on, and $I_{sense(H)}$ is the current flowing into the sense amplifier when the target cell is off. The worst case read margin occurs when reading an on state while all of the cells along the selected row are on, and when reading an off state while all of the cells along the selected row are off. In the worst case condition, the selected row is farthest from the sense amplifiers (see, e.g., Figure 1b). Based on these worst case conditions and the circuit model shown in Figure 3, $I_{sense(L)}$ and $I_{sense(H)}$ are described by, respectively, (7) and (8), where R_{off} is the resistance of a memory cell when off, and $R_{sel(H)}$ is

$$R_{sel(H)} = R_{off} + \left(\frac{R_{sneak}}{(N-1)} || R_{sense}\right). \quad (9)$$

The expression in (6) agrees with SPICE, exhibiting a maximum error of 6% for read margins above 0.25 based on the parameter values listed in Table I, as illustrated in Figure 5.

Note the degradation in voltage across the cell with increasing array size (or interconnect resistance), allowing the voltage to fall below the threshold voltage of the selector. The selector resistance can become dominant, making the on and off states indistinguishable. It is therefore crucial to consider the threshold voltage of the selector when estimating the read margin (or voltage drop) across a cell.

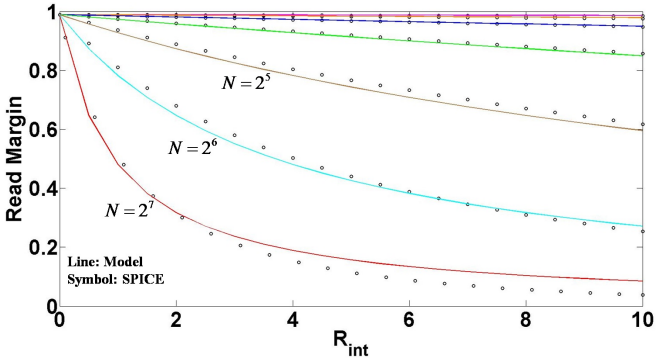

Fig. 5: Comparison of read margin between model and simulation. The maximum error is 6% for read margins above 0.25.

III. Design Requirements for Varying Array Sizes

An important quality of these models is computational efficiency while providing physical intuition on crucial parameters such as K_r, R_{on}, R_{driver}, R_{int}, R_{sense}, and N. The area of the drivers (R_{driver} dependent), process technology (R_{int} dependent), and device requirements (K_r and R_{on} dependent) can be extracted for a target crossbar array size N. Moreover, these models describe the device and circuit requirements for large array sizes and interconnect resistance. In this section, projected design requirements for large arrays are discussed.

A. Driver resistance

The driver resistance in terms of array size is shown in Figure 6. The read operation sets the upper bound on the

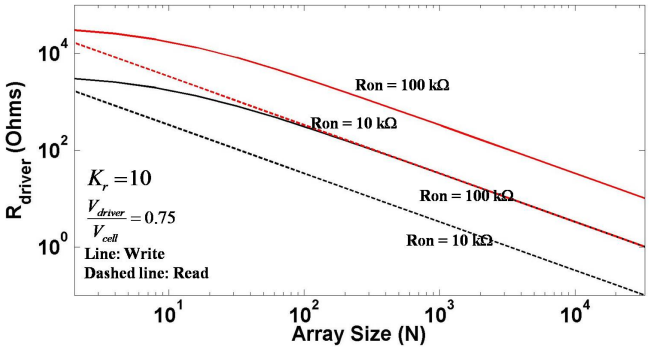

Fig. 6: Driver resistance vs. array size.

driver resistance. From Figure 6, the driver resistance should be below 10 Ω for a large scale crossbar array (> 1 Mbits) with an R_{on} of 10,000 Ω. This constraint requires a large area dedicated to the peripheral circuitry, degrading the $4F^2$ density advantage of RRAM crossbar arrays. This drastic degradation in driver resistance is due to the read scheme. Since selecting a single cell during a read selects all of the other cells on the same row, the input resistance of the selected row is inversely proportional to the array size. During a write operation, due to the nonlinearity of the selector devices, the half selected cell remains at a higher resistance. The input resistance is therefore much greater during a write operation.

$$I_{sense(L)} = \frac{V_{read}}{R_{on}R_{sense}(\frac{1}{R_{sense}} + \frac{1}{R_{on}} + \frac{N-1}{R_{sneak}})(1 + \frac{N^2 R_{int}}{\alpha R_{sel(L)}})} \quad (7)$$

$$I_{sense(H)} = \frac{V_{read}}{R_{off}R_{sense}(\frac{1}{R_{sense}} + \frac{1}{R_{off}} + \frac{N-1}{R_{sneak}})(1 + \frac{N^2 R_{int}}{\alpha R_{sel(H)}})} \quad (8)$$

B. Write operation

An implication of (3) is that a good nonlinearity factor is insufficient in large crossbar arrays. A significantly high R_{on} is essential for large crossbar arrays to maintain a reasonable ratio between the cell voltage and the write voltage. These qualities are noted in Figure 7. A nonlinearity factor greater

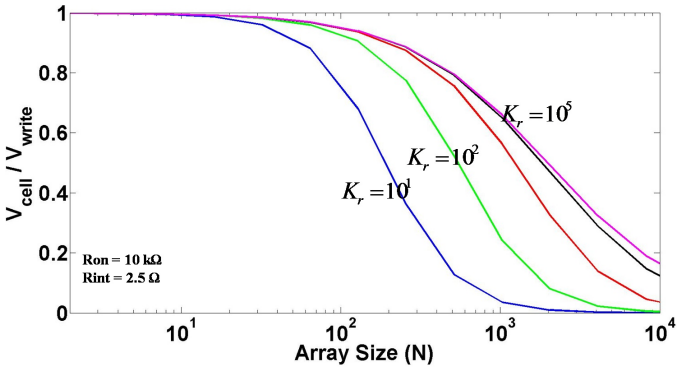

Fig. 7: Voltage degradation vs. array size during a write operation.

than 10^4 only slightly improves the voltage across the worst case selected cell. Beyond 10^4, a higher R_{on} is required to produce a larger voltage drop across the selected cell.

C. Read operation

The denominator of (4), (7), and (8) consists of two different parts. One part considers the loss due to the interconnect resistance while the other part considers the loss due to sneak path currents. The resistance between the selected column and unselected rows R_{sneak} creates a sneak path. Since a voltage forms at the node connecting the column to the sense amplifier, the current flowing through the selected cell is partially lost due to the current flow through R_{sneak}. The current loss due to the sneak path, however, has a negligible effect on the read margin. The degradation in read margin with respect to the array size is shown in Figure 8. The read margin is maintained for crossbar array sizes of up to a gigabit assuming negligible interconnect resistance, as illustrated in Figure 8. The primary limitation is therefore interconnect resistance rather than sneak path currents.

IV. Conclusions

Design models for three important metrics in crossbar arrays are provided, the driver resistance, voltage across the worst case cell (during both writes and reads), and the read margin.

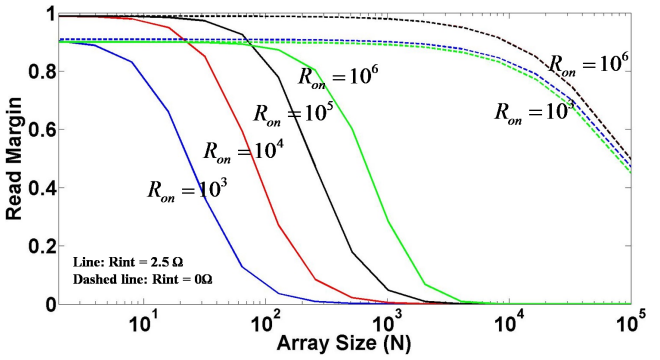

Fig. 8: Read margin vs. array size.

These metrics can be used to provide intuition during the design of resistive crossbar arrays. The models exhibit relatively good accuracy as compared to simulation and can be used to project the performance characteristics of large crossbar arrays. Based on these results, for nonlinearity factors greater than 10^4, voltage degradation during a write operation can no longer be mitigated and R_{on} needs to be increased to prevent degradation of the voltage ratio. For the read margin, sneak path currents are not the primary cause of signal degradation, but rather, the interconnect resistance. Similarly, the models show that a higher R_{on} can greatly improve all three critical metrics that limit the size of a crossbar array.

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