Memristive Model for Synaptic Circuits

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***Abstract*—As a promising alternative for next-generation memory, memristors provide several useful features such as high density, nonvolatility, low power, and good scalability as compared with conventional CMOS-based memories. In this brief, a voltage-controlled threshold memristive model is proposed, which is based on experimental data of memristive devices. Moreover, the model is more suitable for the design of memristor-based synaptic circuits as compared with other memristive models. The effects of memristance variations are considered in the proposed model to evaluate the behavior of memristive synapses within memristor-based neural networks.**

***Index Terms*—Crossbar array, memristor, neural network, synaptic circuits, threshold model.**

I. Introduction

As IT has become increasingly difficult to reduce transistor dimensions [1], alternative methods are desired for manufacturing high-density nanoscale memories. One possible candidate is the memristor, which was first theoretically postulated by Chua in 1971 [2], and later, Williams' team presented a memristor at HP in 2008 [3].

As compared with conventional memories based on CMOS technology, memristors provide several advantages such as high density, nonvolatility, low power, and good scalability [4]. Memristors are particularly suitable for realizing neuromorphic systems since these devices are nanoscale two-terminal devices and can be efficiently integrated within crossbar array circuits [5].

Different models of memristive devices have been developed to describe the characteristics of memristors. In 2009, a model for the HP memristor was proposed by Biolek *et al.* [6]. This model does not include a threshold voltage. An approach for modeling a magnetic flux controlled memristor is presented in [7], although this model also lacks a threshold voltage. The TEAM model was proposed in 2013 [8]. This memristor model is however current controlled while most practical memristive devices are voltage controlled. The TEAM model was extended to the "voltage controlled" VTEAM model in 2015 [9]; however, when the inputs are pulse voltages, the derivative of the state variable is constant. An LTSPICE memristive model quantitatively correlated to multiple devices for both sinusoidal and repetitive sweeping inputs is presented in [10]; however, this model does not match changes in the memristance in recent devices [11]–[15]. Existing models do not describe the synaptic behavior of recent memristive devices in memristor-based neural networks. It is therefore of great significance to provide a memristive model that accurately and effectively characterizes artificial synaptic behavior.

In this brief, a new threshold memristor model based on experimental data is proposed, which matches the current–voltage ($I-V$) characteristics of both sinusoidal and repetitive sweeping inputs and changes in the memristances due to voltage pulses. In addition, the application of the model to a proposed memristor-based synaptic circuit is discussed. The proposed memristor-based synaptic circuit requires fewer amplifiers and resistors as compared with [5]. Moreover, this memristive model can evaluate synapses that consider the effects of variations in the memristance in memristor-based neural networks.

II. Memristive Model

An effective memristive model needs to satisfy several requirements. The model should be both sufficiently accurate and computationally efficient. It is desirable for the model to describe the relevant time in closed form. It is also preferable that the model can characterize a memristor composed of different materials. In this section, a model is introduced and compared with different memristive models. The model is also shown to support different types of materials.

As described by Chua in 1971 [2], the charge-controlled memristor is

$$M(q) = \frac{d\phi}{dq} \tag{1}$$

where $M(q)$ is the memristance (in Ω), ϕ is the magnetic flux, and q is the electric charge. The HP memristor is described by [13], [16]

$$\left.\begin{aligned} v(t) &= R(t)i(t) \\ R(t) &= R_{\rm ON}\frac{w(t)}{D} + R_{\rm OFF}\left(1-\frac{w(t)}{D}\right) \end{aligned}\right\} \tag{2}$$

$$\frac{dw(t)}{dt} = \mu_v \frac{R_{\rm ON}}{D} i(t) f\left(w(t)\right) \tag{3}$$

where $w(t)$ is the width of the doped region, $R(t)$ is the memristance, D is the thickness of the TiO_2, μ_v denotes the average ion mobility, $R_{\rm ON}$ denotes the internal low memristance when the memristor is completely doped, $R_{\rm OFF}$ denotes the internal high memristance when the memristor is completely undoped, and $i(t)$ and $v(t)$ are, respectively, the current and voltage of

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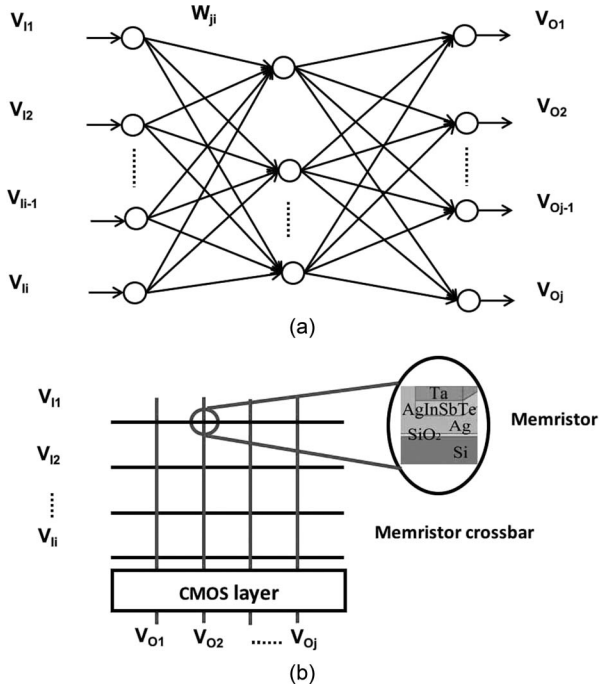

Fig. 1. Architecture of a memristor-based neural network. (a) Artificial neural network. (b) Memristor-based neural network.

the memristor [3]. It is also possible to add a nonlinear ion drift phenomenon, such as a decrease in the ion drift speed close to the bounds, with a window

$$f\left(w(t)\right) = 1 - \left(\frac{2w(t)}{D} - 1\right)^{2p} \tag{4}$$

where p is a positive integer.

Memristor-based neural networks are used to imitate biological neural networks, as shown in Fig. 1. To describe the behavior of memristive synapses within memristor-based neural networks, several recent memristive devices have been fabricated based on different materials, such as the AIST-based memristor [11], [12], PCMO-based memristor [13], [14], and TaO_x-based memristor [15]. The device behavior of AIST-based, PCMO-based, and TiO_2-based memristors, however, cannot be described by the HP model. A new model is therefore proposed here, which matches the behavior of recent memristive devices. The derivative of the state variable in the proposed memristive model is

$$\frac{dw(t)}{dt} = \begin{cases} \mu_v \frac{R_{\rm ON}}{D} \frac{i_{\rm off}}{i(t)-i_0} f\left(w(t)\right), & v(t) > V_{T+} > 0 \\ 0, & V_{T-} \leqslant v(t) \leqslant V_{T+} \\ \mu_v \frac{R_{\rm ON}}{D} \frac{i(t)}{i_{\rm on}} f\left(w(t)\right), & v(t) < V_{T-} < 0 \end{cases} \tag{5}$$

where i_0, $i_{\rm off}$, and $i_{\rm on}$ are constants, μ_v denotes the average ion mobility, and V_{T+} and V_{T-} are, respectively, positive and negative threshold voltages.

Ag (100 nm)/AgInSbTe (25 nm)/Ta (100 nm) stacked capacitor-like memristors have been fabricated and characterized [12]. Different applied voltages change the memristance of the device. A positive bias is the current flowing from the top Ta electrode through the AgInSbTe memristive layer to the bottom Ag electrode. The $I-V$ characteristics can be

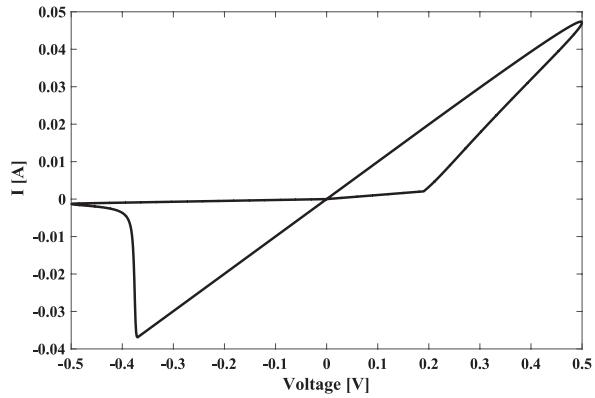

Fig. 2. $I-V$ characteristics of an AIST-based memristor [12].

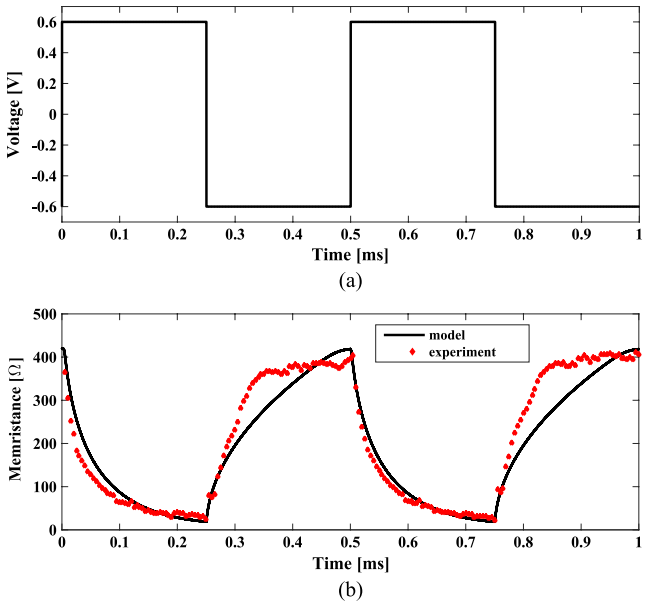

Fig. 3. Change in memristance of an AIST-based memristor [12]. (a) Input voltage, and (b) change in memristance (both simulation and experiment).

evaluated by the proposed model, as shown in Fig. 2. The gradual conductance tuning property under a positive or a negative voltage pulse and the experiment data are also shown in Fig. 3. The proposed model can also be used to evaluate the behavior of a PCMO-based memristor [13], [14] (see Fig. 4) and TaO_x-based memristor [15] (see Fig. 5). The relevant parameters of the proposed model used to fit these different memritive devices are listed in Table I.

A comparison of different memristor models is listed in Table II. Since most practical devices are voltage-controlled threshold memristors, three voltage-controlled models (VTEAM [9], Generalized model [10], and the proposed threshold model) are compared. For READ/WRITE circuits, the memristor is treated as a single-bit memory element. For logic circuits, the memristor is considered as a binary-valued element. The threshold characteristics of the memristor are required for logic operations. For a memristor-based neural synapse, the memristance (or conductance) of the memristors gradually changes with bias voltage.

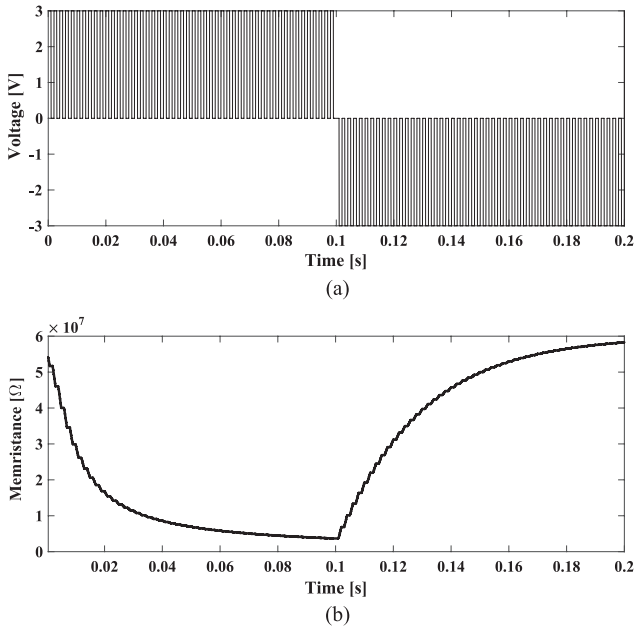

Fig. 4. Change in memristance of a PCMO-based memristor [13], [14]. (a) Input voltage, and (b) change in memristance.

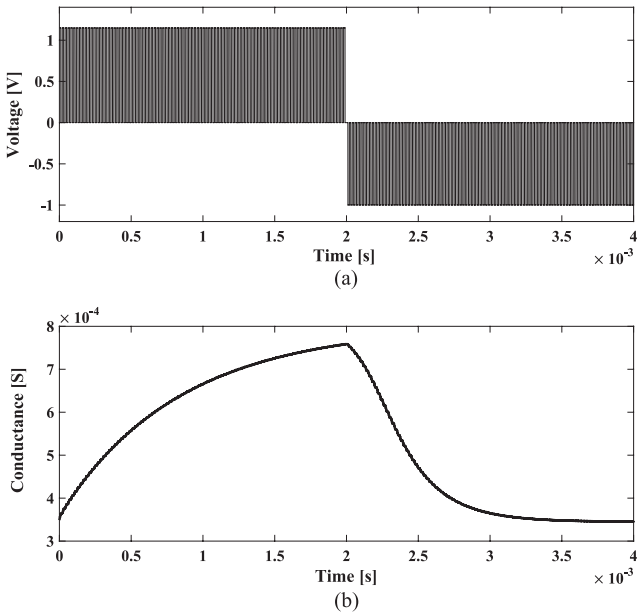

Fig. 5. Change in conductance of a TaO_x-based memristor [15]. (a) Input voltage, and (b) change in conductance.

TABLE I
FITTING CHARACTERISTICS OF THE PROPOSED MODEL TO PRACTICAL MEMRISTIVE DEVICES

Parameters of Physical Device	*AIST-based memristor*	*PCMO-based memristor [14]*	*TaO_x-based memristor [15]*
$R_{\rm ON}(\Omega)$	10	1e6	1250
$R_{\rm OFF}(\Omega)$	420	6e7	2900
$V_{\rm T-}$ (V)	-0.19	-2.4	-0.3
$V_{\rm T+}$ (V)	0.37	1.2	0.5
D (nm)	3	3	3
μ_v ($\rm m^2 s^{-1} \Omega^{-1}$)	1.6e-12	3.2e-15	3.8e-14
$i_{\rm on}$ (A)	1	1	1
$i_{\rm off}$ (A)	1e-5	1.4e-14	5.8e-8
i_0 (A)	1e-3	3e-8	4e-4

Of the three models, only the proposed threshold model can be used to evaluate synaptic behavior and fit different memristors. For example, to model the behavior of a neural synapse, the conductance of the AIST-based memristor changes during application of 50 potentiation pulses (-0.6 V, 5 μs) and 50 depression pulses (0.6 V, 5 μs). The memristance of the PCMO-based memristor changes during application of 50 potentiation pulses (-3 V, 1 ms) and 50 depression pulses (3 V, 1 ms; see Fig. 4) [13], [14], which stores the weight of the neural synapse. In Fig. 5, the conductance of a TaO_x-based memristor changes during application of 100 potentiation pulses (-1 V, 10 μs) and 100 depression pulses (1.15 V, 10 μs) [15].

The derivative of the state variable in the VTEAM model [9] and the Generalized model [10] is constant when the inputs are pulse voltages. In practical memristive devices, if the inputs are positive pulse voltages, the memristance decreases fast at first and decreases slowly at the end of the transition. If the inputs are negative pulse voltages, the memristance increases fast at first and increases slowly at the end of the transition [shown in Fig. 3(b)]. In the Linear ion drift model [6] and the Magnetic flux controlled model [7], despite no threshold voltage if the inputs are positive pulse voltages, the memristance increases slowly at first and increases fast at the end of the transition, which is opposite the behavior of practical devices.

III. APPLICATION IN SYNAPTIC CIRCUITS

In this section, the proposed model is applied to synaptic circuits in Section III-A. Memristors store the synaptic weight in artificial neural networks. The weight change method is presented in Section III-B.

A. Synaptic Circuits

Assume a neural network system that receives a pair of vectors of size M and N: inputs $\mathbf{V}_I \in \mathbb{R}^M$ and outputs $\mathbf{V}_O \in \mathbb{R}^N$. For example, assume $\mathbf{W}$ is an adjustable $N \times M$ matrix and consider the estimator,

$$\mathbf{V}_O = \mathbf{W}\mathbf{V}_I \tag{6}$$

or

$$V_{Oj} = \sum_{i=1}^{M} W_{ji} V_{Ii} \tag{7}$$

where $i = 1, 2, \ldots, M$ and $j = 1, 2, \ldots, N$.

A synaptic array circuit composed of a positive crossbar array of $M^+(G_{ji})$ and a negative crossbar array of $M^-(G'_{ji})$ is shown in Fig. 6. Here, G_{ji} ($G_{ji} = 1/R_{ji}$) and G'_{ji} ($G'_{ji} = 1/R'_{ji}$) are, respectively, the memristor conductance at the crossing point between the ith row and the jth column in the positive and negative arrays. V_{Ii} is the input voltage applied to the ith row. According to Kirchhoff's voltage law, V_{Oj} is

$$\begin{aligned} V_{Oj} &= -\sum_{i=1}^{M} \left(-\frac{R_0}{R_{ji}} \times V_{Ii} \times \frac{R_0}{R_0} + \frac{R_0}{R'_{ji}} \times V_{Ii} \right) \\ &= \sum_{i=1}^{M} R_0 \times \left(G_{ji} - G'_{ji} \right) \times V_{Ii}. \end{aligned} \tag{8}$$

TABLE II
COMPARISON OF DIFFERENT MEMRISTOR MODELS

Model	*Linear ion drift model [6]*	*Magnetic flux-controlled model [7]*	*TEAM [8]*	*VTEAM [9]*	*Generalized model [10]*	*Proposed model*
State variable	$0 \leqslant w \leqslant D$	$0 \leqslant w \leqslant D$	$x_{on} \leqslant x \leqslant x_{off}$	$x_{on} \leqslant x \leqslant x_{off}$	$0 \leqslant x \leqslant 1$	$0 \leqslant w \leqslant D$
Control mechanism	Current controlled	Voltage controlled	Current controlled	Voltage controlled	Voltage controlled	Voltage controlled
I-V relationship	Explicit	Explicit	Explicit	Explicit	Explicit	Explicit
Memristance change	Explicit	Explicit	Explicit	Ambiguous	Ambiguous	Explicit
Threshold charateristics	No	No	Threshold currents	Threshold voltages	Threshold voltages	Threshold voltages
Read/Write circuits	Available	Available	Available	Available	Available	Available
Logic circuits	Unavailable	Unavailable	Available	Available	Available	Available
Neural synaptic circuits	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable	Available

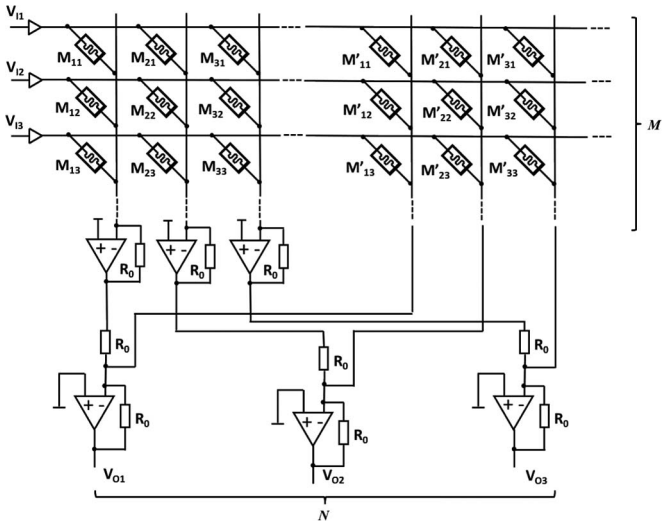

Fig. 6. Proposed synaptic circuits.

The synaptic weight is

$$W_{ji} = R_0 \times \left(G_{ji} - G'_{ji}\right). \tag{9}$$

The proposed synaptic circuit requires fewer amplifiers and resistors, as compared with the work in [5], reducing area and power dissipation.

According to experimental data [shown in Fig. 3(b)], the memristance of an AIST-based memristor can be changed by applying different voltages. When the input voltage is a positive square wave pulse with magnitude of +0.6 V and width of 0.25 ms, the memristance of the AIST-based memristor changes from R_{OFF} to R_{ON}, as shown in Fig. 3. When the input voltage is a negative square wave pulse with magnitude of −0.6 V and width of 0.25 ms, the memristance of the AIST-based memristor changes from R_{ON} to R_{OFF}.

B. Weight Change Process

When the synaptic weight changes, for example, if $\Delta W_{22} > 0$, M_{22} decreases or M'_{22} increases. Similarly, if $\Delta W_{22} < 0$, M_{22} increases or M'_{22} decreases. Consider the weight changes in the positive memristor-based crossbar array $(M^{+}(G_{ji}))$. If $\Delta W_{22} > 0$, weight change voltage $V > 0$. Assume only

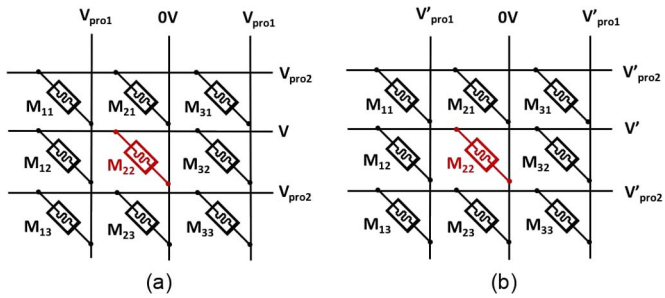

Fig. 7. Proposed weight change in the memristor-based crossbar. (a) Weight increases. (b) Weight decreases.

memristor M_{22} changes and the remaining memristors are unchanged. One possible solution is to apply different voltages on different rows and columns. Weight change voltage V and protect voltages V_{pro2} are applied to, respectively, row 2 and the other rows. Protect voltages V_{pro1} and 0 V are applied, respectively, to the other columns and column 2, as shown in Fig. 7(a). The positive and negative threshold voltages of the synaptic memristors are, respectively, V_{T+} and V_{T-}. Only the voltage of memristor M_{22} is larger than V_{T+}, which is voltage V. The memristance of M_{22} therefore decreases. The voltage of memristors, M_{11}, M_{13}, M_{31}, and M_{33}, is equal to $V_{\mathrm{pro2}} - V_{\mathrm{pro1}}$, and the absolute value is smaller than V_{T-}. The voltage of memristors, M_{12}, M_{32}, is $V - V_{\mathrm{pro1}}$ and smaller than V_{T+}. The voltage of memristors, M_{21} and M_{23}, is V_{pro2} and smaller than V_{T+}. The memristances therefore remain unchanged. The constraint conditions are

$$\begin{cases} V > V_{\mathrm{pro1}} > V_{\mathrm{pro2}} \geqslant 0 \\ V_{\mathrm{pro2}} < V_{T+} \\ V_{\mathrm{pro2}} - V_{\mathrm{pro1}} > V_{T-} \\ V - V_{\mathrm{pro1}} < V_{T+} \\ V > V_{T+}. \end{cases} \tag{10}$$

Similarly, if $\Delta W_{22} < 0$, the weight change voltage $V' < 0$. The weight change voltage V' and protect voltages V'_{pro2} are applied, respectively, to row 2 and the other rows. Protect voltages V'_{pro1} and 0 V are applied, respectively, to the other columns and column 2, as shown in Fig. 7(b). Only the voltage of memristor M_{22} is smaller than V_{T-}. The memristance of M_{22} therefore increases. The voltage of memristors, M_{11}, M_{13},

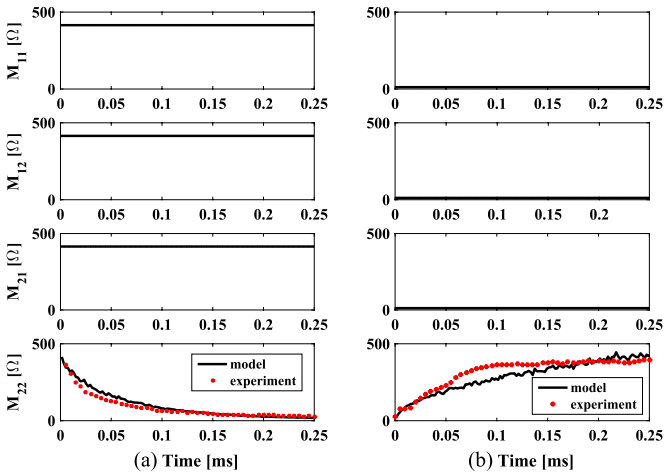

Fig. 8. Change in synaptic weight of memristor M_{22} with 20% memristance variations in the synaptic crossbar array. (a) Increase in weight. (b) Decrease in weight.

M_{31}, and M_{33}, is $V'_{\rm pro2} - V'_{\rm pro1}$ and smaller than V_{T+}. The voltage of memristors, M_{12} and M_{32}, is $V' - V'_{\rm pro1}$, and the voltage of memristors, M_{21} and M_{23}, is $V'_{\rm pro2}$. The absolute value of the voltages is smaller than V_{T-}. The memristance therefore remains the same. The constraint conditions are

$$\begin{cases} V' < V'_{\rm pro1} < V'_{\rm pro2} \leqslant 0 \\ V'_{\rm pro2} > V_{T-} \\ V'_{\rm pro2} - V'_{\rm pro1} < V_{T+} \\ V' - V'_{\rm pro1} > V_{T-} \\ V' < V_{T-}. \end{cases} \tag{11}$$

IV. Experimental and Simulation Verification

Electrical characterization is performed using a probe station (Cascade S300) equipped with a semiconductor characterization system (Keithley 4200-SCS) under the pulse voltage sweep mode. During electrical measurements, the positive bias is the current flowing from the Ta electrode to the bottom Ag electrode. All measurements are performed at room temperature in air. PSPICE is used to evaluate the proposed memristor model and crossbar circuits. The parameters of the AIST-based memristor are listed in Table I.

With the aforementioned method for changing the weight, the simulation results demonstrate that only M_{22} can be changed (see Fig. 8) while the other devices remain in the same state during the weight change process. The amplitude of the applied positive input voltage is 0.6 V or -0.6 V, and the width is 0.25 ms according to Fig. 3. To consider practical conditions, 20% memristance variations are included in the model during the weight change process. The change in memristance in the proposed model matches the experimental data within 18% accuracy, as shown in Fig. 8.

Different sizes of crossbar architectures have been verified, and a similar conclusion is noted that the memristance of the unselected memristors does not change during the weight change process.

V. Conclusion

A memristive model has been presented for memristor-based synaptic circuits. The model is based on experimental data of practical memristive devices and matches the $I - V$ characteristics of both sinusoidal and repetitive sweeping inputs and changes due to voltage pulses. The model can also be tuned to describe memristors composed of different materials. The proposed synaptic circuit requires fewer amplifiers and resistors as compared with [5], reducing area and power dissipation. Moreover, the robustness of the model is verified by 20% additive memristance variations. The accuracy of the model is within 18%, and the proposed synaptic circuits can be used within crossbar arrays of memristive neural networks.

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