Test Point Insertion for RSFQ Circuits

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***Abstract*—A test point insertion technique for enhanced testability in superconductive RSFQ logic is proposed here. Test point insertion reduces the overhead of a set/scan chain while maintaining most of the functionality. The SFQ multiplexers are replaced with mergers and blocking gates. The multiplexer control signals are replaced with a gated clock signal. Clocked blocking gates are used to disable undesired data input. The proposed technique requires 35% fewer Josephson junctions as compared to multiplexers when applied to a 64-bit register. This technique can be utilized to evaluate error prone SFQ circuits and for built-in self-test of SFQ compatible memory systems.**

I. Introduction

Rapid single flux quantum (RSFQ) logic is a superconductive technology for low power, high performance cryogenic computing, first introduced in 1987 [1]. In this technology, information is represented as the presence or absence of a magnetic flux quantum in a superconducting loop, consisting of inductors and Josephson junctions (JJ). The movement of a flux quantum through a loop produces a voltage pulse across a Josephson junction, called a single flux quantum (SFQ) pulse. This technology, with several energy efficient modifications, provides a 200-fold advantage in energy per operation as compared to CMOS [2].

SFQ circuit fabrication and technology development has enabled complex integrated circuits achieving approximately 11,000 JJs for RSFQ digital signal processors of practical significance [3] and similar complexity RSFQ prototype microprocessors [4]. Recently, SFQ circuits with regular layout structures such as an AC-biased SFQ shift register used for fabrication process benchmarking reached 800,000 JJs [5].

Sub-THz clock frequencies achievable by SFQ circuits operating in a cryogenic environment make it difficult to generate and externally control test inputs via probing. Prototype testing of these circuits requires advanced testing methodologies. A design for testability (DFT) capability for SFQ logic is therefore proposed here.

With the complexity and integration of conventional CMOS circuits, multiple automated testing techniques have been developed including built-in self-test (BIST) and automated test pattern generation (ATPG) [6]. A common method to insert and control the test inputs and outputs produced by an arbitrary complex circuit is the use of set/scan chain circuits [7].

Scan chains are used to insert and observe information in serially connected flip flops. The sequential logic is disconnected from the combinatorial flip flops to form a long shift register through which test patterns are shifted by a clock signal. After the state of a register is asserted, combinatorial logic is reconnected to produce an output state. This output is read from the flip flops by connecting the flip flops into a shift register, and the data are shifted out of the register. The data are compared with the expected output.

While the full scan approach provides observability and controllability to all flip flops in a chain, it also introduces significant overhead. Every flip flop requires a multiplexer, as well as additional area for routing.

To reduce this overhead, a modified test methodology has been proposed for CMOS-based scan chains, called *test point insertion* [8]. In this methodology, the combinatorial logic is included within the scan chain. The multiplexers are replaced with AND or OR gates, and placed at the chain boundaries, greatly reducing the overhead of the structure.

Several notable differences between conventional CMOS logic and SFQ logic exist, requiring standard CMOS-based DFT techniques to be modified to support SFQ logic. Traditional CMOS-based scan chains rely on a multiplexer to choose between normal operation and scan mode operation. In SFQ logic, a multiplexer circuit requires 14 Josephson junctions for each bit [9], as compared to only four transistors in CMOS.

Unlike conventional CMOS logic, SFQ logic gates are inherently clocked and latched. Most SFQ logic gates consist of at least one storage loop. Moreover, each logic stage between sequentially-adjacent registers [10] may require several clock cycles to produce an output. The test controller needs to be aware of the number of cycles. Separating the combinatorial logic from the sequential blocks in SFQ logic is therefore more difficult than in CMOS.

Another issue with applying scan chains to SFQ logic is the limited fanout of the gates and flip flops. The fanout of a standard SFQ logic gate and flip flop is one. Providing an additional output for a register requires a splitter cell (one splitter for each bit). The test outputs in a scan chain should therefore be placed sparingly to avoid this significant overhead.

While these issues are disadvantageous for the application of traditional scan chains, SFQ logic also exhibits certain

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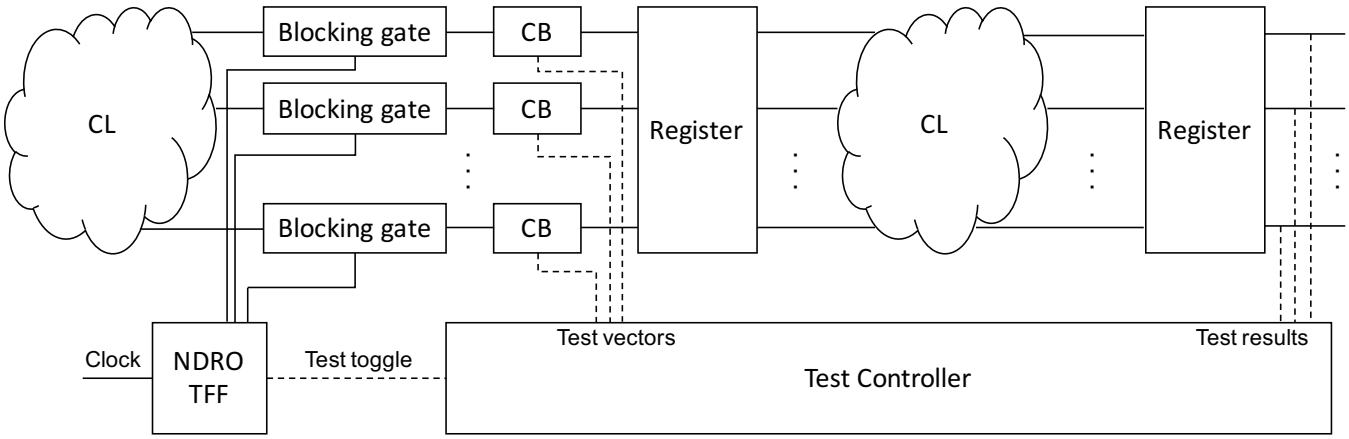

Fig. 1: Proposed test point insertion method. The dashed lines are active connections during test mode.

benefits. The power dissipated by SFQ circuits is small. The additional DFT circuits therefore dissipate negligible power.

II. Test Point Insertion in RSFQ

A modified test point insertion method targeted to SFQ circuits is proposed here. This method utilizes test inputs and outputs along the critical, most error prone logic paths. A test controller ensures correct operation of these paths. By sparingly placing the test inputs and outputs, the overhead of the test circuits is small. By including logic gates along the test path, operation of the combinatorial logic can also be verified.

The pulse based nature of SFQ logic provides inherent isolation of the inputs from the different data sources. If two outputs are connected to one via through a confluence buffer (CB), and one of the input sources is a zero input, the logic element functions correctly with only one input without requiring additional multiplexing circuitry. As a CB only requires five Josephson junctions as compared to 14 JJs for a multiplexer, a CB is preferable for test point operation.

The overall structure of the proposed method is schematically shown in Fig. 1. At the input, the CBs combine a regular data path with the test data path. Normal operation is disabled by a clocked blocking gate, as described in the following section. The test output consists of SFQ pulse splitters at the output of the circuit under test (CUT).

A. Blocking a normal data path

To replace the multiplexers with confluence buffers, it is necessary to ensure that no input pulses arrive at an inactive port of a CB. One method to ensure this behavior is to terminate any upstream signal generation by turning off the logic elements feeding data to the circuit under test. This capability is achieved with a test controller, which supplies predefined test vectors during test mode.

Normal operation of a logic path is turned off when operating during test mode. Multiple methods exist for blocking the normal mode inputs, where the choice depends upon the test controller.

One possible method blocks all upstream logic relative to the CUT. When the test controller initiates the test mode, the upstream logic outputs are turned off and therefore do not affect the test vectors. This method, however, introduces significant overhead into the upstream logic. Furthermore, the test inputs can not be inserted at arbitrary nodes within a logic path, and the test modes are not utilized during normal circuit operation.

Another possible method is to reduce the bias current of the input Josephson transmission line (JTL) within a register, thereby preventing propagation of an incoming SFQ pulse. This method requires a test controller to control the bias current, and a controlled current source.

Normal mode signals are disabled by a blocking gate. This gate either blocks or passes an SFQ pulse. This approach, while requiring considerable overhead, relaxes the requirements on the test controller, allowing a test input to be inserted at any point within a logic path.

An example of a blocking gate is shown in Fig. 2. This

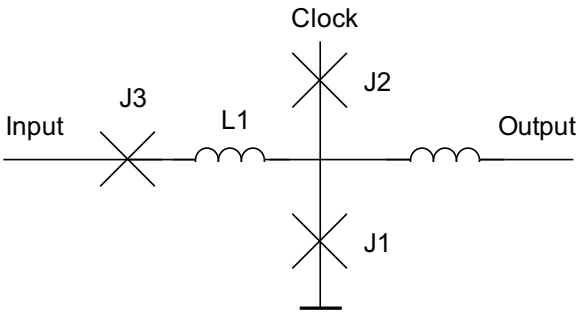

Fig. 2: DFF with an escape junction as a clocked blocking gate.

gate, essentially a D flip flop (DFF), consists of a decision making pair [11] combined with an auxiliary escape junction at the data input. All of the Josephson junctions are shunted, where the Stewart-McCumber parameter [12] β_c is set to 1. Depending upon the persistent current within the J3-L1-J1 loop, the arriving clock pulse either produces a 2π phase change in J2, leading to the absence of an SFQ pulse at the output, or triggers an output SFQ pulse by producing a 2π phase change in J1. Escape junction J3 prevents the blocking gate from being switched by two consecutive input

pulses without a clock pulse. In this case, J3 initially switches, preventing a 2π phase change in J1. An output pulse is therefore not produced.

When the clock input is first enabled after the test mode is initiated, a single flux quantum may be present in the J3-L1-J1 loop. In this case, the flux quantum will escape and produce an output pulse which should be discarded. While this spurious output can be detrimental when the gate is used in a logic operation, for DFT purposes, this pulse only extends the test mode by one clock cycle, and therefore has a negligible effect on the test operation.

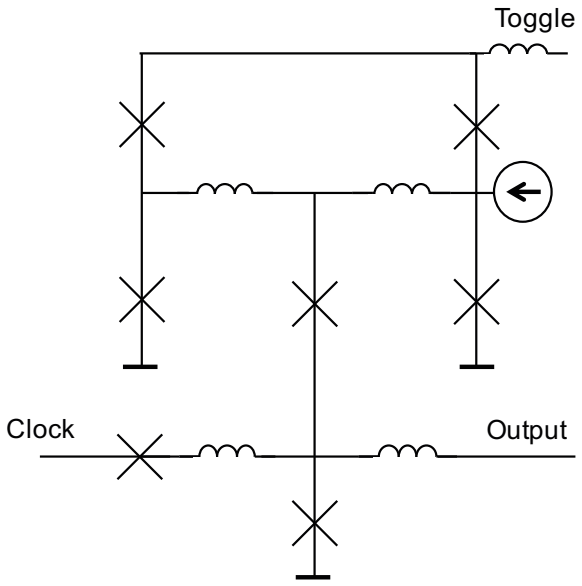

Fig. 3: NDRO T flip flop.

The clocked blocking gate is combined with each bit of the normal data path and is enabled by a clock signal. This clock is gated during test mode. When the clock is enabled at this gate, the data path is transparent to any incoming SFQ pulses. When the clock is disabled, no output is produced. The gated clock can be a non-destructive readout (NDRO) T flip flop attached to a clock output. An NDRO T flip flop is shown in Fig. 3, and consists of a T flip flop and an NDRO D flip flop [9].

With a T flip flop toggle input, the circuit switches between normal and test mode. A clock signal passes from a nearby register through an SFQ pulse splitter. The clock skew between the upstream logic and the blocking gate can be tuned to minimize the delay introduced by the blocking gate during normal operation [13], [14].

The temporal behavior of the combination of a clocked blocking gate with a merger is shown in Fig. 4. Correct multiplexing of data and test inputs is achieved, provided no signals originate from the test controller when not operating in test mode. By attaching clocked blocking gates to both inputs of the merger, full functionality of a multiplexer is duplicated independent of the data inputs while requiring only 11 JJs.

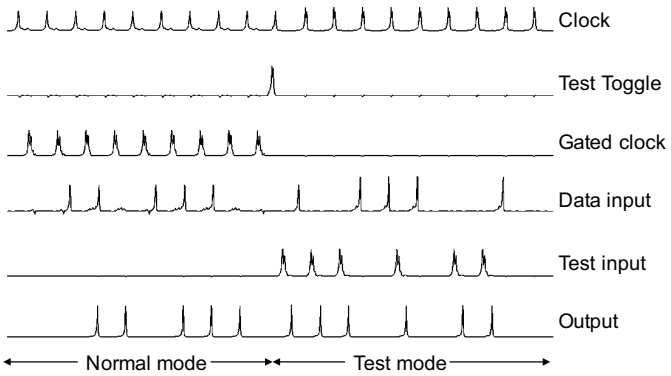

Fig. 4: Waveforms illustrating multiplexer operation performed by a blocking gate and a merger.

B. Test process

After blocking the normal data path, the CUT is supplied with test vectors. These vectors provide sufficient coverage of the circuit functionality. As each logic element requires multiple clock cycles to process the entire scan chain, the timing characteristics are included within the expected result by adding the correct number of clock cycles between output data.

The test controller for a CUT can include either predetermined test vectors or the test vectors can be supplied by an external BIST/ATPG controller. Similarly, the output for the predetermined test vectors can be saved on-chip in a ROM or stored externally.

After the CUT produces a set of output responses for a set of input test vectors, the output response is passed to the test controller using splitter gates and transmission lines. These signals are compared with the expected results from the test controller. Alternatively, the outputs can be compared off-chip.

C. Comparison to multiplexers

The proposed gate, consisting of a CB and a merger, is compared to multiplexers to achieve the same function. An SFQ multiplexer consists of 14 Josephson junctions switched by set/reset inputs [9]. The SFQ pulse mergers are combined with clocked blocking gates, requiring fewer JJs for the gates, and only one control signal for a clock with $log_2 n$ splitters (as opposed to two networks, set and reset, required by a multiplexer).

As the splitter gates are required to provide additional fan-out for the test readout, the overhead of the readout circuit is set by the complexity of the splitter gate. A typical splitter gate consists of three JJs [9], and is placed on each bit of the output interface. The overhead of the test readout for the multiplexers and blocking gate/CB combination is the same.

The following expressions describe the number of JJs required for each test point as a function of the data bus width. The number of required junctions J_m if regular multiplexers are used is

$$J_m = (M + S) * n + 2 * log_2(n) * S. \quad (1)$$

TABLE I: Number of junctions per function, see (1) and (2) [9].

Parameter	Description	Number of JJs
M	Multiplexer	14
S	Splitter	3
B	Clocked blocking gate	3
C	Confluence buffer	5
T	NDRO T flip flop	7

The number of required junctions J_c by the clocked blocking gates and confluence buffers is

$$J_c = (B_1 + C + S) * n + log_2(n) * S + T + S. \quad (2)$$

where n is the width of a data path, M is the number of JJs in a multiplexer gate, and S and C are, respectively, the number of JJs in a splitter and confluence buffer. T is the number of JJs in a NDRO T flip flop. B is the number of JJs in a clocked blocking gate. The number of JJs for each of these gates is listed in Table I.

A comparison of the number of JJs for these two approaches for different bus widths is shown in Fig. 5. The data for this plot are generated from (1) and (2). The advantages of the proposed technique increase with wider data paths. For a 64-bit register, the use of multiplexers for test point insertion requires 1,124 JJs, while the proposed technique only requires 732 JJs, a 35% improvement.

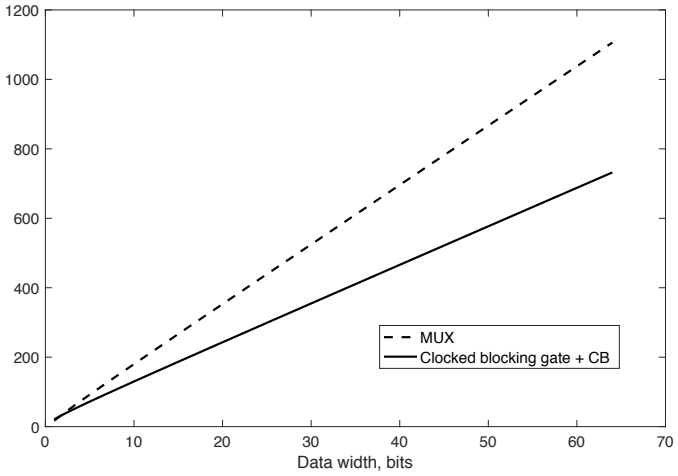

Fig. 5: Number of junctions in proposed gates as compared to multiplexers.

D. Advantages and disadvantages

As compared to the traditional scan chain approach widely used in CMOS, this technique does not place data in arbitrary registers, restricting the set of testable circuits. Multiple logic stages between registers are not bypassed, requiring changes in the input data to provide sufficient coverage. As this method includes sequential test pattern generation, similar to CMOS, considerable computational resources are necessary to choose an optimal set of test vectors and to determine the expected outputs, particularly with logic paths containing feedback [15].

As compared to a straightforward application of the test point insertion technique to SFQ logic, the proposed method replaces the multiplexers with clocked blocking gates and confluence buffers to reduce the area overhead. As compared to the set/scan chain technique, the proposed method provides test coverage of both the registers and sequential logic gates.

III. Conclusions

A test point insertion technique for RSFQ circuits is proposed. This method can be used to test critical and error prone logic paths, and is particularly useful for testing complex operations on wide data buses. In addition, the method can be used with a memory BIST controller to provide access to address, data, and control lines within a memory block with negligible overhead.

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