Hybrid Write Bias Scheme for Non-Volatile Resistive Crossbar Arrays

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***Abstract*—Crossbar arrays based on non-volatile resistive devices are planned for future memory systems due to the scalability and performance as compared to conventional charge based memory systems. To enhance the feasibility of these resistive memory systems, the energy consumption needs to be reduced. The write operation of a resistive memory based on a one-selector-one-resistor crossbar array consumes significant energy. The energy consumed by a crossbar array is dependent on the device and interconnect characteristics as well as the bias scheme. While the device and circuit parameters are the same for a specific application, the bias scheme of an array can be tuned to improve the energy efficiency. In this paper, an intelligent write scheme is proposed to provide a hybrid bias scheme. The proposed system adaptively sets the bias schemes to enhance energy efficiency. The most energy efficient bias scheme depends upon several parameters such as the size of the array, nonlinearity factor, and number of selected cells. For a specific array size and device characteristics, a power delivery system is described that sets the bias voltages based on the number of selected cells. Energy improvements of more than 2x are demonstrated with this hybrid bias scheme.**

I. Introduction

Resistive memories are expected to replace charge based conventional memories due to scalability limitations and energy benefits from non-volatility characteristics. Resistive memory devices such as resistive RAM (RRAM), phase change memory (PCM), and magnetic RAM (MRAM) have been explored for non-volatile memories [1], [2]. These resistive devices are placed within a crossbar array structure for high density. The area of a memory cell in an RRAM based crossbar array utilizing a one-selector-one-resistor (1S1R) configuration can be as low as $4F^2$, where F is the minimum feature size of a technology node. The energy consumption of 1S1R memories increases significantly with larger array size. In particular, the write energy is a large portion of the total energy and is significantly greater than the read energy [3]. This difference is due to the long switching times of the selected devices whereas the read latency primarily depends upon the sense amplifier which improves with technology scaling. The write latency is typically on the order of a few hundred nanoseconds whereas the read latency can be as low as 5 ns [4]. While the write latency can be lowered using higher write voltages, the disturbance across half-selected cells limits the maximum write voltage. Moreover, higher write voltages significantly increase the write current of the selected and half-selected cells, thereby exacerbating the voltage degradation due to IR drops along the interconnects.

In this paper, an intelligent write scheme is proposed to reduce the write energy of a 1S1R crossbar array by adapting a hybrid bias scheme. The write energy is reduced by choosing the appropriate bias scheme depending upon the number of selected cells. A 1S1R crossbar array is biased either using a $V/2$ bias scheme or a $V/3$ bias scheme, as shown in Fig. 1 [5], [6]. During a write operation, the selected row (wordline)

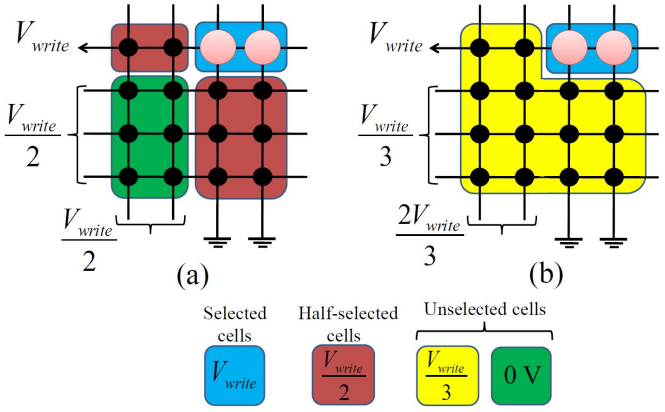

Fig. 1: Bias scheme of a 1S1R crossbar array, (a) $V/2$ bias scheme, and (b) $V/3$ bias scheme.

of the crossbar array is biased with the write voltage and the selected columns (bitlines) connected to ground. With the $V/2$ bias scheme, the unselected rows and columns are connected to one half of the write voltage. With the $V/3$ bias scheme, the unselected rows are biased at one third of the write voltage whereas the unselected columns are biased at two thirds of the write voltage. Hence, the voltage across the half-selected cells on the selected row and columns for the $V/2$ bias scheme is one half of the write voltage and the voltage across the unselected cells is zero. For the $V/3$ bias scheme, the voltage across all of the unselected cells is one third of the write voltage. The proposed hybrid write scheme switches between the two bias schemes to improve the energy efficiency by monitoring the number of selected bits for each write operation. Since this hybrid approach requires both the $V/2$ and $V/3$ bias schemes, four different voltage levels are necessary. To accommodate these on-chip voltages, a power delivery system using on-chip LDOs is proposed to lower cost

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due to the limited number of power I/Os and the area of the printed circuit board (PCB) for the off-chip power supplies.

In Section II, models describing the energy of a 1S1R crossbar array are presented. The effect of the nonlinearity factor, array size, bias scheme, and number of selected cells on the energy consumption is also discussed. In Section III, the proposed hybrid write scheme is described. The potential challenges and overhead are discussed. Some conclusions are offered in Section IV.

II. Energy Consumption of 1S1R Crossbar Array

The energy consumption of a 1S1R crossbar array is modeled considering the size of the array, number of selected cells, bias scheme, device and selector parameters such as the on and off resistance as well as the nonlinearity factor, and switching time for the case when the interconnect resistance is negligible. An equal number of rows and columns is considered. The selected devices are modeled based on VTEAM [7] considering linear switching, and the remaining devices are modeled as resistors. The switching devices are considered to be symmetric with equal on/off threshold voltages and equal set/reset times. The energy of a 1S1R crossbar array for the $V/2$ and $V/3$ bias schemes are, respectively,

$$E_{V/2} = V_{write}\frac{I_{on}}{K_{V/2}}\frac{(Nn+N-2n)}{2}t_{sw} + nE_{sw}, \quad (1)$$

$$E_{V/3} = V_{write}\frac{I_{on}}{K_{V/3}}\frac{(N^2-n)}{3}t_{sw} + nE_{sw}, \quad (2)$$

where V_{write} is the write voltage, I_{on} is the cell current when biased with the write voltage during the on state, N is the number of rows and columns, n is the number of selected cells, t_{sw} is the switching time, and E_{sw}, $K_{V/2}$, and $K_{V/3}$, are, respectively, the switching energy consumption of the selected device, nonlinearity factor for the $V/2$ bias scheme, and nonlinearity factor for the $V/3$ bias scheme,

$$E_{sw} = \frac{V_{write}^2}{R_{off}-R_{on}} ln(\frac{R_{off}}{R_{on}})t_{sw}, \quad (3)$$

$$K_{V/2} = \frac{I_{cell}(V_{write})}{I_{cell}(V_{write}/2)} = 2\times\frac{R_{on@V_{write}/2}}{R_{on}}, \quad (4)$$

$$K_{V/3} = \frac{I_{cell}(V_{write})}{I_{cell}(V_{write}/3)} = 3\times\frac{R_{on@V_{write}/3}}{R_{on}}, \quad (5)$$

where $I_{cell}(V_{write})$, $I_{cell}(V_{write}/2)$, and $I_{cell}(V_{write}/3)$ are, respectively, the current passing through the cell when the cell voltage is equal to the write voltage, one half of the write voltage, and one third of the write voltage, and R_{on}, $R_{on@V_{write}/2}$, and $R_{on@V_{write}/3}$ are, respectively, the cell resistance during an on-state when the cell voltage is equal to the write voltage, one half of the write voltage, and one third of the write voltage. Lastly, R_{off} is the cell resistance during an off-state.

The energy models are in good agreement with SPICE, exhibiting an average error of 0.28% and a maximum error of 4.5%, as shown in Fig. 2. Due to the different scaling behavior of the energy for the two bias schemes, a crossbar array can be more energy efficient by choosing the appropriate bias scheme. Variations in the energy consumption for the two bias schemes with respect to N and n is shown in Fig. 3. Note that while the energy for both bias schemes increases with larger array size, depending upon the number of selected cells n, one bias scheme can achieve a higher energy efficiency as compared to the other bias scheme. The $V/2$ bias scheme is typically more energy efficient for large arrays ($N > 256$) and a small number of selected cells whereas the $V/3$ bias scheme is more energy efficient for smaller arrays with a large number of selected cells. It is therefore possible to improve the energy efficiency for a given array size by switching between bias schemes as the number of selected cells vary from one write operation to another write operation.

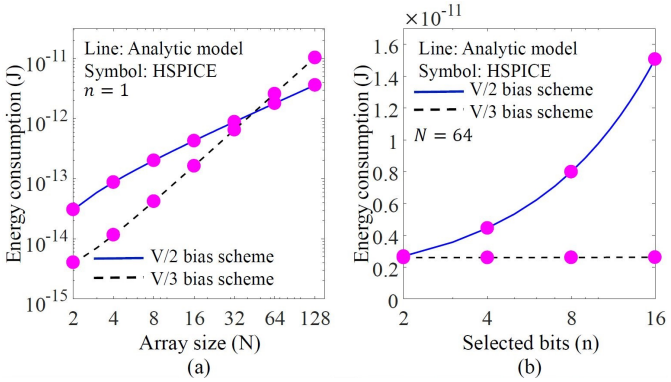

Fig. 2: Energy consumption of a crossbar array with respect to (a) array size, and (b) number of selected cells, assuming R_{on} = 10^4, R_{off} = 10^7, $K_{V/2}$ = 10, and $K_{V/3}$ = 150.

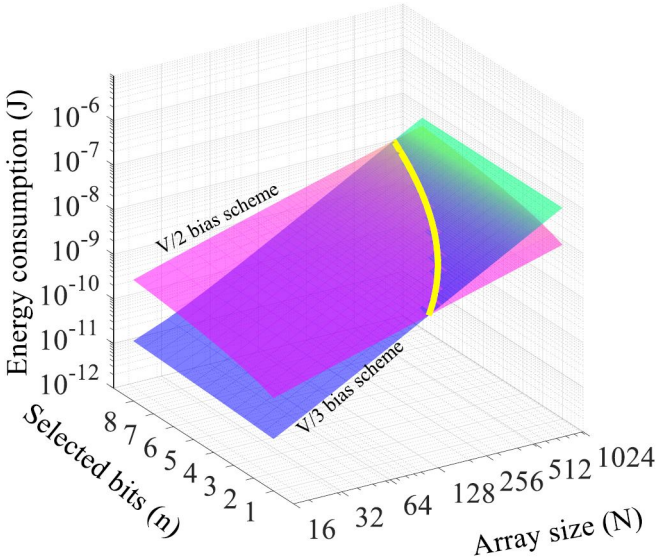

Fig. 3: Comparison of the energy consumption for the $V/2$ and $V/3$ bias schemes in terms of the array size and number of selected cells, assuming R_{on} = 10^4, R_{off} = 10^7, $K_{V/2}$ = 20, $K_{V/3}$ = 1000, V_{write} = 4 volts, and t_{sw} = 100 ns.

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III. Energy Efficienct Hybrid Write Scheme

In this section, a hybrid write scheme is proposed to improve the energy efficiency of a crossbar array during write operations. The optimal choice of energy efficient bias scheme is explained in Section III-A. The overhead and challenges of the proposed system are discussed in Section III-B.

The number of selected cells affects the energy of an array and can be used to determine the most energy efficient bias scheme. The proposed hybrid write scheme improves energy efficiency by switching between the $V/2$ and $V/3$ bias schemes depending upon the number of selected cells during a write operation. The number of selected bits during a write operation depends upon the difference between the patterns of the old data and the new data, as shown in Fig. 4. Considering

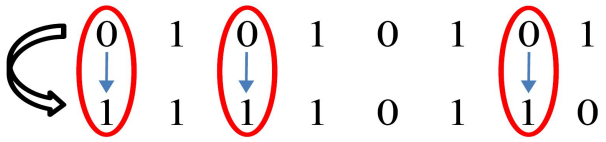

Fig. 4: Writing an eight bit word. Four bits of the new string are the same as the old string; however, only three bits are selected since one bit requires a reset whereas the other three bits require a set operation.

a word size of eight bits, if the new data is the same as the old data, the number of selected cells is equal to zero. If however the new data is different from the previous data, the number of selected cells depends separately upon the number of sets and resets, since in resistive memories writing a 1 or a 0 requires two different write operations. To determine the number of bits, a read-before-write technique is typically used [8]. This approach detects those cells that require switching, reducing excessive energy consumption during a write. By adopting a similar approach to monitor the number of selected cells during each write operation, the optimal bias scheme for energy efficiency can be determined.

While the $V/2$ bias scheme requires two voltages, V_{write} and $V_{write}/2$, the $V/3$ bias scheme requires three voltages, namely, V_{write}, $V_{write}/3$, and $2V_{write}/3$. A hybrid solution using both bias schemes therefore requires four voltage levels. Providing a large number of heterogeneous on-chip voltages is challenging due to the limited board area for the off-chip power supplies and the limited number of power I/Os. To provide a heterogeneous power delivery system with a large number of voltages, on-chip capacitor-less LDOs are used [9]–[11]. In [12], a boost converter with a charge pump is used to bias the array. This approach is however not feasible for a hybrid bias scheme with multiple voltage levels since the switching converter requires large off-chip inductors as well as large capacitors [13]. Capacitor-less LDOs, alternatively, are less efficient as opposed to switching converters; however, are much smaller since bulky capacitors or inductors are not required [14]. Thus, on-chip LDOs can provide greater regulated power per area, with hundreds of regulators distributed across a die [10]. Moreover, on-chip LDO regulators can be placed close to the load, further reducing the response time while providing fast local power management to control the bias scheme as opposed to an off-chip power management solution with higher latency. The proposed intelligent write scheme exploits programmable on-chip capacitor-less LDOs to provide four different voltage levels necessary for the hybrid bias scheme, as shown in Fig. 5. This intelligent

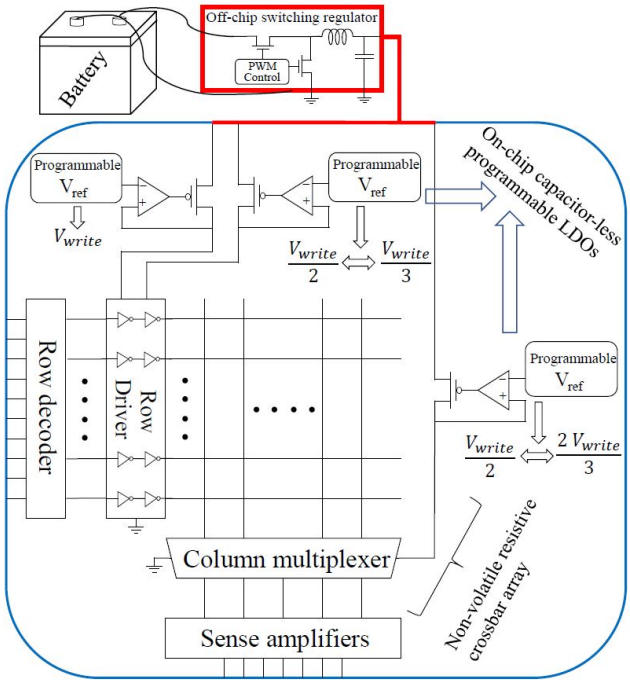

Fig. 5: An intelligent power delivery system to operate a crossbar array using a hybrid bias scheme. The power delivery system switches between the $V/2$ and $V/3$ bias schemes to reduce the energy consumed during write operations.

power delivery system uses three different on-chip capacitor-less LDOs to simultaneously provide the write pulses to the selected wordline, unselected wordlines, and unselected bitlines. By programming the reference voltage of the LDOs, the bias scheme can be altered between $V/2$ and $V/3$ [15]. Alternatively, the LDOs can be programmed by tuning the resistive divider at the output of the regulator [16]. Note that by adding an additional LDO, the four voltage levels can be supplied simultaneously, thereby eliminating the overhead associated with programming the regulators at the expense of additional die area.

The steps summarizing the write process using this intelligent write scheme is shown in Fig. 6. The initial step is a read-before-write operation followed by counting the number of cells that will switch for the new string of data. Once the number of selected cells n is known, it is compared to n_{th} for a specific array (see Section III-A). Following this step, the LDOs are programmed to lower the energy by supporting either the $V/2$ or $V/3$ bias schemes. Finally, the write pulse is executed to write the new data and complete the write process.

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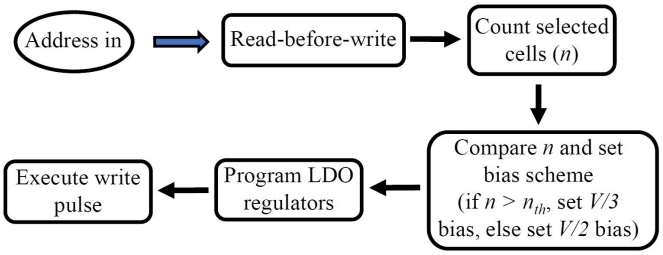

Fig. 6: The write process of a crossbar array in the proposed intelligent write scheme.

A. Optimal Choice of Bias Scheme

The bias scheme of a crossbar array is altered when the number of selected cells n crosses a threshold, n_{th}. Since the energy of the $V/2$ bias scheme grows with increasing n, if $n < n_{th}$, the power delivery system switches to the $V/2$ bias scheme. If $n > n_{th}$, the system switches to the $V/3$ bias scheme. The savings in energy in terms of the number of selected cells n is illustrated in Fig. 7.

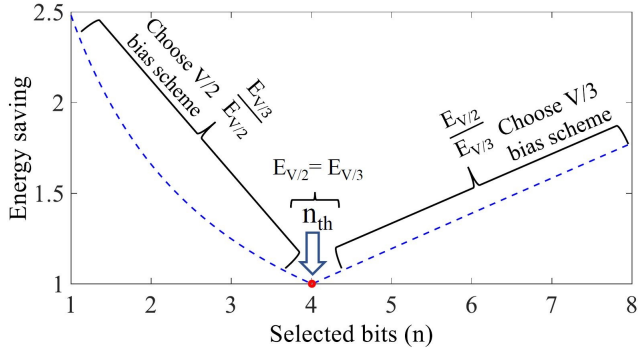

Fig. 7: Energy improvement in terms of the number of selected cells, assuming $N = 128$, $K_{V/2} = 20$, and $K_{V/3} = 345$.

Note that the $V/2$ bias scheme provides as much as 2.5x energy improvement for a 128 x 128 array when a single bit is selected if n_{th} is four. The $V/3$ bias scheme provides up to a 1.8x savings in energy when eight bits are selected. While the energy improvement for the $V/3$ bias scheme increases for large n, the maximum number of selected cells is limited by IR drops due to the parasitic interconnect resistance. By setting the energy for both bias schemes ((1) and (2)) equal, the number of bits in which both bias schemes consume the same energy n_{th} is

$$n_{th} = \frac{2N^2 - 3K_r N}{3K_r N - 6K_r + 2}, \tag{6}$$

where K_r is the ratio of the nonlinearity factors,

$$K_r = \frac{K_{V/3}}{K_{V/2}}. \tag{7}$$

Note that n_{th} is a function of K_r and array size N.

B. Overhead and Challenges

The proposed write scheme can provide significant energy savings (as high as 2.5x) as compared to a conventional system with a single bias scheme. The write process however incurs additional steps as compared to a conventional write operation that utilizes a constant bias scheme (see Fig. 6), thereby increasing the write latency. The write latency is typically determined by the switching time of the 1S1R cell which increases due to the time to program the LDOs. In the proposed write scheme, the read-before-write operation that necessitates a read operation for every write operation, and the time required to compute and compare n with respect to n_{th} have to be considered in addition to the switching time of the 1S1R cell. In memory systems, the read operation is typically a primary performance bottleneck. If however the write latency increases significantly, the write operation can inhibit memory performance. Thus, a fast power delivery system is required for time constrained memory applications such as DRAM and cache memory. For slower memory systems such as flash, the stringent timing requirements can be relaxed. While the read latency is significantly smaller than the write latency [3] and can be as low as five nanoseconds [4], the time required to program an LDO has to be within a few nanoseconds to prevent write dependent performance limitations.

The energy overhead of the intelligent write scheme is insignificant. The write operation for a 1S1R crossbar array is typically on the order of hundreds of nanojoules [3]. The read operation during the read-before-write requires negligible energy, typically less than one nanojoule since the read latency is significantly less than the write latency. The programmable CMOS reference voltage consumes a few picojoules [15], assuming a switching time on the order of hundreds of nanoseconds. The primary challenge for the intelligent write scheme is therefore the increased write latency in time constrained memory applications.

IV. Conclusions

The write energy of a crossbar array is orders of magnitude greater than the read energy and is a large portion of the total energy consumed by a memory system. To improve the energy efficiency during write operations, an intelligent write scheme is proposed. The system provides a hybrid bias scheme to exploit both the $V/2$ and $V/3$ bias schemes to enhance energy efficiency. While the $V/2$ bias scheme provides better energy efficiency for a small number of selected cells, as the number of selected cells increases, the $V/3$ bias scheme provides greater energy efficiency. The number of selected cells for equal energy consumption for both bias schemes (n_{th}) is described. For a specific number of selected bits, the proposed intelligent write scheme considers the most energy efficient bias scheme. The energy improvements provided by the intelligent write scheme can be as high as 2.5x. Due to the multiple steps required for a write operation, the write latency however increases. To effectively exploit this proposed intelligent write scheme in time constrained memory systems, the response time of the LDOs and the time to compute n_{th} need to be on the order of a few nanoseconds. The intelligent write scheme itself incurs negligible energy overhead.

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