Behavioral Verilog-A Model of Superconductor-Ferromagnetic Transistor

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***Abstract*—The superconductor-ferromagnetic transistor (SFT) is a novel cryogenic device with the potential to greatly enhance traditional single flux quantum (SFQ) circuits. Since SFT devices are under active development, compact models are necessary to evaluate this device in novel circuits. In this paper, a simplified compact model of a three terminal SFT device is proposed. The model fits the general I-V characteristics of existing devices with 7.4% mean absolute error, while also capturing the transient behavior of the device. The model has been implemented in Verilog-A and simulated in Cadence Spectre. The proposed model enables the simulation of SFQ circuits containing SFT devices, and is reconfigurable to support developments in SFT technology.**

I. Introduction

Superconducting digital electronics is one of the more extensively studied non-silicon computing technologies, which has recently gained considerable research interest as a promising solution for exascale computing [1], [2]. Rapid single flux quantum (RSFQ) technology [3] and related energy efficient modifications [4], [5] are capable of lowering power consumption by three orders of magnitude [6]. Recently developed circuits with a complexity of over 11,000 Josephson junctions in a microprocessor operating at 18 GHz have been demonstrated [7].

Despite recent developments in SFQ technology, one major drawback is the lack of a fast and dense memory. An unusual characteristic of SFQ technology is the absence of a three terminal device providing good input-output isolation and controllable switching behavior. SFQ circuits are composed of two terminal Josephson junctions (JJ). The introduction of a three terminal device would enhance circuit flexibility and support the development of novel circuits, particularly for memory applications.

One recently introduced family of superconductive devices is the superconductor-ferromagnetic transistor (SFT) [8], [9]. These devices consist of a stack of superconductor, ferromagnetic, and insulator layers where the topologies and properties depend upon the arrangement of the layers within the stack and the number of terminals. In three terminal SFT, the critical current between the acceptor terminals is controlled by the current supplied to the injector terminal.

To enable circuits using this novel SFT device, a closed-form model of this device is necessary [10]. The theory of the device operation is described in [11], where the expressions characterizing the operation are far too complex for circuit simulation. A simplified Verilog-A model for a three terminal SFT device is therefore presented here.

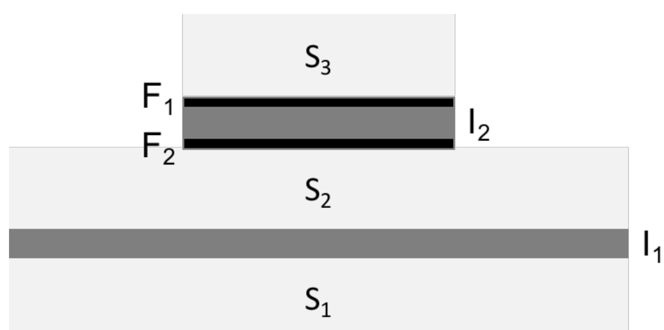

Fig. 1: Structure of a three terminal SFT device. The superconductor layers are marked as $S_{1,2,3}$, ferromagnetic layers as $F_{1,2}$, and insulator layers as $I_{1,2}$.

The three terminal SFT device considered in this paper is shown in Figure 1. This device consists of two junctions stacked above each other. The acceptor junction consists of an insulating layer (I) sandwiched between two superconductor layers (S), forming an SIS

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structure. The injector junction consists of an insulating layer between two ferromagnetic layers (F) and two superconductor layers, forming an $SFIFS$ structure. Both junctions share a superconducting layer, forming an $SFIFSIS$ device, where an SIS acceptor is stacked on top of an $SFIFS$ injector. In section II, the compact model of the $SFIFSIS$ device is described. In section III, the model is verified against experimental data. In section IV, some conclusions are offered.

II. Compact Model of the SFT Device

The compact model of an SFT device is described in this section. In subsection A, the operation of a three terminal SFT device is presented, and an equivalent electrical circuit is proposed. In subsection B, expressions describing the critical current and superconducting energy gap are discussed and a simplified closed-form expression is described. In subsection C, approximations of the gain and threshold voltage are presented. In subsection D, the reactive parameters of the device are discussed.

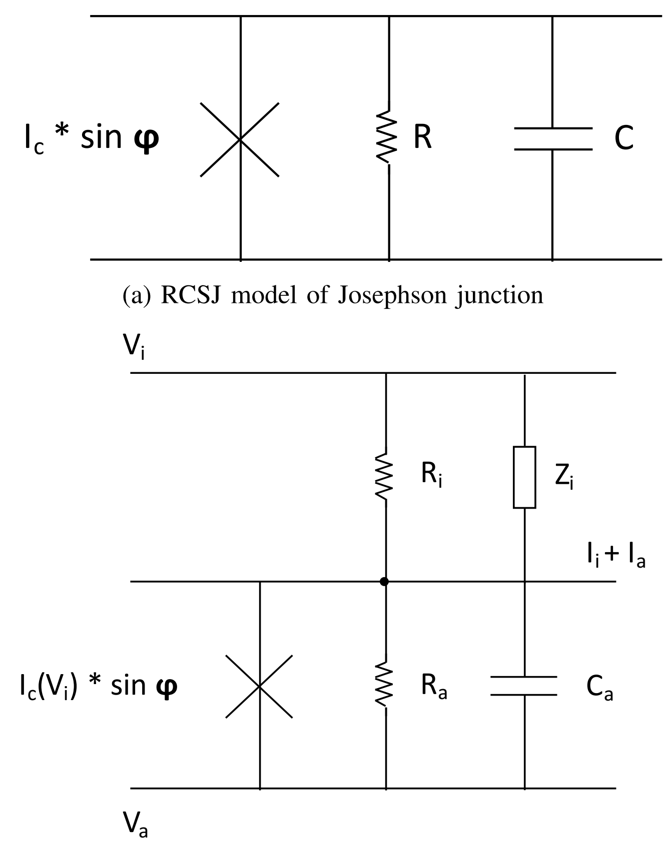
A. SFT device operation

Operation of the SFT device is similar to previously proposed superconductor multilayered stacks, such as a quiteron [12], consisting of an $SISIS$ multilayer. In an $SISIS$ device, when one SIS junction is biased, excess quasiparticles are injected into the shared superconductive middle layer, suppressing superconductivity in this layer, thereby changing the properties of the second SIS junction. One important distinction, however, is the presence of ferromagnetic layers within the stack. These layers suppress Josephson current through one of the two junctions, making the device asymmetric, and introducing input-output isolation [11].

In a three terminal SFT, the current in the $SFIFS$ injector I_i introduces excess quasiparticles in the middle S_2 layer shared between the acceptor and injector, as well as the S_1 layer. This effect suppresses the superconductor energy gap $\Delta_{1,2}$ in both the S_1 and S_2 layers and reduces the critical current I_c of the acceptor SIS junction. Current controlled modulation of the critical current, along with good input-output isolation, are the primary advantages of SFT devices as compared to previous structures. The available experimental data describing the $SFIFS$ injector, such as the linear I-V characteristics of the stack, suggest that the injector current I_i does not exhibit Josephson behavior due to the presence of the exchange field in ferromagnetic layers [11], [13].

The SIS acceptor with a shared S_2 layer generally exhibits properties similar to regular SIS devices, such as a Josephson junction. A Josephson junction is commonly characterized by a resistively and capacitively shunted junction (RCSJ) model [14]. In this model, a junction is represented by an ideal Josephson element connected in parallel with a resistor and capacitor. The equivalent circuit for this model is shown in Figure 2(a).

In a model of an SFT device, the existing RCSJ JJ model should consider the novel behavior caused by the injector stack. The $SFIFS$ injector exhibits a linear current-voltage characteristic and is therefore represented as a resistor. The equivalent circuit of a three terminal SFT device is shown in Figure 2(b).



(a) RCSJ model of Josephson junction

(b) Model of an SFT device

Fig. 2: Equivalent electrical circuit, a) JJ, and b) SFT

B. Critical current and suppression of superconducting energy gap

An expression for the dependence of the critical current on the injector voltage is described in [11]. The integral equations constituting this solution are solved numerically, and are therefore not incorporated into a

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closed-form, computationally efficient expression suitable for circuit simulation.

Critical current suppression in this device is caused by suppression of the superconductive energy gap, which depends upon the injector current, and, consequently, the injector voltage. The energy gap is abruptly suppressed when the voltage reaches a threshold voltage V_{th}.

A graph of this dependence resembles a bell function (1),

$$f = \frac{1}{1 + |\frac{x-c}{b}|^{2a}}, \tag{1}$$

where b is the threshold voltage. The slope of the $\Delta(I_i)$ dependence determines the gain G of the device. Therefore, $2a$ in (1), which determines the slope of the curve, is equal to G.

While the critical current of the device also weakly depends on other parameters, the general shape of the $I_c(I_i)$ curve is due to the shape of the $\Delta(I_i)$ dependence. A simplified closed-form expression of the $I_c(I_i)$ dependence is

$$I_c = \frac{\kappa}{1 + |\frac{V_i}{V_{th}}|^{G}}, \tag{2}$$

where κ is a fitting parameter.

C. Gain and threshold voltage model

One primary parameter characterizing a three terminal SFT device is the ratio of the injector resistance $R_{T(i)}$ and acceptor resistance $R_{T(a)}$ This $\frac{R_{T(i)}}{R_{T(a)}}$ ratio affects both the threshold voltage V_{th} and the gain G of the SFT device.

Both $V_{th}(\frac{R_{T(i)}}{R_{T(a)}})$ and $G(\frac{R_{T(i)}}{R_{T(a)}})$ are numerically characterized in [11]. To provide a closed-form model, however, the dependence is assumed to be approximately linear between the ratio of 1 and 15, gradually changing from 1 to 4.5 mV. The gain of the device also varies linearly, increasing for larger resistance ratios.

Both of these dependences are incorporated within the model. However, as SFT devices are currently immature, the model can be adjusted manually, allowing the estimated gain and threshold voltage to be based on experimental data.

D. Reactive parameters of the injector

As the injector of the device is a complex stack of metal layers, ferromagnetic layers, and an insulating layer, the behavior of the injector is not completely resistive. With the DC-biased injector stack, the acceptor behaves as a current controlled Josephson junction. Capacitive and inductive effects in the injector affect the electrical properties of the device, particularly during transient switching. The injector impedance Z_i is included in the equivalent circuit shown in Figure 1. The capacitance and inductance of the injector is based on the device geometry, and can be estimated or measured experimentally.

III. Model Verification

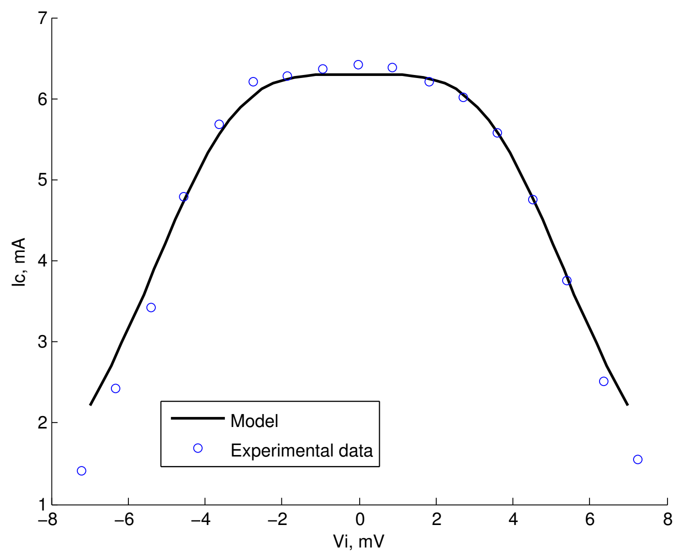

Fig. 3: $I_c - V_i$ characteristic of the proposed model. The experimental data are shown as circles.

The proposed model has been implemented in Verilog-A by modifying the existing RCSJ Verilog-A model of a Josephson junction [14]. The model has been evaluated within the Cadence Spectre simulator. The I-V characteristics resulting from a DC analysis are shown in Figure 3. The model is compared to the experimental data reported in [11].

From the DC analysis, the model accurately captures the behavior of the device. The input parameters of the proposed model are the device geometries, gain, threshold voltage, and maximum critical current. The gain and threshold voltage are estimated by the model, or manually adjusted based on available experimentally measured parameters. The simulation accurately describes the I-V characteristics of existing devices [8], [11], [15] with a mean absolute error of 7.4%.

To date, no experimental transient measurements of SFT devices exist in the literature. The transient simulations have therefore not been compared to experimental data. This model, however, can be compared to the

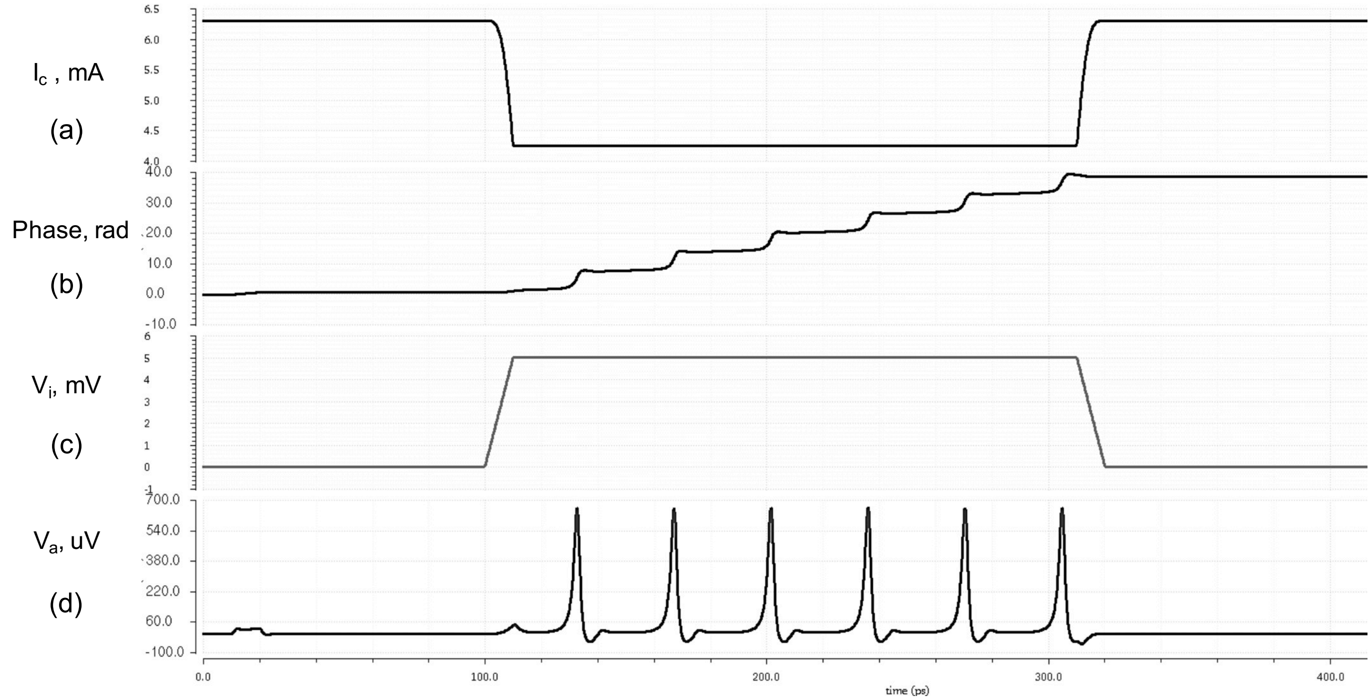

Fig. 4: Transient response of an SFT device based on the proposed model, a) critical current of the acceptor, b) phase of the acceptor, c) injector voltage, and d) acceptor voltage.

expected behavior of a current controlled Josephson junction. This simulation is depicted in Figure 4.

In this transient simulation, the acceptor junction of the model is connected to the bias current source and biased at $I_b = 0.7 \cdot I_c$. This current is insufficient to switch the acceptor junction into a resistive state. The injector current I_i, initially zero, gradually increases to 1.4 mA, corresponding to an injector voltage of 5 mV. After the injector voltage is applied, the acceptor junction continuously switches, generating a series of SFQ pulses. This switching behavior is due to suppression of the acceptor critical current to approximately 66% of the original critical current. After the injector voltage is reduced, the acceptor critical current is restored to the current level without injection, terminating the switching process (see Fig. 4d). This simulation accurately describes the expected transient behavior of the device and confirms the utility of the proposed SFT model to the SFQ circuit design and analysis process.

IV. Conclusions

A simplified closed-form model of a three terminal SFT device is described and implemented in Verilog-A. While the proposed model does not include all possible superconductor-ferromagnetic multilayer interactions and proximity effects, the accuracy of the model is sufficient for the SFQ circuit design process, and can be adapted to support device modifications. The SFT model can be used to evaluate prospective SFT-based superconductive digital circuits and memory arrays, and requires low computational overhead, comparable to the standard RCSJ model of a Josephson junction.

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