Multi-Bit CNT TSV for 3-D ICs

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***Abstract*—Through substrate vias (TSVs) are a seminal component of three-dimensional (3-D) integrated circuits (ICs). Each TSV typically carries a single signal between two adjacent layers of a 3-D structure. A multi-bit carbon nanotube TSV is proposed in this paper to increase the number of I/Os among layers within 3-D ICs. The proposed multi-bit TSV can propagate multiple independent signals due to the high anisotropy of the carbon nanotubes. The electrical properties of each bit within a two-bit TSV and the electrical interactions between the bits are compared to a theory-based electrical model, exhibiting high accuracy. The passive elements deviate by up to 4%, and the S-parameters of the system deviate by up to 1.5% from numerical analysis. Capacitive coupling and leakage current between the bits of the two-bit TSV model have also been evaluated. The structure exhibits negligible noise coupling (less than 1%) and a peak leakage current of 631.7 µA.**

***Index Terms*—3-D IC, carbon nanotube, through substrate via, interconnent.**

I. Introduction

Through substrate vias (TSVs) are an integral element of three-dimensional (3-D) integrated circuits (ICs) [1], [2]. Individually fabricated dies using optimal process technologies for the intended function are vertically aligned and stacked to form a single 3-D structure. The TSVs connect the layers within the 3-D structure and enable signaling and power delivery. TSVs, however, are relatively large, occupying significantly greater area than on-chip vias. Moreover, the number of TSVs within any of the substrates is limited by the difference between the coefficients of thermal expansion of the TSV fill material and the substrate. To prevent cracking of the substrate, these thermal stresses limit the area occupied by the TSVs within typical substrate materials (e.g., silicon) to approximately 2% of the substrate area [3]. Addressing I/O limitations between layers within a 3-D structure is therefore a primary concern [4].

Carbon nanotubes (CNTs) are a strong candidate to replace copper (Cu) and tungsten (W) as the fill material for TSVs [5]. The resistance per micrometer of the CNT bundles (for TSV applications) in the direction of conduction is approximately 2.5 times lower than Cu [6]. In contrast, the resistance between adjacent CNTs within the bundle is on the order of megaohms [7]. This anisotropy property of CNT bundles is exploited here to enable multi-bit TSVs, *i.e.*, TSVs that carry multiple independent signals. This functionality is achieved by connecting groups of CNTs to separate pads at the top and bottom of the TSV. A two-bit TSV is illustrated in Figure 1.

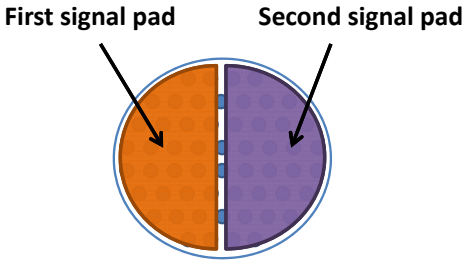

Fig. 1: Top view of a two-bit CNT TSV. Each half of the TSV is connected to an individual signal pad.

The proposed two-bit TSV structure doubles the I/O count between layers and does not occupy additional on-chip area. Alternatively, fewer multi-bit TSVs are required to satisfy a specific inter-layer I/O requirement. The electrical characteristics of the proposed structure are verified using COMSOL Multiphysics [8].

The rest of the paper is composed of the following sections. The electrical characteristics of multi-bit CNT TSVs are discussed in Section II. Electrical evaluation of a two-bit structure is described in Section III. An electrical model of a two-bit CNT TSV is proposed and compared to numerical analysis in Section IV. Issues related to fabrication of the proposed structure is discussed in Section V. Some conclusions are offered in Section VI.

II. Electrical Characterization of Multi-Bit TSVs

The electrical characteristics of multi-bit TSVs are determined from the properties of CNT bundles (arrays of CNTs fabricated as the fill material of TSVs). The vertical and

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horizontal conductivity of a multi-bit CNT TSV is described in Subsection II-A. The coupling capacitance between the individual bits is described in Subsection II-B.

A. Conductivity of multi-bit TSVs

From [9], the resistance of a CNT bundle in the direction of conduction (*i.e.*, vertical direction) is

$$R_{TSV} = \frac{R_{CNT}}{N_{CNT} \cdot F_m} \quad , \tag{1}$$

where R_{CNT} is the resistance of a single CNT, N_{CNT} is the number of CNTs within a bundle, and F_m is the metallic fraction of the CNT bundle (the effective number of conducting CNTs within the bundle). The number of CNTs within a bundle assumes a two-dimensional triangular packing structure [10],

$$N_{CNT} = \frac{2\pi r_{TSV}^2}{\sqrt{3}(d_{CNT} + \delta)^2} \quad , \tag{2}$$

where r_{TSV} is the radius of the TSV, d_{CNT} is the diameter of the CNTs, and δ is the minimum van der Waals inter-tube spacing [11], [12].

The resistance of a single CNT is

$$R_{CNT} = R_Q + R_S \quad , \tag{3}$$

where

$$R_Q = \frac{h}{2q^2} \tag{4}$$

is the quantum resistance, and

$$R_S = \frac{h \cdot h_{TSV}}{2q^2\lambda} \tag{5}$$

is the ballistic resistance. h is the Planck constant, h_{TSV} is the height of the TSV, q is the electron charge, and λ is the mean free path of electrons within the CNTs. Substituting (2) and (3) into (1) yields

$$R_{TSV} = \frac{\frac{\hbar}{4q^2} + \frac{\hbar \cdot h_{TSV}}{4q^2\lambda}}{\frac{2\pi r_{TSV}^2}{\sqrt{3}(d_{CNT}+\delta)^2} \cdot F_m} \quad . \tag{6}$$

To evaluate the resistance of a CNT TSV using a finite element method (FEM), the vertical and horizontal conductivities are treated as electrical parameters of a homogeneous anisotropic material within a TSV structure. From the classical resistance model ($R = \frac{1}{\sigma} \cdot \frac{l}{A}$), the vertical conductivity is

$$\sigma_{vertical} = \left(\frac{R_{TSV} \cdot \pi r_{TSV}^2}{h_{TSV}} \right)^{-1} \quad . \tag{7}$$

The horizontal conductivity of a CNT (the conduction between adjacent CNTs) has not been widely researched, nevertheless, the conductivity of CNT alumina composites has been demonstrated to be seven orders of magnitude lower than the vertical conductivity [13]. The horizontal conductivity is therefore

$$\sigma_{horizontal} = 10^{-7} \cdot \sigma_{vertical} \quad . \tag{8}$$

By dividing the TSV into multiple independent signals, the resistance of each part of the TSV increases since fewer CNTs are used to conduct that signal. The resistance of each bit is

$$R_{bit} = R_{TSV} \cdot N_{bits} \quad , \tag{9}$$

where N_{bits} is the number of independent signals propagating within the multi-bit TSV. The resistance between any two bits within the multi-bit TSV is based on (8),

$$R_{inter\_bit} = \frac{1}{\sigma_{horizontal}} \cdot \frac{w_s}{2 \cdot r_{TSV} \cdot h_{TSV}} \cdot N_{bits} \quad , \tag{10}$$

where w_s is the width of the separation between the bits within a TSV.

B. Capacitance of multi-bit TSVs

The capacitance between any two bits of a multi-bit TSV can be approximated by an expression for the parallel plate capacitance. The dielectric between the two bits of the TSV is formed by the anisotropy of the CNTs. The distance d between the plates is the width of the separation w_s. The area of the plates is the separation between the bits. The capacitance between the two bits is

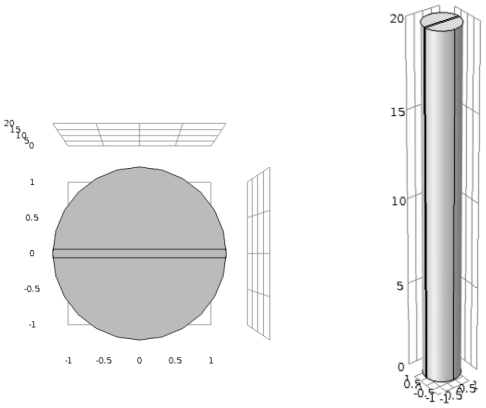
$$C_{inter\_bit} = \frac{\epsilon\epsilon_0 \cdot A}{d} = \frac{\epsilon\epsilon_0 \cdot 2 \cdot r_{TSV} \cdot h_{TSV} \cdot \frac{N_{bits}}{2}}{w_s} \quad , \tag{11}$$

where ϵ and ϵ_0 are, respectively, the relative and vacuum permittivity of the material. C_{inter_bit} is numerically validated in Section III.

III. Evaluation of Two-Bit CNT TSV

The electrical characteristics of a two-bit TSV (depicted in Figure 2) are evaluated in COMSOL Multiphysics [8]. The conductivity of the fill material of the TSV (CNT alumina composite) is determined from (7) and (8). The relative permittivity of the fill material is $\epsilon_0 = 4$ [14].

The test structure of a two-bit CNT TSV is illustrated in Figure 3. The structure is used to determine the electrical properties of each part of the CNT TSV in both the vertical and



(a) (b)

Fig. 2: Two-bit CNT TSV, (a) top view, and (b) 3-D view. All dimensions are in micrometers.

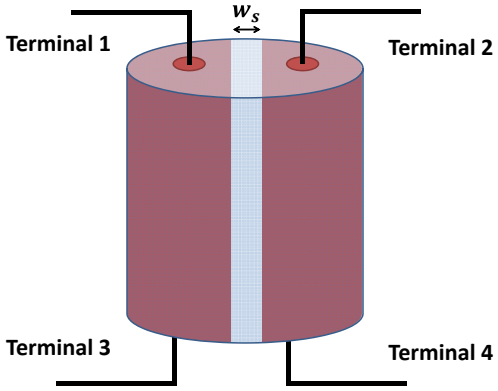


Fig. 3: Test structure for the electrical evaluation of a two-bit TSV.

TABLE I: Electrical and physical parameters for evaluating the multi-bit structure.

Parameter	Value
h_{TSV}	20 µm
r_{TSV}	1 µm
h	$1.054{\cdot}10^{-34}$ J·s
λ	1 µm
q	$1.6{\cdot}10^{-19}$ C
d_{CNT}	1 nm
δ	0.34 nm
F_m	$\frac{1}{3}$
w_s	100 nm
ϵ_0	4

horizontal directions. The electrical and physical parameters used in the numerical evaluation of the two-bit CNT TSV are listed in Table I.

TABLE II: Resistance of each terminal pair of the two-bit CNT TSV.

Terminal pairs	Numerically evaluated resistance [Ω]
T1 - T2, T3 - T4	1,586.4
T1 - T3, T2 - T4	0.84
T1 - T4, T2 - T3	1,586.6

The numerically evaluated resistance between each terminal pair within the two-bit TSV is listed in Table II. The structure is symmetric. The resistance between a symmetric pair of terminals is therefore the same. The ratio of the vertical and horizontal resistance is approximately 1,889. Validation of the effective isolation of the signals propagating within each bit of the TSV is described in Section IV. The vertical resistance between terminals T1 and T3 (second row in Table II) corresponds to R_{bit}.

The horizontal resistance between the two bits within the TSV (corresponding to R_{inter_bit}) is independent of whether the resistance is measured between terminals T1 and T2 (first row in Table II), or T1 and T4 (third row in Table II). This

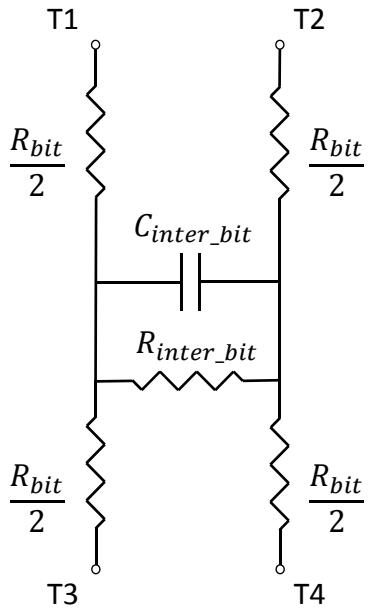


Fig. 4: Electrical model of a two-bit TSV.

characteristic is due to the high ratio of the horizontal and vertical resistance.

The capacitance between the two bits of the TSV C_{inter_bit} is also evaluated in COMSOL. The capacitance is 14.16 fF, the same order of magnitude as the coupling capacitance of a standard single-bit TSV with the surrounding substrate [15].

IV. Electrical Model of a Two-bit TSV

An electrical model of a two-bit TSV is depicted in Figure 4. The passive elements are determined from (9), (10), and (11). Given the parameters listed in Table I, the magnitude of the passive elements in the two-bit TSV model are: $R_{bit} = 0.806\ \Omega$, $R_{inter\_bit} = 1,582.3\ \Omega$, and $C_{inter\_bit} = 14.17$ fF. The worst case difference between the theoretical and COMSOL passive elements is 4%, 0.3%, and 0.07% for, respectively, R_{bit}, R_{inter_bit}, and C_{inter_bit}.

The S-parameters of the electrical model are extracted from SPICE and compared to the S-parameters of the physical two-bit TSV structure in COMSOL, as shown in Figure 5. The worst case difference between the numerical and SPICE evaluations for all S-parameters is 1.5%.

The model depicted in Figure 4 is also evaluated for capacitive coupling and leakage current between the two bits of the TSV. A ramp input voltage is applied to the first bit at terminal 1. The second bit (between terminals 2 and 4) is assumed to be either static, *i.e.*, logic '0' (0 volts) or '1' (1 volt), or transitioning between '0' and '1' in either direction. Note that the capacitance between the bits changes according to the relative direction of transition of the bits [16]. For a static victim, the capacitance between the bits is C_{inter_bit}. For transition of the victim and aggressor in the same direction, the capacitance between the bits is zero. For transition of the victim and aggressor in the opposite direction, the capacitance between the bits is approximately $2 \cdot C_{inter\_bit}$. The peak

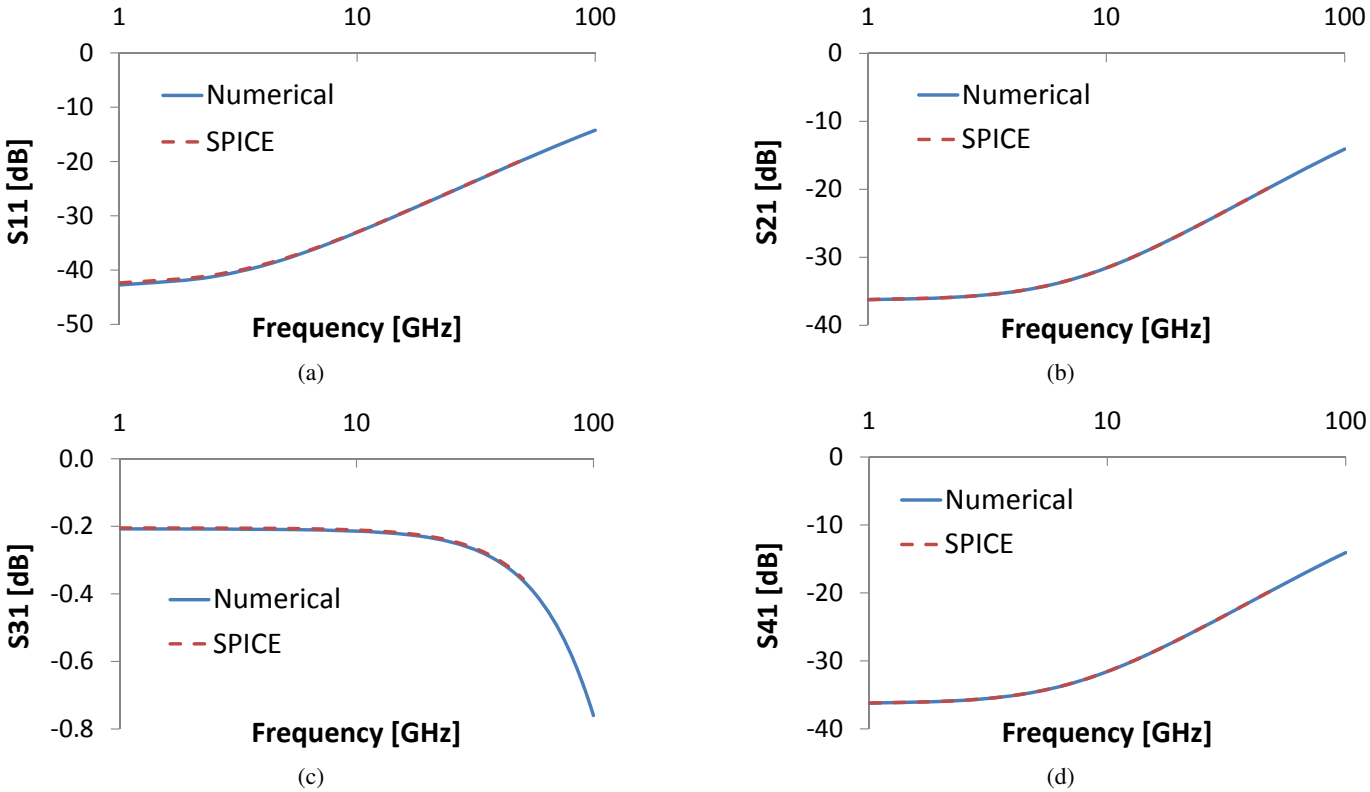


Fig. 5: Comparison of S-parameters of the two-bit TSV from COMSOL and SPICE. (a) S11, (b) S21, (c) S31, and (d) S41.

TABLE III: Capacitive coupling and leakage current at the victim bit, assuming a transient voltage ramp from 0 to 1 volt with a rise time of 10 ps at terminal 1.

Logic state of victim	Peak voltage [mV]	Leakage current [μA]
0	0.82	631.7
1	0.82	0
0 to 1	0.25	0
1 to 0	1.39	631.7

noise voltage and leakage current at the victim (second bit) for different logic states are listed in Table III. The leakage current is determined after the system reaches steady state. The two-bit TSV model exhibits low leakage current (631.7 μA) between the bits when the bits settle on opposite logic states. When both bits of the TSV settle on the same logic state, no leakage current is observed. The capacitive coupling between the two bits is practically negligible (5.43 mV). The worst case noise coupling is under 1% of the full swing of the voltage transition in the case when the aggressor and victim bits transition in opposite directions (row four in Table III).

V. Fabrication Issues of Multi-bit CNT TSVs

A primary concern in multi-bit TSVs is fabrication of the individual pads for each of the independent signals within the TSV. The connections to each bit are realized using metal pads and μ-bumps at each end of the TSV. Dividing the TSV into multiple bits reduces the area to connect to each bit, however, technological advancement leads to reductions in the size of the μ-bumps. Alternatively, other integration technologies, such as thermal compression bonding can be utilized to reduce the contact area of the metals [17].

Another issue related to fabrication is the relatively high contact resistance between the CNTs and metal interconnect. Recent work however, indicates the possibility of integrating graphite as a horizontal on-chip interconnect to replace copper. Graphite and CNTs are both covalently bonded carbon based materials. This integrated technology should simplify the connection process of independent bits within a multi-bit TSV.

VI. Conclusions

A multi-bit CNT TSV is proposed in this paper. Each TSV can carry multiple independent signals, significantly increasing the number of I/Os within 3-D ICs. A two-bit TSV is numerically evaluated and both passive elements and S-parameters are extracted. In addition, an electrical model is evaluated in SPICE, and exhibits high accuracy as compared to the numerical model. The magnitude of the passive elements is within 4% error, and the S-parameters are within 1.5% error.

The proposed electrical model of the two-bit TSV is also evaluated for capacitive coupling and leakage current between the two signals. The worst case coupling noise is less than 1% of the full voltage swing of the victim signal, and the peak leakage current is 631.7 μA. The proposed electrical model is highly scalable and can be extended to multi-bit TSVs with more than two bits.

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