Cryogenic Dynamic Logic

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***Abstract*—Cloud computing is increasing the demand for large scale, energy efficient, and fast computing systems. One circuit technique satisfying these goals is dynamic logic. Furthermore, since portability is not required for cloud computing centers, these systems can support cryogenic operation. Cryogenic dynamic circuits eliminate the seminal issue of these circuits, loss of logic state due to leakage currents. The operation of dynamic CMOS circuits operating at cryogenic temperatures is discussed in this paper. For a 160 nm MOSFET technology, dynamic logic at room temperature can operate as low as 180 kHz. The same circuit in a cryogenic temperature can operate at DC. The state in a dynamic logic circuit operating at cryogenic temperatures is shown to remain indefinitely. This property makes low frequency testing of dynamic logic more feasible, supporting the development of complex VLSI circuits targeting high frequency applications such as cloud computing.**

***Index Terms*—Cryogenics, LHT, CMOS, MOSFET, dynamic logic**

I. Introduction

Cloud computing requires high performance, energy efficient processors and can support cryogenic operation since portability is not desired. Higher frequency circuits, required in cloud computing systems, can utilize dynamic logic circuits for improved performance. As compared to static logic circuits, dynamic circuits are faster, more power efficient, and utilize less area. Despite these benefits, room temperature dynamic logic circuits cannot operate at low frequencies and are highly sensitive to noise. Dynamic circuits operating at room temperature provide a valid output only during short periods of time since the state is temporarily stored on a capacitor. This drawback makes building complex dynamic circuits challenging, since low frequency test of these circuits is a difficult task. Dynamic circuits operating at cryogenic temperatures bypass these issues [1].

Significant improvements in performance can be achieved by cooling the environment [2]. Cryogenic electronics play an important role in meteorology, quantum computing, high energy physics, and space technologies. Furthermore, applications which require a high signal-to-noise ratio and/or receive weak input signals benefit when the circuits operate at cryogenic temperatures [3]. Cryogenic environments also avoid thermal runaway in semiconductors [4].

In this paper, dynamic CMOS logic circuits operating at liquid helium temperatures (LHT), specifically 4.2 K, are evaluated. The performance of dynamic logic in a cryogenic environment is compared to room temperature (RT) operation. The primary advantage is dynamic logic at LHT can operate at DC unlike RT operation, supporting low frequency testing of complex dynamic circuits that target high frequency applications.

The paper is organized as follows: static and dynamic logic circuits and insight into MOSFET operation at cryogenic temperatures are described in Section II. The cryogenic behavior of a MOSFET and a related HSpice model are discussed in Section III. A dynamic circuit is characterized at 300 K and 4.2 K operation in Section IV. Some conclusions are drawn in Section V.

II. Background

The latest high complexity digital circuits primarily deploy static logic circuits. These circuits can be enhanced to use dynamic circuits if operated at cryogenic temperatures. Differences between static and dynamic logic circuits are described in subsection II-A. The behavior and advantages of dynamic circuits operating at LHT are discussed in subsection II-B, and the behavior of a MOSFET operating at cryogenic environments is reviewed in subsection II-C.

A. Static and dynamic logic circuits

Many types of MOSFET logic circuits have been developed since the 1970's. These circuits fall into two primary groups, static logic circuits and dynamic logic circuits.

Logic circuits are combinatorial in nature and without memory. To reduce power consumption, static logic circuits can operate at lower frequencies or placed into a standby mode [1]. An example of a static logic circuit (a D flip flop) is shown in Fig. 1. In this master-slave flip flop, the state is maintained at the master stage output, and is transferred upon arrival of the next clock cycle to the slave stage.

Dynamic logic circuits, alternatively, depend upon the temporary storage of information. Gate and stray capacitances store the charge in these circuits, maintaining the logic state. Dynamic circuits require a periodic refresh since the charge decays over time. In dynamic circuits, the logic and memory elements are the same circuit, and the charge is transferred between capacitors. This signal flow between capacitors is controlled by an external signal. An example of a dynamic logic circuit, specifically, a dynamic shift register, is shown in Fig. 2. The output and input of each stage of a shift register

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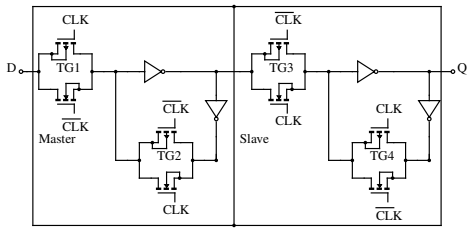


Fig. 1: Master-slave D flip flop as an example of a static logic circuit. Each state can be maintained indefinitely regardless of the clock frequency as long as power is maintained.

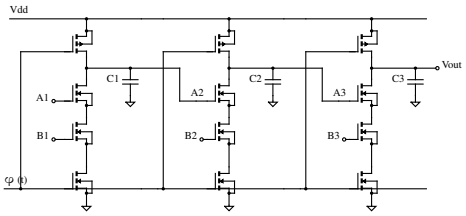


Fig. 2: Dynamic shift register. At low frequencies, the output degrades due to leakage currents.

are connected to each other. At each transition of the clock signal, a bit of information is shifted by one position, passing in the input data and passing out the output data.

Dynamic logic requires less area and consumes less power than static circuits. Furthermore, dynamic circuits can operate at higher clock frequencies. These circuits, however, exhibit some undesirable characteristics. Dynamic logic circuits cannot operate at low frequencies due to the leakage of charge on the capacitors and exhibit lower noise immunity. These issues cause another problem: the testability of a dynamic circuit is poor. Since it is not possible to maintain a logical state at DC in RT dynamic logic circuits, it is difficult to statically test a circuit and/or probe individual nodes [5].

B. Dynamic logic

A dynamic logic circuit is shown in Fig. 3. The capacitive load C_{out} maintains the output voltage V_{out}. The NMOS logic network behaves as a composite switch. As previously noted, V_{out} can decay within a short time due to leakage currents.

The clock signal $\varphi(t)$ controls the operation of the circuit, where the data flow from one stage to another stage across a cascaded network. The clock signal alternates between logic 0 and 1, described as the precharge and evaluate phases of the network. The precharge occurs at $\varphi = 0$. The PMOS transistor is active and the NMOS transistor is cutoff; as a result, the output charges to V_{dd}. Although the output node is always charged to V_{dd}, the output does not always remain at logic 1. Rather, this phase pre-conditions the output, *i.e.*, the output node is charged to V_{dd} regardless of the input signals, preparing the node for the evaluation phase.

Conversely, at $\varphi = V_{dd}$, the NMOS transistor is active and the PMOS transistor is in cutoff during the evaluation process. The logic gate evaluates the inputs based on the signal polarity and establishes the output voltage. Two possible scenarios can

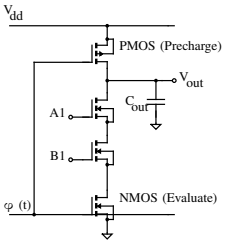


Fig. 3: A dynamic logic circuit.

occur. If the composite logic block forms a closed switch, the output capacitor discharges to ground, resulting in a logic 0 at the output. If, alternatively, the composite logic block is an open circuit, the charge is not discharged to ground, resulting in a logic 1 at the output. This state, however, cannot be maintained indefinitely due to leakage currents discharging the output capacitor. The charge at the output must therefore be read before the voltage drops below the logic 1 noise margin, introducing a temporal limit on the read time. Thus, these types of circuits are dynamic in nature [1].

These disadvantages of dynamic circuits no longer exist when operated at cryogenic temperatures. Since the leakage current at cryogenic temperatures is negligible, the charge on the capacitors does not leak as compared to room temperature operation. This property allows a dynamic circuit to operate at lower frequencies, essentially DC, which reduces the power consumption and supports low frequency testing.

At 4.2 K, a MOSFET exhibits enhanced physical properties such as higher transient currents, negligible leakage currents, and increased subthreshold slope. These properties are discussed in the following subsection.

C. MOSFET characteristics in cryogenic temperatures

Silicon MOSFETs operating at cryogenic temperatures exhibit significant improvements in performance and reliability as compared to operation at room temperatures. Substantial research in cryogenic MOSFET operation occured during the 1980's but has received much less attention since then. The first studies on the behavior of MOSFETs at cold temperatures are described in [6]–[12]. The topic is once again becoming important due to the growing interest in cloud computing, enhancing the need for energy efficient, stationary computing platforms.

The carriers within the substrate of a CMOS transistor start to freeze out at 77 K or below [13]. However, with a voltage applied between the source and drain, the carriers, driven by energy from an electric field, form an inversion layer, becoming conductive. The mobility of the channel increases with a decrease in temperature due to less carrier scattering caused by lattice vibrations, but is limited by coulombic scattering at lower gate voltages and surface roughness at higher gate voltages [14]. As a result, the speed of the MOSFET devices increases as compared to room temperature operation. A MOSFET operating at cryogenic temperatures exhibits the following advantages of 4.2 K behavior as compared to 300

K behavior: negligible leakage currents, higher sub-threshold slope, insignificant electromigration, fewer thermal induced failures such as oxide degradation, higher transconductance, and no latch-up [13].

III. CMOS CHARACTERIZATION AND MODELING AT LHT

The design of high performance circuits requires efficient simulation models. A model of a CMOS transistor operating at cryogenic temperatures is crucial for circuit analysis. The properties of LHT operation and the development of an HSpice model are described, respectively, in subsections III-A and III-B.

A. Properties of CMOS technology at 4.2 K

The MOSFET considered in these simulations is a 160 nm CMOS transistor [15]. The transistor has a width of 2.32 μm and a channel length of 160 nm with a thin oxide. The drain current I_D at 4.2 K is 40% higher than the drain current at room temperature due to the increase in the carrier mobility (μ). As compared to room temperature operation, the threshold voltage increases from 0.55 volts to 0.7 volts and the subthreshold slope (SS) is 3.8 times steeper in LHT than RT, increasing from 87.0 mV/dec to 22.8 mV/dec. The kink effect is observed in thick oxide CMOS at LHT [15]. Since the kink effect is not observed in thin oxides, which is assumed here, the kink effect is not considered. I-V curves for different V_{GS} at room temperature (300 K) and LHT (4.2 K) are shown in Fig. 4 [15].

The SS plays a significant role in leakage current, greatly lowering the leakage current at lower temperatures. The drain current in the subthreshold regime can be modeled [16] as

$$I_{DS} \approx I_S \mathrm{e}^{\frac{q(V_{GS}-V_T)}{nkT}} \left(1 - \mathrm{e}^{-\frac{qV_{DS}}{kT}}\right), \tag{1}$$

where I_S is the saturation current, q is the electron charge, k is the Boltzmann constant, and T is the absolute temperature. The subthreshold slope factor n [15] is

$$n(T) = 1 + \frac{C_{dep}(T)}{C_{ox}}. \tag{2}$$

$C_{dep}(T)$ is the channel and bulk depletion capacitance, while C_{ox} is the gate oxide capacitance.

An expression for the subthreshold slope [15] is

$$SS(T) = \left[\frac{\partial \log I_D}{\partial V_{GS}}\right] = \ln(10)\frac{nkT}{q}. \tag{3}$$

At cryogenic temperatures, however, due to incomplete ionization of the dopants, carrier freeze-out occurs [13]. This effect causes the SS to no longer be proportional to the temperature at LHT.

B. HSPICE model

The Phillips MOS11 HSpice model is used for the 160 nm CMOS transistor [15]. The temperature dependent parameters have been modified to fit the experimental data. The revised parameters are based on [15].

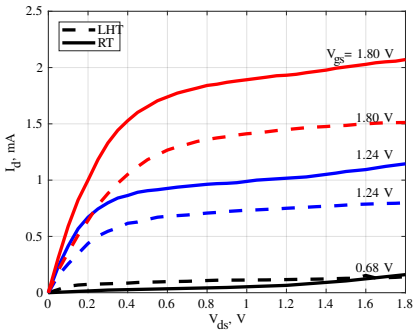


Fig. 4: Experimental $I_D(V_{DS})$ characteristics of 160 nm CMOS for different V_{GS} [15].

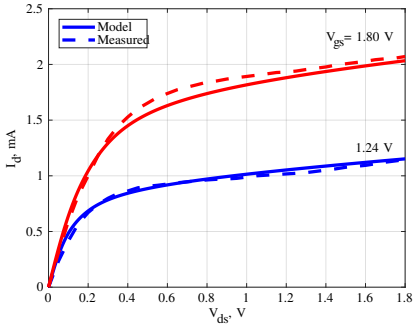


Fig. 5: I_D vs V_{DS} for V_{GS} = 1.24 volts and 1.8 volts for measured and simulated CMOS. An average error below 4% and maximum error below 5% between the model and the experimental data are observed.

To match the properties of the device to a device operating at 4.2 K, parameters such as VFB BETSQ, THESRR, THESATR, SDIBLO, ALPR and KOR are fitted to the LHT data. Certain fitting parameters for the original temperature of the MOS11 model are inaccurate at LHT, and therefore defaulted to zero. The I-V curves exhibit an average error below 4% and a maximum error below 5% for V_{GS} above the threshold voltage. I_D versus V_{DS} for this model and measured data at 4.2 K are shown in Fig. 5.

IV. DYNAMIC CIRCUIT CHARACTERIZATION AND SIMULATION

The behavior of dynamic logic circuits operating at 300 K and 4.2 K is described in this section, and the results are confirmed with HSpice simulations. The circuit is presented in subsection IV-A, and the behavior of this circuit at RT and LHT is described in subsection IV-B. Results of the simulation at room temperature and cryogenic temperature are shown, respectively, in subsections IV-C and IV-D.

A. Dynamic circuit operation

A dynamic CMOS circuit, as shown in Fig. 3, operating at room temperature (300 K) and LHT (4.2 K) is considered here. The circuit consists of four transistors and a 20 fF capacitive load.

In the dynamic logic block, $A1$ is set to 1 and $B1$ is set to 0. During precharge, the voltage across the output is charged to logic 1. However, during the evaluation phase, although the NMOS transistors are on, the output remains at logic 1 since the logic block behaves like an AND gate. Although $A1$ is 1, $B1$ is 0, therefore V_{out} is not connected to ground. The clock signal and output voltage are shown in Fig. 6a, with operation at room temperature and a frequency of 10 MHz. During the evaluation phase, the output voltage degrades due to leakage currents. Since the frequency is sufficiently high, the voltage does not drop below the threshold voltage (which is 0.55 volts at RT, labeled in the figure as logic 1).

B. Dynamic circuit behavior at 300 K and 4.2 K

To develop an expression for the decay time, the subthreshold current described by (1) is equated to the capacitor current,

$$I_S \mathrm{e}^{\frac{-qV_T}{nkT}} \left(1 - \mathrm{e}^{-\frac{qV_{out}}{kT}}\right) = C_{out} \frac{\partial V_{out}}{\partial t}. \tag{4}$$

The decay time t is

$$t = \frac{C_{out} kT}{I_S q} \mathrm{e}^{\frac{qV_T}{nkT}} \ln\left[\mathrm{e}^{\frac{q}{kT}} \left(V_{dd} - V_{out}\right) - 1\right]. \tag{5}$$

The decay time of V_{out} for $V_T = 0.55$ volts and $T = 300$ K is 3.1 μs. The minimum frequency for proper operation at room temperature is 161 kHz.

For cryogenic LHT operation, the charge decay time is significantly longer than the age of the Universe. A dynamic circuit at LHT can therefore operate at DC.

C. Simulation of dynamic logic circuit at 300 K

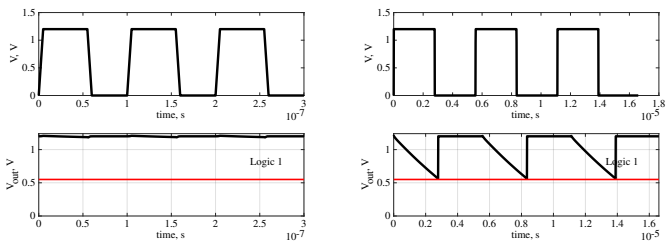
For room temperature operation, the minimum frequency is 180 kHz. The output voltage at this frequency is shown in Fig. 6b. During the evaluation phase, the charge on the output capacitor drops below the threshold voltage; in the next stage, this voltage is no longer at logic 1. Since 180 kHz represents a decay time of 2.78 μs, the difference between the simulation and analytic solution for the decay time is 10%.

If the frequency drops further, the charge completely leaks away before arrival of the next clock pulse when operating at RT. An example of this condition is shown in Fig. 7a, where the frequency is 500 Hz. Note that the charge on the output capacitor completely leaks away during the evaluation phase.

D. Simulation of dynamic logic circuit at 4.2 K

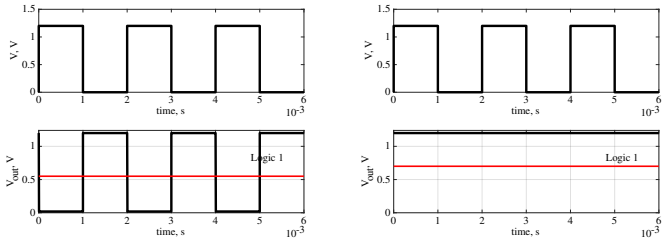
In comparison to the dynamic circuit operating at RT and 500 Hz, the same circuit at LHT exhibits no drop in voltage at 500 Hz, as shown in Fig. 7b. This result agrees with the analytic solution. Note that the frequency can be further reduced, allowing the dynamic circuit at 4.2 K to operate at DC.

The maximum speed and power at room temperature and liquid helium temperature are compared. The highest frequency at RT is 2.5 GHz while dissipating 37.1 nW. The frequency and power consumption of the same circuit at LHT is, respectively, 20 GHz and 7.2 fW, eight times faster and 5x10^6 times less power. These results demonstrate the speed and power advantages of LHT operation.



(a) (b)

Fig. 6: Dynamic circuit at RT operating at (a) 10 MHz, and (b) 180 kHz. 10 MHz operation shows the circuit operating normally, while 180 kHz is the minimum functional frequency.



(a) (b)

Fig. 7: Dynamic circuit operating at 500 Hz in (a) RT, and (b) LHT. The circuit shows an incorrect output at RT, while at LHT the circuit operates properly.

V. Conclusions

Interest in cloud computing systems has been growing, demanding the need for energy efficient, stationary computing platforms. Due to the static nature of these platforms, cloud computing can support cryogenic operation. This characteristic suggests the introduction of dynamic logic operating at cryogenic temperatures to cloud computing centers due to the capability to operate at higher frequencies with lower power consumption. An important drawback of dynamic circuits as compared to static circuits is low frequency test. This testability issue is overcome by operating dynamic circuits at cryogenic temperatures.

Dynamic logic operating at liquid helium temperature is compared to room temperature, characterizing the standby performance in terms of the charge decay time. Room temperature dynamic logic operates correctly for frequencies above 180 kHz. Dynamic logic operating at cryogenic temperatures, alternatively, is independent of frequency, correctly operating at DC. The seminal issue of leakage currents in dynamic logic circuits does not exist at 4.2 K, supporting testability at low frequencies while lowering power consumption at high frequencies. The same dynamic circuit operating at 4.2 K exhibits an eight times speed enhancement and an $\sim 10^6$ power consumption improvement over 300 K operation, making dynamic logic at LHT an effective technology for cloud computing platforms.

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