Challenges in High Current On-Chip Voltage Stacked Systems

Kan Xu and Eby G. Friedman

Department of Electrical and Computer Engineering, University of Rochester,
Rochester, New York
(kxu8, friedman)@ece.rochester.edu

***Abstract*—Due to the increasing throughput of high performance integrated circuits, the power consumption of recent high performance computing systems has grown significantly, leading to high on-chip current demand. The large current flowing within the power delivery network leads to challenging issues such as electromigration, low power efficiency, and thermal hotspots. As a technique to reduce on-chip current demand, voltage stacking has become a topic of growing interest within the industrial and academic communities. The challenges of on-chip voltage stacking are however significant. The limitations of relying on on-chip decoupling capacitors when load imbalances occur within a high current system are reviewed. To manage these load imbalances, a ladder topology switched capacitor converter is proposed to regulate the voltages between layers within a voltage stacked system. A 20X improvement in voltage drop is demonstrated on a case study. The current path within a voltage stacked system is quite different from a standard system. A horizontal current path is formed due to the serial connection between layers, producing large parasitic impedances within the power network. The on-chip power network within a voltage stacked system therefore requires careful consideration and specialized design techniques.**

***Index Terms*—Voltage stacking, ladder switched capacitor converter, load balancing, power delivery network.**

I. Introduction

OVER the past few years, the number of cores and throughput of high performance integrated circuits (ICs) have significantly increased [1]–[5]. This increase in the throughput of the processor, and the slowdown in scaling the power supply voltage have led to much greater dynamic power consumption [6]. Aggressive CMOS device scaling has greatly increased gate and channel leakage power, which has become the primary component of the total power dissipated in modern ICs [7]. As a result, the power consumption of a high performance computing (HPC) system is continuing to increase, despite the challenging requirements on system performance [8]. The power consumption of recent high performance CPUs, GPUs, and ASICs can exceed 300 watts [1]–[5]. The IRDS predicts further increases in power consumption in high performance processors [8]. Alternatively, with scaling of power supply voltages and demand for greater current, novel topologies for high performance ICs are being considered [9].

Significant current flow within a high performance IC leads to challenging issues within the power delivery network. Electromigration, an old problem within the IC community [10], has become a major reliability issue in power delivery networks, particularly within the power and ground ball grid array (BGA) and controlled collapse chip connections (C4). Moreover, "last inch" power loss has become a major efficiency concern in high performance ICs due to the quadratic increase with on-chip current demand [11]. This additional power loss in the power network leads to thermal removal issues, which further increase the leakage power and aggravate electromigration concerns. Voltage stacking, also referred to as charge recycling [12] and multistory power delivery networks [13], has recently drawn significant attention from both the industrial and academic communities, targeting HPC systems [12]–[20].

A fully integrated on-chip push-pull switched capacitor converter is used to regulate the voltage when load imbalances occur [14]. A hybrid voltage stacked system is proposed in [12], where an off-chip VRM combined with an on-chip IVR is utilized to address load imbalances. It is reported that 82.4 mm^2 of on-chip area is dedicated for the IVRs [12]. Die unfolding is proposed in [15], where the circuit blocks are grouped into two voltage domains based on a power consumption profile. An optimized framework of logic partitioned for a voltage stacked system is proposed in [16]. Significant work has focused on board level pull-push converters to support voltage stacked systems [17]–[19]. Challenges in high current on-chip voltage stacked systems such as relying on decoupling capacitors and power network parasitic impedances are however minimally discussed.

The rest of the paper is organized as follows. Voltage stacked systems are briefly described in Section II. The effects of load imbalances are also discussed. The limitations of using on-chip decoupling capacitors to alleviate load imbalances in voltage stacked systems are presented in Section III. A symmetric ladder topology switched capacitor converter is introduced in Section IV to tackle load imbalances in a four layer voltage stacked system. Some conclusions are offered in Section V.

II. Load imbalances in voltage stacked systems

Voltage stacking is a circuit and architectural level technique that serially connects multiple voltage domains. In this way, charge flowing through one voltage domain can be "recycled" within the following voltage domains. A high input voltage and low on-chip current are therefore achieved, alleviating electromigration constraints, distribution loss, and thermal hotspots caused by higher on-chip current. Assuming a constant current,

This research is supported in part by the National Science Foundation under Grant No. CCF-1716091, IARPA under Grant No. W911NF-17-9-0001, and by grants from Cisco Systems, Qualcomm, and Synopsys.

978-1-7281-3320-1/20/$31.00 ©2020 IEEE

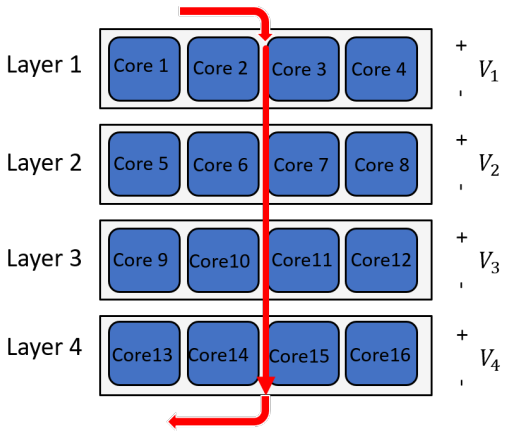


Fig. 1. 16 core four layer voltage stacked system.

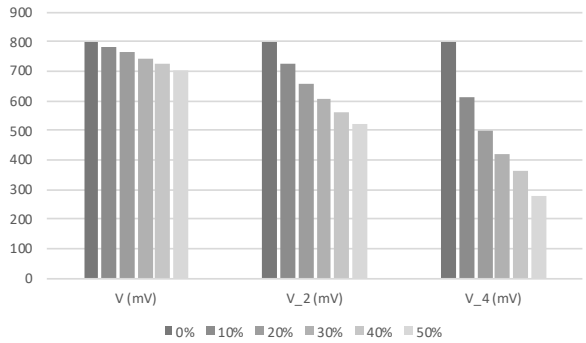


Fig. 2. Variation in voltage levels with activity factor changing from 0 to 50% for a regular system, two layer voltage stacked system, and four layer voltage stacked system.

an n-layer voltage stacked system can ideally reduce the on-chip current demand by $1/\mathrm{n}$, which reduces the IR drop by a factor of n, and the distribution loss by n^2. Voltage stacking is therefore a useful technique to alleviate electromigration in HPC systems, while reducing the metal resources required by the power network and pinouts.

An example of a 16 core, four layer voltage stacked system is illustrated in Fig. 1, where a 16 core processor is divided into four voltage domains. Each voltage domain includes four cores and shares the same voltage level, where V_1 = V_2 = V_3 = V_4. The processor cores within the same voltage domain, for example within layer 1, are connected in parallel. Alternatively, the processor cores in different voltage domains are connected in series, ensuring that the same current flows from layer 1 to layer 4.

The current passing through each stacked layer is ideally the same. In practice, load or current imbalances exist across the stacked layers. These load imbalances lead to voltage variations across the n-layer voltage domains, challenging system performance and reliability. To evaluate the effects of load imbalances on the power noise in a voltage stacked system, a comparative case study has been performed. Three scenarios, a regular power network, a two layer voltage stacked system, and a four layer voltage stacked system, are considered. The input voltage is modeled as a DC voltage source. The power delivery network is modeled as serially cascaded RL branches and parallel RLC branches [21]. The on-chip load is modeled as a resistor R_{load}, where the load activity factor is varied by changing R_{load}.

The specifications of the load imbalance analysis process is listed in Table I. The input voltage V_{in} of a regular system is 0.8 volts, the same as the nominal voltage V_{nom} for the on-chip load. The input voltage of the two layer and four layer voltage stacked systems is, respectively, 1.6 volts and 3.2 volts. The average current flowing to the on-chip load I_{load} is accordingly less, respectively, 80 amperes and 40 amperes. Note that R_{load} of each layer in a voltage stacked system is identical when the loads are balanced. The load imbalances occur when differences in the activity factor between layers exist. Layer-to-layer regulation is not considered in this case study.

TABLE I
SPECIFICATIONS OF THE LOAD IMBALANCE ANALYSIS PROCESS

	V_{in} (V)	V_{nom} (V)	I_{load} (A)	R_{load} ($m\Omega$)
Regular system	0.8	0.8	160	5
Two layer voltage stacking	1.6	0.8	80	10
Four layer voltage stacking	3.2	0.8	40	20

A comparison of the voltage levels within a regular system, a two layer voltage stacked system, and a four layer voltage stacked system with different activity factors is illustrated in Fig. 2. With no change in the activity factor, the voltage level of the three systems remains at a nominal voltage since the loads are balanced. If the activity factor of one of the layers in a voltage stacked system increases, the voltage in that layer becomes lower. The first group shown in Fig. 2 illustrates the voltage level of a regular system while the second and third groups represent, respectively, the two layer and four layer voltage stacked systems. The voltage drop in a voltage stacked system is more sensitive to changes in the activity factor than in a regular system. This behavior occurs because the parasitic impedance of the power delivery network produces a voltage drop in both the regular and voltage stacked systems while voltage division among the layers also occurs in the voltage stacked systems. The lower R_{load} due to the higher activity factor in a certain layer leads to a lower voltage in that layer as compared with the other layers. A larger voltage drop is observed in a voltage stacked system with a larger number of layers. A voltage regulator is therefore necessary in voltage stacked system to alleviate this load imbalance.

III. Limitations of On-Chip Decoupling Capacitors on Case Study

Board-level pull-push converters have been developed to alleviate this load imbalance in voltage stacked systems [17]–[19]. The response of a board-level voltage regulator is however slow due to the large parasitic impedance between the voltage regulator and the on-chip load [9]. An on-chip switched capacitor DC-DC converter with a relatively fast response has been developed for voltage stacked systems [14]. The power consumption is quite low as compared with high performance ICs. To consider the effects of the on-chip decoupling capacitors on load balancing, a case study has been performed. The intention is to verify if a high performance IC

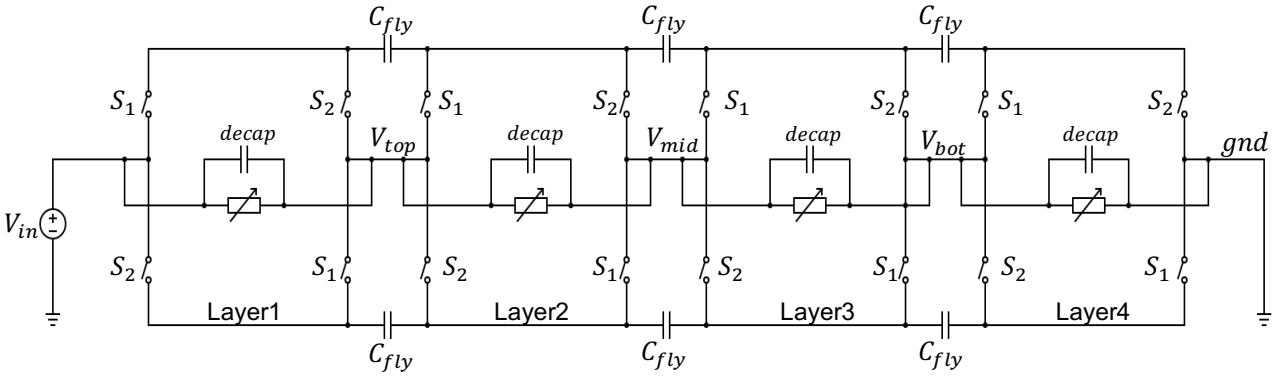


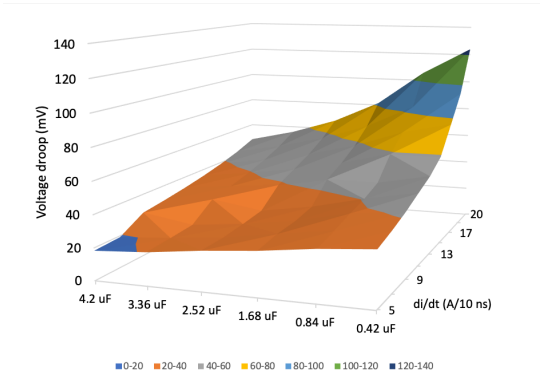
Fig. 3. Symmetric ladder topology switched capacitor converter utilized in a four layer voltage stacked system.

can survive a few hundred nanoseconds after a load imbalance occurs and before an off-chip regulator responds.

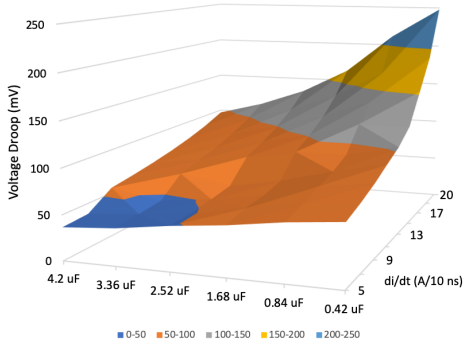
A four layer voltage stacked system is evaluated in this case study. The on-chip decoupling capacitor [6] is

$$C_{decap} = \frac{P}{V^2 f}\frac{1-\alpha}{\alpha}, \tag{1}$$

where P is the dynamic power consumption of an IC, assumed to be 60 watts. f is the operating frequency of the IC, assumed to be 2 GHz. α is the switching factor of the IC, assumed to be 10%. V is the nominal voltage, 0.8 volts in this case study. The magnitude of the on-chip decoupling capacitor is 0.42 μF based on (1). To evaluate the effects of the decoupling capacitor on the load balance in a worst case scenario, I_{load} is assumed to be 40 amperes and only one layer exhibits a change in activity factor. A transient current of 0.3 A/ns is applied [21]. A range of di/dt from 0.5 A/ns to 2 A/ns is assumed in this case study. The variation of the voltage droop in the voltage stacked system as a function of on-chip decoupling capacitance and transient current during a load imbalance is illustrated in Fig. 4. The response shown in Figs. 3a and 3b are produced, respectively, 5 ns and 10 ns after the load imbalances occurs. At 5 ns, the intrinsic on-chip decoupling capacitor is sufficient to maintain the voltage droop below the 5% margin with a normal transient current, as illustrated in Fig. 3a. Alternatively, to ensure that the voltage droop at 10 ns is below the 5% margin, a minimum 2.52 μF on-chip decoupling capacitor is required and the transient current can not be larger than 0.9 A/ns, as illustrated in Fig. 3b. The response time of a typical off-chip voltage regulator is often larger than 10 ns. An on-chip voltage regulator is therefore necessary to alleviate load imbalances in voltage stacked systems.



a)



b)

Fig. 4. Voltage droop as a function of on-chip decoupling capacitance and transient current during a load imbalance, (a) 10 ns, and (b) 5 ns. Note the decoupling capacitance ranges from 0.42 to 4.2 μF and the transient current ranges from 0.5 to 2 A/ns.

IV. Ladder Topology Switched Capacitor Voltage Regulator

A linear regulator suffers from low efficiency, particularly when the dropout voltage and/or supply current is high. A linear regulator is therefore not desirable in a high current voltage stacked system. Although a buck converter can provide high current with high efficiency, the size of the passive elements, particularly the output inductor, in a buck converter is often excessively large, leading to a challenge in on-chip integration. With the advancement of integrated capacitor technologies, high density on-chip capacitors have become feasible for on-chip regulators [22]. A switched capacitor converter is therefore considered here.

A symmetric ladder topology switched capacitor converter [23] is utilized in the four layer voltage stacked system, as illustrated in Fig. 3. Five voltage levels are provided by the converter, V_{in}, V_{up}, V_{mid}, V_{low}, and V_{Gnd}, dividing the IC into four layers. Each layer is connected to an adjacent voltage level, forming four voltage domains. The load of each layer is modeled as a resistor in parallel with a decoupling capacitor. The nominal voltage for each layer is assumed to be 0.8 volts.

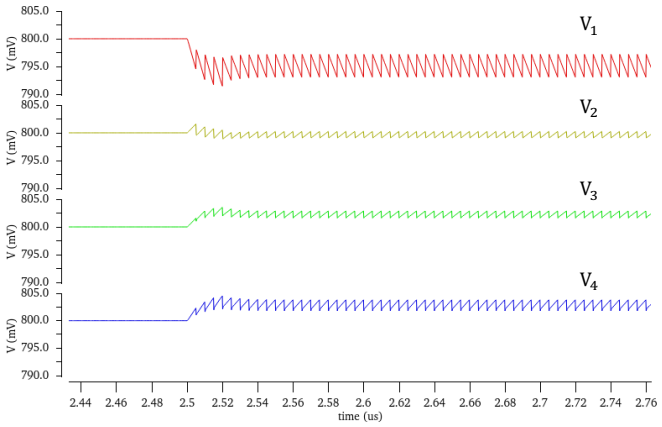


Fig. 5. Voltage droop after 10% load imbalance within a four layer voltage stacked system with a ladder switched capacitor converter.

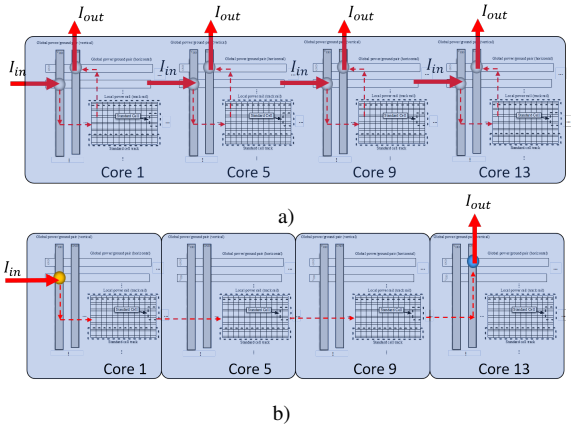


Fig. 6. Comparison of the current path between a) a regular four core system, and b) a four layer voltage stacked system.

V_{in} is therefore 3.2 volts. Six capacitors are connected to different voltage domains through switches, as illustrated in Fig. 3. Note that these capacitors are flying capacitors since the capacitors are not directly connected to ground. Depending upon the operation of the switches, the flying capacitor, C_1 for example, is connected to the first or the second voltage domain. The switches are divided into two groups, S_1 and S_2, which are intermittently turned on and off. When the load is balanced, the current flowing through each layer is identical; the current passes through each of the four layers without flowing through the flying capacitors. Alternatively, when the load is unbalanced, the activity factor of each layer is different, current also flows to the flying capacitors and switches. The flying capacitors charge and discharge depending upon the direction of the current. In this way, charge is passed between each of these four layers, regulating the voltage of each layer when a load imbalance occurs.

Simulation of this symmetric ladder switched capacitor converter is performed in Cadence Virtuoso, utilizing the PSPICE transistor model for the switches. As discussed in the previous section, the on-chip converter responds within 10 ns after the load imbalance occurs and before the voltage droop reaches the 5% noise margin. The switching frequency of the circuit is therefore 100 MHz. The total flying capacitance is 4.5 μF, which is practical for on-chip integration with a deep trench capacitor technology [22]. The decoupling capacitor is 0.42 μF, which is evenly distributed among the four layers. A 10% increase in activity factor models the load imbalance. To produce the worst case load imbalance scenario, the activity factor of only one layer changes while the activity factor of the other layers are maintained constant.

The voltage droop after the load imbalance occurs is illustrated in Fig. 5. The voltage levels across the four layers are illustrated, respectively, as V_1, V_2, V_3, and V_4. The voltage level of the four layers is initially stable at 0.8 volts due to the balanced load condition. The load imbalance occurs at 2.5 μs, where V_1 and V_2 exhibit a voltage drop while V_3 and V_4 exhibit a rise in voltage. The first layer with a changing activity factor exhibits a worst case voltage drop of about 10 mV, which is 20X lower than the voltage drop without regulation, as described in the previous section. In a voltage stacked system without regulation, only the layer with a higher activity factor exhibits a voltage drop; the remaining layers exhibit a rise in voltage. As illustrated in Fig. 5, V_2 also exhibits a voltage drop. This behavior occurs because the switched capacitor converter does not regulate a specific layer but rather naturally balances the load among all four layers [24]. Regulation schemes of switched capacitor converter are not considered [25, 26].

Note that the parasitic impedance of the power network connecting adjacent layers is not considered in this case study. Due to the serial connection between each layer, the current distribution path in a voltage stacked system is different from a regular system. A comparison of the current path between a four core regular system and a four layer voltage stacked system is illustrated in Fig. 6. In a regular system, the current distribution is dominated by the current flowing from the bumps to the on-chip load, as illustrated in Fig. 6a. In a voltage stacked system, the current flows through the serially connected power network, producing a horizontal current path, as illustrated in Fig. 6b. This horizontal current path produces a large voltage drop across the parasitic impedances within the power network, degrading the performance of the voltage regulator within the voltage stacked system. The on-chip power network in a voltage stacked system should therefore be carefully considered.

V. Conclusions

Challenges in applying on-chip voltage stacking to high current systems are discussed in this paper. The power noise in a voltage stacked system is more sensitive to changes in the activity factor than in a regular system. The on-chip intrinsic decoupling capacitance is not sufficient to manage the significant load imbalances within a voltage stacked system. An on-chip voltage regulator is therefore required to alleviate these load imbalances, regulating the voltage between layers. A symmetric ladder switched capacitor converter is presented, demonstrating good regulation for a 10% load imbalance. A 20X lower voltage drop is achieved as compared to no on-chip regulation. The current path within a voltage stacked system is quite different from a regular system, requiring special consideration during development of the on-chip power network.

REFERENCES

[1] T. Paul, "Tearing Apart Google's TPU 3.0 AI Coprocessor," https://www.nextplatform.com/2018/05/10/tearing-apart-googles-tpu-3-0-ai-coprocessor/, 2018.

[2] Intel ARK (Product Specs), "https://ark.intel.com/products/95830/Intel-Xeon-Phi-Processor-7295-16GB-1_50-GHz-72-core," 2018.

[3] S. K. Sadasivam, B. W. Thompto, R. Kalla, and W. J. Starke, "IBM Power9 Processor Architecture," *IEEE Micro*, Vol. 37, No. 2, pp. 40–51, March 2017.

[4] Nvidia, "https://images.nvidia.com/content/volta-architecture/pdf/volta-architecture-whitepaper.pdf," 2018.

[5] Radeon Technologies Group (AMD), "https://www.amd.com/en," 2017.

[6] I. P. Vaisband, R. Jakushokas, M. Popovich, A. V. Mezhiba, S. Kose, and E. G. Friedman, *On-Chip Power Delivery and Management, Fourth Edition*, Springer International Publishing, 2016.

[7] E. Salman and E. G. Friedman, *High Performance Integrated Circuit Design*, McGraw-Hill Professional, 2012.

[8] IRDS Roadmap Teams, *International Roadmap for Devices and Systems*, 2017.

[9] K. Xu, B. Vaisband, G. Sizikov, X. Li, and E. G. Friedman, "Power Noise and Near-Field EMI of High-Current System-in-Package With VR Top and Bottom Placements," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, Vol. 9, No. 4, pp. 712–718, April 2019.

[10] J. R. Black, "Electromigration–A Brief Survey and Some Recent Results," *IEEE Transactions on Electron Devices*, Vol. 16, No. 4, pp. 338–347, April 1969.

[11] K. Xu, B. Vaisband, G. Sizikov, X. Li, and E. G. Friedman, "EMI Suppression with Distributed LLC Resonant Converter for High Voltage VR-on-Package," *IEEE Transactions on Components, Packaging and Manufacturing Technology*, pp. 1–1, 2019, doi: 10.1109/TCPMT.2019.2960699.

[12] A. Zou *et al.*, "Efficient and Reliable Power Delivery in Voltage-stacked Manycore System with Hybrid Charge-recycling Regulators," *Proceedings of the IEEE/ACM Design Automation Conference*, pp. 43:1–43:6, June 2018.

[13] Q. Zhang, L. Lai, M. Gottscho, and P. Gupta, "Multi-Story Power Distribution Networks for GPUs," *Proceedings of the ACM Design, Automation Test in Europe Conference*, pp. 451–456, March 2016.

[14] T. Tong *et al.*, "A Fully Integrated Reconfigurable Switched-Capacitor DC-DC Converter with Four Stacked Output Channels for Voltage Stacking Applications," *IEEE Journal of Solid-State Circuits*, Vol. 51, No. 9, pp. 2142–2152, September 2016.

[15] E. K. Ardestani *et al.*, "Managing Mismatches in Voltage Stacking with CoreUnfolding," *ACM Transactions on Architecture and Code Optimization*, Vol. 12, No. 4, pp. 43:1–43:26, November 2015.

[16] K. Blutman *et al.*, "Logic Design Partitioning for Stacked Power Domains," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, Vol. 25, No. 11, pp. 3045–3056, November 2017.

[17] C. Schaef and J. T. Stauth, "Efficient Voltage Regulation for Microprocessor Cores Stacked in Vertical Voltage Domains," *IEEE Transactions on Power Electronics*, Vol. 31, No. 2, pp. 1795–1808, February 2016.

[18] K. Kesarwani, C. Schaef, C. R. Sullivan, and J. T. Stauth, "A Multi-Level Ladder Converter Supporting Vertically-Stacked Digital Voltage Domains," *Proceedings of the IEEE Applied Power Electronics Conference and Exposition*, pp. 429–434, March 2013.

[19] P. S. Shenoy and P. T. Krein, "Differential Power Processing for DC Systems," *IEEE Transactions on Power Electronics*, Vol. 28, No. 4, pp. 1795–1806, April 2013.

[20] K. T. Zhan and *et al.*, "Serial Power Supply Circuit, Virtual Digital Coin Mining Machine and Computer Server," China Patent CN105045364A, 2016.

[21] Intel Pentium 4 Processor in the 423 pin package/Intel 850 Chipset Platform, "http://happytrees.org/files/chips/datasheets/datasheet-Intel-Pentium-4–423-pin–1.30,1.40,1.50,1.60,1.70,1.80,1.90,2GHz.pdf," 2001.

[22] L. Chang *et al.*, "A Fully-Integrated Switched-Capacitor 2:1 Voltage Converter with Regulation Capability and 90% Efficiency at 2.3 A/mm^2," *Proceedings of the IEEE Symposium on VLSI Circuits*, pp. 55–56, June 2010.

[23] I. Vaisband, M. Saadat, and B. Murmann, "A Closed-Loop Reconfigurable Switched-Capacitor DC-DC Converter for Sub-mW Energy Harvesting Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 62, No. 2, pp. 385–394, February 2015.

[24] L. Delmas, G. Gateau, T. A. Meynard, and H. Foch, "Stacked Multicell Converter (SMC): Control and Natural Balancing," *Proceedings of the IEEE Power Electronics Specialists Conference*, Vol. 2, pp. 689–694, June 2002.

[25] B. P. McGrath, T. Meynard, G. Gateau, and D. G. Holmes, "Optimal Modulation of Flying Capacitor and Stacked Multicell Converters Using a State Machine Decoder," *IEEE Transactions on Power Electronics*, Vol. 22, No. 2, pp. 508–516, March 2007.

[26] A. K. Sadigh, S. H. Hosseini, M. Sabahi, and G. B. Gharehpetian, "Double Flying Capacitor Multicell Converter Based on Modified Phase-Shifted Pulsewidth Modulation," *IEEE Transactions on Power Electronics*, Vol. 25, No. 6, pp. 1517–1526, June 2010.