Spintronic/CMOS-Based Thermal Sensors

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***Abstract*—Stacking more systems into a compact area or scaling devices to increase the density of integration are two approaches to provide greater functional complexity. Excessive heat generated as a result of these technology advancements leads to an increase in leakage power and degradation in system reliability. Hence, a thermal aware system composed of hundreds of distributed thermal sensor nodes is needed. Such a system requires an efficient thermal sensor placed close to the thermal hotspots, small in size, fast response, and CMOS compatibility. In this paper, two hybrid spintronic/CMOS circuits are proposed. These circuits exhibit a low power consumption of 11.9 μW during the on-state, a linearity (R^2) of 0.96 over the industrial temperature range of operation (-40 to 125)^oC, and a sensitivity of 3.78 mV/K.**

I. Introduction

Thermal aware systems are becoming increasingly important due to the greater number of integrated transistors and the stacking of multiple dies within the same package. The excessive heat affects system performance, while degrading the reliability of the system and increasing the leakage current. Hence, an integrated system of distributed thermal sensors is becoming increasingly necessary. The thermal sensors should be placed close to the local hot spots, small in size, provide a fast response, and CMOS compatible.

Conventional methods for allocating a small number of integrated thermal sensors is insufficient to fully monitor the thermal behavior of a large scale system [1], [2]. CMOS-based thermal sensors exhibit low sensitivity and an exponential relationship with temperature, complicating the process of estimating the ambient temperature [3], [4]. Hence, to increase sensor accuracy and sensitivity, additional computational blocks, such as amplifiers, A/D converters, and look-up tables, should be added to determine the precise temperature [5], [6]. This complexity makes it difficult to distribute hundreds of thermal sensors across an integrated system.

In this paper, hybrid spintronic/CMOS based thermal sensors are proposed as the backbone of a next generation thermal aware system. The proposed thermal sensing circuits exhibit small area, high sensitivity, and low power. These circuits operate over a wide temperature range with high sensitivity and linearity, making the proposed hybrid spintronic/CMOS circuits competitive with CMOS-only thermal sensors.

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The paper is organized as follows. The thermal influence on spintronic and CMOS devices is described in Section II. The proposed thermal sensors are reviewed in Section III. A comparison between the spintronic/CMOS-based thermal sensors and CMOS-only thermal sensors is presented in Section IV, followed by the conclusions in Section V.

II. Temperature effects on the resistance of electronic devices

Resistance describes the movement of electrons from one atom to another under the influence of an electric field. The movement of electrons is characterized by interactions and scattering within the device material, which causes the devices and interconnects to heat up. The heat generated from these interactions changes the ambient temperature, causing the atoms to vibrate at a higher rate. The higher the temperature, the more violently the atoms vibrate, affecting the resistance of the electronic devices.

To simplify the influence of temperature on the resistance of an electronic device, two types of devices are considered as thermal resistors with a temperature coefficient of resistance TCR, as described by the following expression,

$$\frac{R-R_{Ref}}{T-T_{Ref}} = \frac{dR}{dT} = TCR \times R_{Ref}, \tag{1}$$

where T_{Ref} is a reference temperature at 0^oC, and R_{Ref} is the resistance at T_{Ref}. TCR describes an absolute measure of the relative change of a thermal resistor to a change in temperature. The change in the resistance of a magnetic tunnel junction (MTJ) (a spintronic device) and a CMOS transistor is described, respectively, in Sections II-A and II-B.

A. Thermal behavior of an MTJ

A magnetic tunnel junction (MTJ) is an emerging spintronic device composed of two ferromagnetic (FM) layers separated by a non-magnetic insulator layer [7]. An MTJ exhibits two states of operation. A parallel state, where the two FM layers are magnetized in the same direction, and an antiparallel state, where the orientation of the magnetization of the two FM layers is 180^o apart. The resistance of the MTJ in the antiparallel state is higher than in the parallel state due to the spin filtering process within the MTJ structure [7].

The conductance of an MTJ is composed of two primary components, a spin-dependent (elastic) conductance and a spin independent (inelastic) conductance. Both conductance

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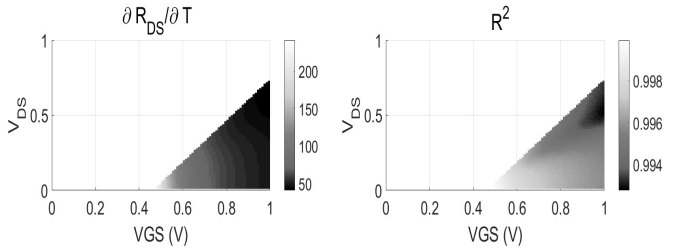
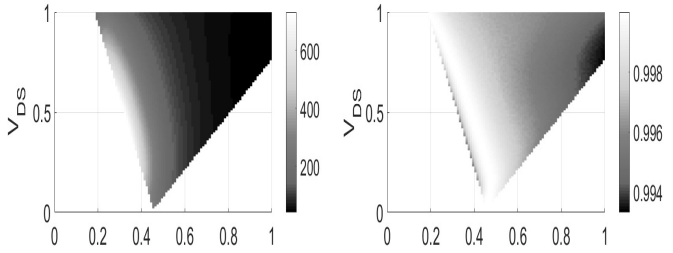


(a)



(b)

Fig. 1: Linearity and sensitivity of a CMOS transistor at different bias conditions, a) linear region, and b) saturation region

components exist in the parallel and antiparallel states but with different contributions. The MTJ conductance is due to a mixture of different mechanisms such as hopping dependent tunneling, magnon assisted tunneling, phonon assisted tunneling, and direct spin polarized tunneling [8], [9], [10]. An increase in temperature causes an increase in the number of impurities which enhances the hopping mechanism, thereby raising the hopping conductance [11]. The temperature influences the magnetoresistance of the ferromagnetic layers of the MTJ and the magnetism of the interface between the ferromagnetic layers and the insulator [11], [12], [13]. Most of the conductance in the MTJ parallel state is direct spin polarized conductance, which is less affected by temperature than other types of conductance mechanisms.

The antiparallel resistance of an MTJ is more sensitive to temperature than the parallel state, since most of the conductance mechanisms contributing to the antiparallel state are an inelastic conductance which exhibits a high temperature dependence [13], [14], [15]. A compact physical model of an MTJ based on experimentally fabricated devices is described in this paper to characterize the electrical and magnetic behavior of an MTJ [15], [16], [17]. As an example, an MTJ with a sense voltage of 0.8 volts exhibits a $TCR|_{MTJ}$ of $-8\times10^{-5}1/^{o}C$ and a linearity R^2 of 0.99999. The thermal behavior of a CMOS transistor is described in Section II-B.

B. Thermal behavior of a CMOS transistor

The temperature dependence of a CMOS transistor depends upon whether the device is operating in the linear or saturation region. The linearity and sensitivity of the change in drain-to-source resistance of a CMOS transistor to temperature are illustrated in Figure 1. As an example, a CMOS transistor operating in saturation with $V_{GS}=0.45$ volts and $V_{DS}=0.45$ volts exhibits a $TCR|_{Transistor}$ of $53\times10^{-4}1/^{o}C$ and a linearity of 0.9992.

A saturated transistor features a high linearity of up to 1 and a sensitivity approaching 600 ohms/K while an MTJ exhibits a negative sensitivity approaching -4 ohms/K but with higher linearity. The sensitivity of an MTJ can be controlled by changing the size, bias point, or material [15], [18]. In this paper, an MTJ is biased with a CMOS transistor, where the thermal influence of both devices compensates each other to achieve a thermal sensor with high sensitivity and linearity. The proposed circuits are presented in the following section.

III. Proposed spintronic/CMOS-based thermal sensors

MTJ devices are combined with CMOS to provide an efficient temperature sensor. The sensing technique considers the effects of temperature and sense voltage on the thermal stability and resistance of an MTJ. An MTJ exhibits higher sensitivity in the AP state than in the P state [9], [19], [20]. Hence, an MTJ is designed to operate as a thermal sensor in the stable AP state despite fluctuations in operating temperature and supply voltage. The thermal stability Δ of an MTJ determines the limits of the applied voltage and range of temperature over which the device can stably operate without switching [15]. Δ is the ratio of the magnetization energy of an MTJ and the thermal perturbation to the system, which is a function of temperature and applied voltage,

$$\Delta(T,V)=\frac{\Delta E(T,V)|_{MTJ}}{K_BT}=\frac{K_{eff}(T,V)v_{FM}}{K_BT}, \tag{2}$$

where K_B is the Boltzmann constant, $\Delta E(T,V)|_{MTJ}$ is the system anisotropy energy of an MTJ, K_{eff} is the effective anisotropy constant, and v_{FM} is the volume of the FM layer. Fluctuations in the sense voltage when switching an MTJ is related to the critical switching voltage of an MTJ,

$$V_{C0}(T)|_{PMTJ}\approx \frac{t_{ox}t_{FM}}{\zeta_{VCMA}(T)}\left[\frac{K_i(T)}{t_{FM}}-\frac{1}{4}\mu_0(N_z-N_{x,y})M_S(T)^2\right]. \tag{3}$$

CMOS-only thermal sensors exhibit an exponential relationship with temperature which complicates the measurement process. To exploit the capabilities of both an MTJ and CMOS transistor to sense temperature, both of these devices are used within the same circuit. Two different MTJ/CMOS-based thermal sensing circuits are proposed in this paper, as shown in Figure 2. These circuits are described in terms of the thermal sensitivity and linearity characteristics in, respectively, Sections III-A and III-B.

A. Circuit I, Hybrid-I MTJ/transistor

Circuit I, Hybrid-I is composed of a transistor and an MTJ, where the output voltage V_{out} (the drain-to-source voltage) exhibits a linear relationship between the output voltage of the circuit and the temperature. Note the decrease in the MTJ resistance and increase in the transistor resistance with temperature; both devices compensate each other and hence the output voltage exhibits a linear relationship with temperature.

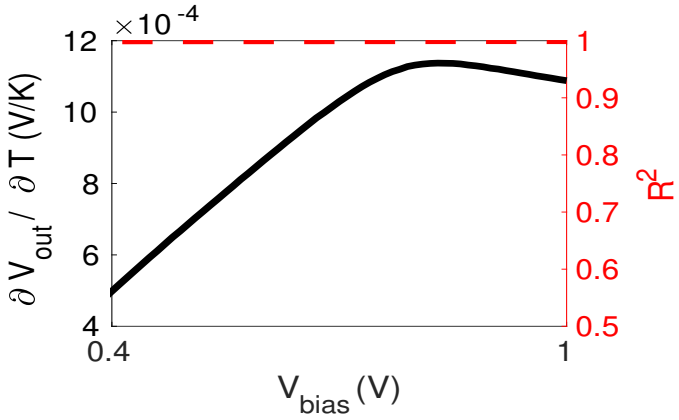
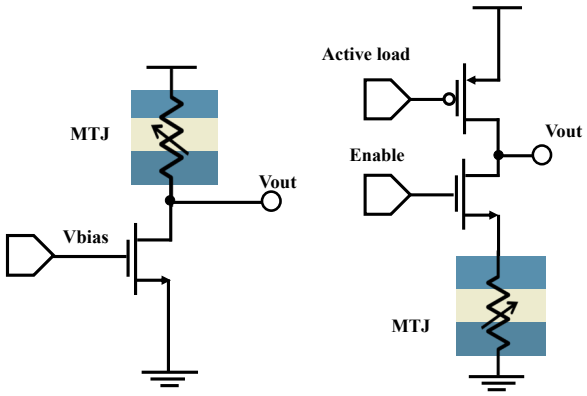


Fig. 3: Thermal performance of the Hybrid-I circuit; sensitivity $\partial V_{out}/\partial T$ (solid line) and linearity R^2 (dotted line)



(a) (b)

Fig. 2: Proposed CMOS/MTJ thermal sensors, a) Hybrid-I MTJ/transistor, and b) Hybrid-II MTJ/transistor with an active load

The output voltage V_{out} of Circuit I is described by the following expression,

$$V_{out1} = \frac{V_{DD}R_{DS}(T)}{R_{DS}(T)+R_{MTJ}(T)}, \tag{4}$$

where R_{DS} and R_{MTJ} are, respectively, the drain-to-source resistance of the transistor and the resistance of the MTJ. As previously mentioned, a change in the resistance of both the transistor and MTJ with temperature compensates each other, making the output voltage directly proportional to the temperature.

The linearity and sensitivity of the output voltage of Hybrid-I under different bias conditions are illustrated in Figure 3. The circuit achieves a sensitivity of up to 1.2 mV/K and a linearity of almost 1. These simulations are based on the predictive transistor model (PTM) for CMOS transistors [21]. The CMOS transistors are 32 nm × 16 nm [21], and the 16 nm PTM model parameters are based on BSIM-CMG [22].

Although Hybrid-I exhibits high linearity and sensitivity, note the circuit behavior under thermal or bias fluctuations. The MTJ in Hybrid-I provides a stable feedback system, since any decrease in R_{MTJ} with an increase in temperature will raise the drain voltage, maintaining the transistor within the saturation region. As previously mentioned, operating a transistor in the saturation region enhances the linearity and sensitivity of the circuit. Hybrid-I cannot however maintain stable operation under fluctuations in the supply voltage. Hybrid-II is proposed to overcome this disadvantage, as described in the following subsection.

B. Circuit II, Hybrid-II

Circuit II, Hybrid-II is composed of an NMOS transistor, PMOS transistor, and an MTJ. The PMOS transistor is biased at a DC operating point, labeled as Active load, as illustrated in Figure 2-b. Hybrid-II provides greater control on the bias voltage by changing the state of the active load. In addition, the NMOS, PMOS, and MTJ devices contribute to the relationship between the output voltage and temperature, which affects both the linearity and sensitivity of the circuit. The resistance of both the NMOS and PMOS transistors increases with temperature, while the MTJ resistance decreases. The nonlinear increase in the resistance of the NMOS and PMOS devices compensates the linear decrease in the resistance of the MTJ, maintaining a linear relationship with temperature, as expressed by (5). The output voltage of the circuit is described by the following expression,

$$V_{out2} = \frac{V_{DD}R_{DS1}(T)}{R_{DS1}(T)+R_{DS2}(T)+R_{MTJ}(T)}. \tag{5}$$

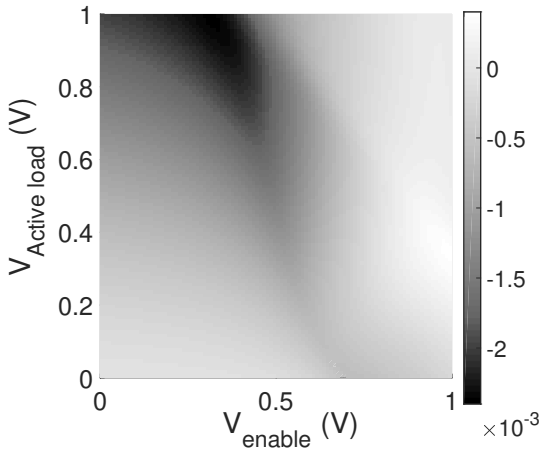
The variation in linearity and sensitivity of Hybrid-II under different bias conditions is illustrated in Figure 4. The circuit exhibits a sensitivity of up to 2.2 mV/K with a linearity approaching 1. Over a wide range of bias conditions, Hybrid-II maintains high linearity and sensitivity, making the circuit a good candidate to overcome fluctuations in the bias voltage. The dark area in Figure 4-a describes where the circuit exhibits the highest sensitivity and linearity.

To provide further insight into the superiority of the proposed circuits, a comparison between four thermal sensors (a diode connected transistor, two paired transistors, Hybrid-I, and Hybrid-II) is characterized in terms of the sensitivity, linearity, power consumption, and area, as presented in Section IV.

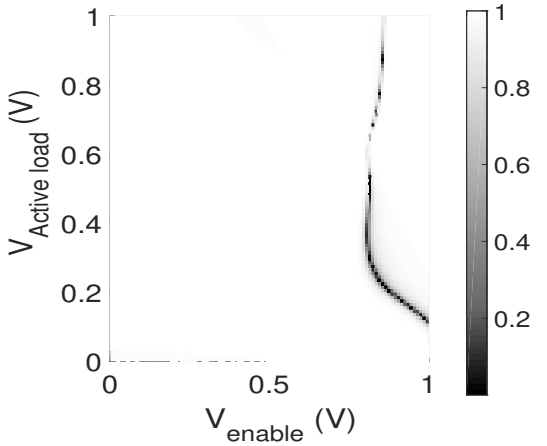
IV. Comparison of Thermal Sensors

The proposed circuits benefit from the influence of temperature on the transistor parameters (such as the threshold voltage, mobility, saturation velocity, gate tunneling current, tunneling and recombination current, drain induced barrier lowering, impact ionization, and body effect) and the MTJ antiparallel resistance. The proposed MTJ/CMOS-based thermal sensors are illustrated in Fig. 2 while the CMOS-only circuits are illustrated in Figure 5. A comparison of the four different circuits clarifies the advantages of the hybrid thermal sensor composed of an MTJ with CMOS.

Circuits CMOS-I and CMOS-II are CMOS-only thermal sensors, where CMOS-I is a diode connected thermal sensor

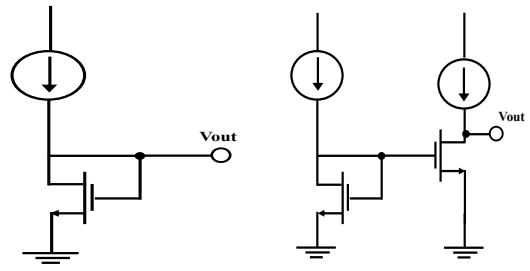


(a)



(b)

Fig. 4: Thermal performance of the Hybrid-II circuit, a) sensitivity $\partial V_{out}/\partial T$, and b) linearity R^2. The dark area in (a) describes where the circuit exhibits the highest sensitivity and linearity.



(a) (b)

Fig. 5: CMOS-only sensors, a) CMOS-I, diode connected transistor, and b) CMOS-II, two paired transistors

biased by a current source, and CMOS-II is the same as CMOS-I followed by a common source amplifier. A comparison of these sensors is listed in Table I. The CMOS transistors are sized the same (32 nm $\times$ 16 nm) and biased at the same current (17 μA) to establish a fair comparison.

For the two CMOS thermal sensors, these circuits exhibit good sensitivity with reasonable linearity. In Hybrid-II, the two CMOS transistors and MTJ behave as temperature sensor elements. Hybrid-II exhibits a higher thermal sensitivity than Hybrid-I. In terms of power consumption, Hybrid-II exhibits the lowest power consumption. The MTJ/CMOS thermal sensor requires less area since no current source is required. CMOS-II exhibits a higher linearity than CMOS-I but requires more area. Based on Table I, Hybrid-II provides appropriate capabilities for a system requiring a large number of on-chip distributed temperature sensors.

Table I: Comparison of the proposed temperature sensor and conventional CMOS sensors in terms of sensitivity, linearity, power consumption, and area

		CMOS-I	CMOS-II	Hybrid-I	Hybrid-II
Sensitivity (mV/K)	**Commercial (0 to 85)**	0.51	0.51	0.4	1.91
	Industrial (-40 to 100)	1.03	1.03	0.64	3.78
	Automotive (-40 to 125)	1.08	1.08	0.77	3.97
	Military (-55 to 125)	1.35	1.35	0.81	4.8
Linearity	**Commercial (0 to 85)**	0.985	0.985	1	0.983
	Industrial (-40 to 100)	0.953	0.953	0.999	0.96
	Automotive (-40 to 125)	0.941	0.941	0.999	0.947
	Military (-55 to 125)	0.919	0.919	0.996	0.936
Power Consumption at 27^{o}C (μW)		40	80	18	11.9
Area (μm^2)		4X	8X	1X	2X

V. Conclusions

Two hybrid spintronic/MTJ thermal sensors are proposed in this paper. These circuits are based on a magnetic tunnel junction which exhibits a thermal sensing capability with a linearity up to 0.983 and a thermal sensitivity of 1.91 mV/K over a wide range of operational temperatures while consuming low power (32 μW). Incorporating an MTJ with a CMOS transistor exhibits a sensitivity of 3.78 mV/K and a linearity approaching 1 while consuming only 11.9 μW during the on-state over a temperature range of -40 to 125^oC. The proposed hybrid spintronic/CMOS temperature sensors are appropriate within a next generation thermal aware system composed of hundreds of on-chip distributed thermal sensor nodes.

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