MTJ-Based Dithering for Stochastic Analog-to-Digital Conversion

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Abstract— **The stochastic behavior of magnetic tunnel junctions (MTJ) finds use in many applications – from analog-to-digital conversion to neuromorphic computing. In this paper, a dithering method exploiting the stochastic behavior of an MTJ, based on the voltage controlled magnetic anisotropy effect, is proposed. This method is used to measure low frequency analog signals over an interval. The circuit is composed of two MTJ devices that convert an analog signal into a series of high resistance and low resistance stochastic states, creating a dithering effect. The behavior of the input signal is extracted from the switching frequency. The binary nature of the output signal reduces the complexity, enabling a small, fast, and energy efficient circuit for extracting different forms of information from an analog signal.**

I. Introduction

Exploring the stochastic behavior of magnetic tunnel junctions (MTJ) induced by the voltage controlled magnetic anisotropy (VCMA) effect has opened numerous possibilities for MTJ applications. Examples include neuromorphic computing [1], analog-to-digital conversion [2, 3], and random number generation [4]. One of the most important properties of the VCMA switching mechanism in MTJs is the dependence of the switching probability on the applied voltage. This effect can be used to convert a signal into a series of high resistance and low resistance stochastic states, depending upon the direction of magnetization of the free layer within the MTJ [5]. Utilizing this property enables the use of MTJs as dithering elements. This dithering is applied in an MTJ-based stochastic analog-to-digital converter (MSADC). The MSADC utilizes the method of measurement over an interval [6], which can be used for analog-to-information conversion (AIC).

The paper is organized as follows. In Section II, the concepts of analog-to-information conversion, measurement over an interval, and dithering are introduced. The MSADC circuit is described in Section III. In section IV, a compact model of an MTJ within the MSADC is presented and characterized. The paper is concluded in Section V.

II. Background

The tradeoff between accuracy and speed in analog-to-digital converters (ADC) presents an important challenge in electronic systems. The concept of analog-to-information conversion is introduced to mitigate the constraints of an ADC while preserving the information from the signal of interest. This approach is explained in Section II-A. In Section II-B, small and fast AICs based on the concept of measurement of a signal over an interval are presented. Dithering is explained in Section II-C.

A. Analog-to-information conversion

Processing wideband signals by Nyquist rate ADCs is often prohibitive due to constraints on the resolution and power requirements [7]. The concept of analog-to-information converters is introduced to mitigate these restrictions [8, 9]. Most solutions for AICs are based on reducing the sampling rate by applying compressed sensing (CS) [8-10]. CS explores the notion that the bandwidth of certain types of information embedded within a signal is often smaller than the bandwidth of the signal, and can therefore be recovered by sub-Nyquist rate sampling. Capturing information from the signal without reconstructing the signal waveform in the digital domain is therefore enabled, alleviating constraints on the high speed analog-to-digital converter.

B. Measurement over an interval

For certain applications, *e.g.,* internet-of-things (IoT) and power sensors, a long measuring time is expected. Increasing the time interval for signal processing enables a different approach for analog-to-information conversion, based on the concept of measurement over an interval [6]. Rather than reducing the sampling rate to relax hardware constraints by applying CS, this approach is based on oversampling signals over a certain time interval and extracting the integral. The method is based on low resolution flash ADCs, enabling low complexity, while a large number of samples maintains the accuracy of the measurement. This approach can be used to provide different forms of information describing the integral of a physical quantity (*e.g.,* average value, RMS, harmonic spectrum). An important aspect of measurement over an interval is dithering – adding random noise to the measured signal.

C. Dithering

With certain limitations, dithering can increase the effective resolution of analog-to-digital converters by decreasing the effects of quantization noise [11-13]. Quantization introduces distortions into a signal waveform that can misrepresent the

converted signal. This effect can be mitigated by increasing the resolution of the converter. A tradeoff is produced between accuracy and complexity which can be relaxed by applying high frequency random noise (dither) to the input signal [14, 15].

An effect of dithering is illustrated in Fig. 1. A low amplitude sine wave is applied to a two bit quantizer (see Fig. 1(a)). The input signal waveform is contained within a quantization step. The output of the quantizer, which provides insufficient information describing the signal, is shown in Fig. 1(b). Applying dither, as shown in Fig. 1(c), increases the amount of information at the output (Fig. 1(d)), enabling higher precision with the same ADC resolution.

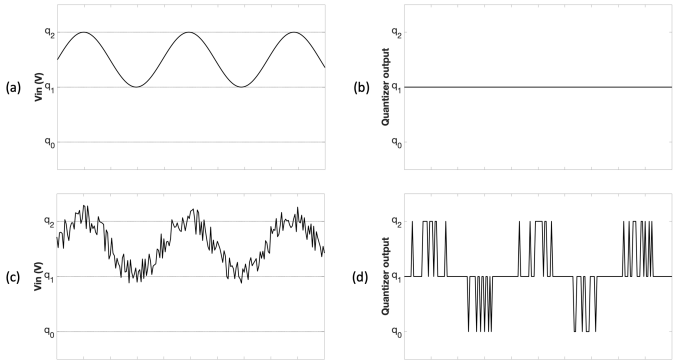

Fig. 1 – Quantization with and without dithering, with quantization levels denoted by q_0, q_1 and q_2. (a) Small amplitude sinusoid applied to a quantizer. (b) Quantized sine wave with insufficient information describing the signal waveform. (c) Sinusoid with added dither. (d) The output of the quantized dithered sinusoid with additional information describing the input signal.

III. Proposed Stochastic ADC

Measuring a signal over an interval can be achieved with low resolution flash ADCs with added dither. This approach is explained in Section II-A. Applying a voltage across an MTJ induces the voltage controlled magnetic anisotropy effect, introducing random noise into the input signal. The VCMA effect is explained and an MTJ-based stochastic ADC is proposed in Section II-B.

A. Theory of operation

A block diagram of a stochastic ADC to measure a signal over an interval [6] is shown in Fig. 2, where *m* is the signal being measured and *d* is the dither – random noise added to the signal. Combining a low resolution flash ADC with dither increases the effective resolution of the integral (*e.g.*, the average value or RMS) over a time interval.

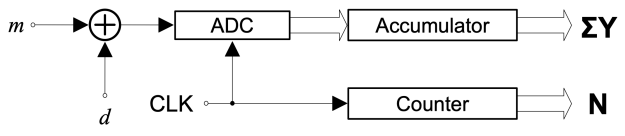

Fig. 2. Block diagram of a stochastic ADC to measure a signal over an interval.

To perform elementary measurements over an interval, a two bit flash ADC is used [16]. This converter produces three output states:

$$\begin{array}{lll} 1 & \text{for} & (m+d) > +Vref \\ 0 & \text{for} & -Vref < (m+d) < +Vref \\ -1 & \text{for} & (m+d) < -Vref \end{array}$$

as illustrated in Fig. 3. In the case of a two bit converter, the accumulator is reduced to an up/down counter. This output format enables mathematical operations with elementary logic gates.

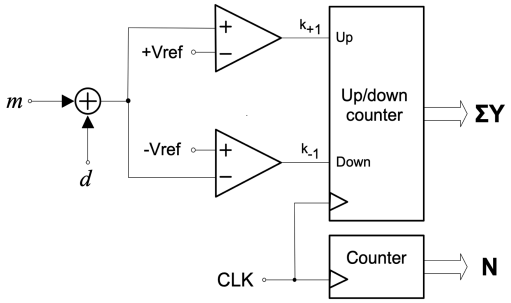

Fig. 3. Two bit ADC with dither to measure a signal over an interval [16].

If $m = f(t)$ and d contains a uniform distribution of amplitudes, the measured value over an interval $[t_1, t_2]$ is [16]

$$\overline{Y} = \frac{1}{(t_2 - t_1)} \cdot \int_{t_1}^{t_2} f(t) \cdot dt. \quad (1)$$

Expression (1) is derived from the expectation of a random variable Y while considering the probability distribution of the two added signals, m and d. A practical version of (1) is obtained by dividing the value of two counters,

$$\overline{Y} = \frac{1}{N} \cdot \sum_{i=1}^{N} Y_i. \quad (2)$$

To ensure the proper accuracy of the instrument, 12 bit digital-to-analog converters are used to generate dither, establishing the distribution and amplitude properties of d [16]. In this paper, the use of MTJs as dithering circuits is proposed, reducing the complexity while providing a nearly all-digital alternative for the circuit shown in Fig. 3.

B. MTJ-based two bit stochastic additive ADC

Applying a voltage across an MTJ induces the VCMA effect – modulation of the magnetic anisotropy which aids in switching the magnetization state [17-20]. In Fig. 4, the energy landscape for an MTJ with two perpendicular equilibrium states is illustrated. An energy barrier E_b along the in-plane axis separates these two states. A positive voltage lowers the energy barrier between the two magnetization states of the free layer, increasing the likelihood of thermal fluctuations inducing switching.

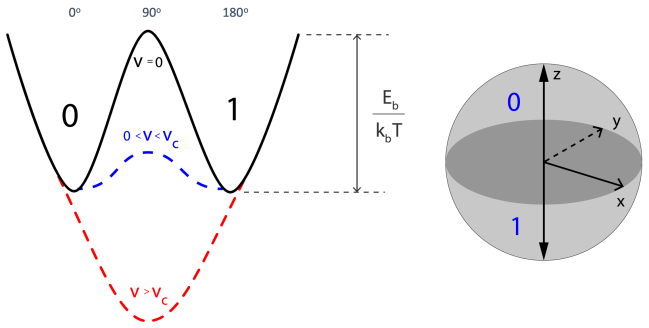

Fig. 4. Effect of an applied voltage on the energy barrier between two magnetization states of an MTJ.

An applied electric field affects the thermal stability Δ of an MTJ [18],

$$\Delta(V) = \frac{E_b - {}^{\xi AV}/_{t_o}}{k_B T}, \tag{3}$$

where V is the voltage applied across the MTJ, ξ is the VCMA coefficient, A is the cross sectional area of the MTJ, t_o is the oxide thickness, k_B is the Boltzmann constant, and T is the temperature. An increase in the voltage above a certain limit V_c changes the energy barrier, creating a new energy minimum in the intermediate state (at 90°). The critical voltage V_c is determined by setting (3) to zero [21],

$$V_c = \frac{t_o k_B T}{\xi A} \Delta(V = 0). \tag{4}$$

Utilizing the stochastic behavior induced by the VCMA effect to apply dither modifies the circuit shown in Fig. 3 to the circuit shown in Fig. 5. The input voltage $V_{in}(t)$ switches the magnetization of the free layer of the two MTJs, each MTJ with a different switching probability, which is set by the two bias voltages. Transistors T7 and T8 form a voltage divider with resistances of M1 and M2, enabling the read operation [22]. The state of the two MTJs – 1 being the high (antiparallel) resistance state, and 0 being the low (parallel) resistance state – are detected by sense amplifiers and passed to the counter. The counter enumerates the number of 1's from both MTJs: the high resistance state from M1 increments the counter, whereas the high resistance state from M2 decrements the counter. A ring counter can be used to generate the timing conditions of the MSADC, as shown in Fig. 6.

The operation of the MSADC is based on the dependence of the switching probability on the applied voltage and the stochastic behavior induced by thermal noise. The MSADC should therefore operate in the thermally activated regime (as shown in Fig. 4), placing a limit on the maximum amplitude of the input signal,

$$V_{bias1} - V_c \leq V_{in} \leq V_c + V_{bias2}. \tag{5}$$

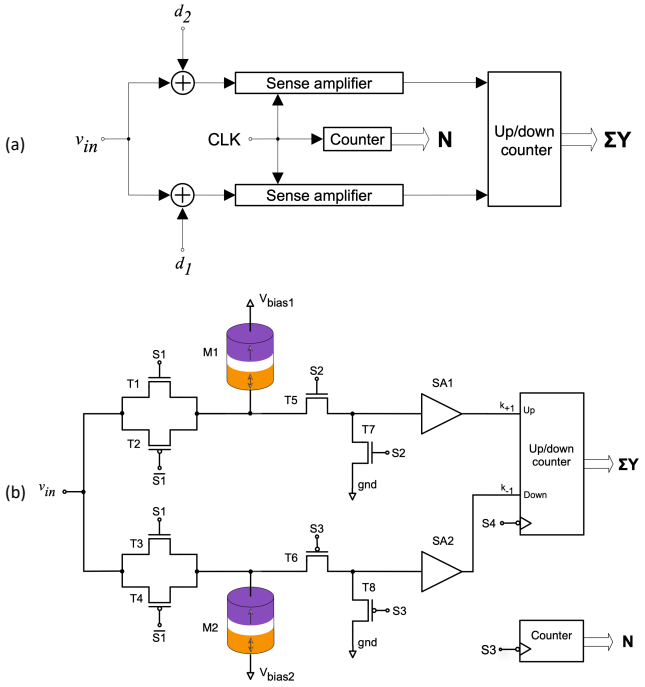

Fig. 5. MTJ-based two bit ADC with added dither. (a) Block diagram of the MSADC. Dithering signals d_1 and d_2 are added to the input signal. (b) Circuit schematic of the MSADC. The high resistance states from the MTJs, M1 and M2, are used to, respectively, increment and decrement the counter.

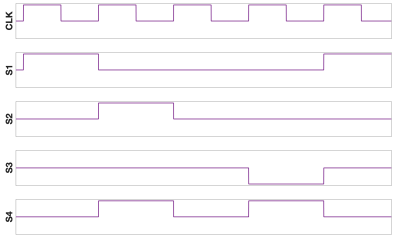

Fig. 6. Timing diagram of the MSADC.

IV. Simulation Results and Discussion of the MSADC

Proper operation of the MSADC is achieved by applying a positive bias voltage to M1 and a negative bias voltage to M2. In this configuration, the positive input voltage increases the energy barrier between the two magnetization states of M1 while lowering the energy barrier between the two states of M2, as described in Section III-B. The probability of switching M2 therefore increases while the probability of switching M1 is reduced. In a similar manner, a negative voltage applied at the input reduces the switching probability of M2 and increases the switching probability of M1. The counter within the MSADC (see Fig. 5) is incremented when M1 is in a high resistance state and decremented when M2 is in a high resistance state, to reflect the increase and decrease in the input voltage. Adjusting the bias voltages affects the probability of switching the MTJs, changing the properties of the MSADC. This behavior is evaluated by SPICE simulations of the MSADC including an MTJ compact model [23]. The properties of the distribution of the output of the two MTJs are shown in Fig. 7.

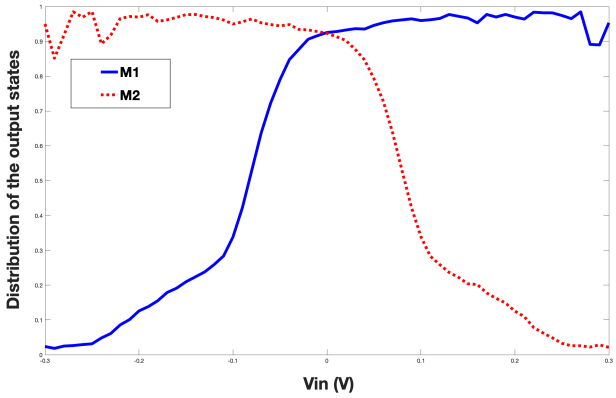

Fig. 7. Distribution of output of two MTJs for different voltage levels. The bias of the MTJs is V_{bias1} = 1.38 volts and V_{bias2} = -1.38 volts.

The distribution of output states is determined by the number of high resistance states – *i.e.,* ones – measured for different input voltages over a time interval divided by the number of measurements during that interval. For high input voltages for M1 and low input voltages for M2, the function stops behaving monotonically, degrading the linearity of the ADC. This behavior deterioriates the accuracy of the measurement, confirming the need to set a limit on the input voltage, as described by (5).

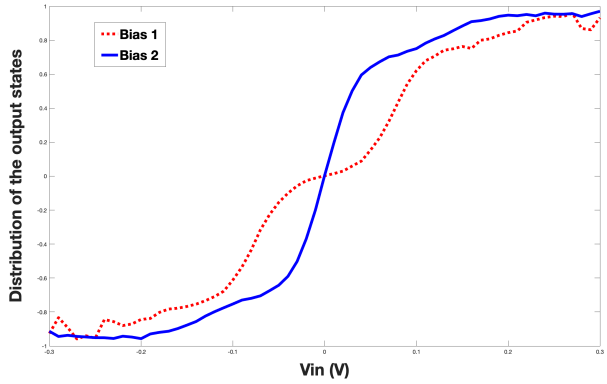

Fig. 8. Combined distribution of output of two MTJs for different MTJ bias voltages. Bias 1: V_{bias1} = 1.38 volts, V_{bias2} = -1.38 volts. Bias 2: V_{bias1} = 1.45 volts, V_{bias2} = -1.45 volts.

The output of the counter reflects the combined distribution of the output of the two MTJs. This output can be mapped to the corresponding mean value of the input voltage by including a multiplicative factor. The distribution resulting from the combined effect of the two MTJs, configured as illustrated in Fig. 5(b), is shown in Fig. 8. The dotted line corresponds to the bias configuration illustrated in Fig. 7. Adjusting the bias voltage of the two MTJs affects the switching probability, flattening the curve of the combined distribution, as illustrated by the solid line shown in Fig. 8. The resulting distribution is approximately linear around zero over a certain range of input voltage amplitudes. In this range, the output is mapped to the corresponding measured value by a linear transformation, decreasing the complexity of the measurement algorithm. To achieve this distribution, however, the bias voltage of M1 is increased, and the bias voltage of M2 is decreased. It can be concluded from (5) that this reduction in complexity requires a reduced range of measured voltages.

An example of the behavior of this circuit configuration, for an offset sinusoidal input voltage, is shown in Fig. 9, illustrating the dithering effect of the two MTJs. The number of ones at the output of the MTJs follows the previously described distribution of output states, tracking the input voltage waveform.

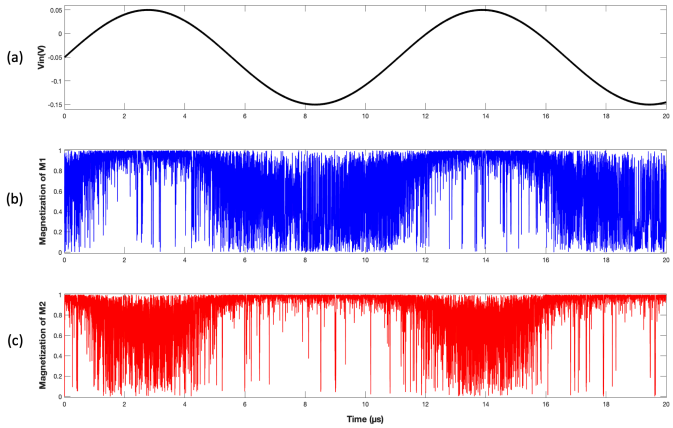

Fig. 9. Magnetization switching of the two MTJs within the MSADC for a 90 kHz sinusoid with a negative offset. (a) Input voltage. (b) Switching of M1. (c) Switching of M2.

The accuracy of the measurement can also be improved by increasing the number of samples. Either extending the measurement interval or increasing the sampling frequency will achieve this objective. The sampling frequency is limited by the clock frequency and the speed of switching the free layer magnetization - on the order of GHz at the current state of technology [23]. This circuit can be used to measure the integral of the signals at frequencies up to ~100 kHz. The MSADC is small, fast, and energy efficient. Due to the nature of the output which provides values of 1, 0, and -1, simple mathematical operations are enabled, reducing the complexity of certain logic functions. The small size and low complexity enable the use of the MSADC as an analog-to-information converter and for multi-channel IoT measurements.

V. Conclusions

A novel application of MTJs for generating dither in a stochastic additive two bit ADC is presented in this paper. Simulation results show that this circuit enables low power measurement of the integral (*i.e.,* mean) of a signal over a low frequency range – up to 100 kHz. The information describing the mean value of the input signal is produced by sampling over a time interval and utilizing the inherent property of stochastic magnetization switching of an MTJ operating under the VCMA effect. The effective resolution of the ADC increases with the length of the time interval. This MTJ-based ADC is almost fully digital and can be used as an analog-to-information converter.

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