Superconductive Logic Using $2\phi-$Josephson Junctions with Half Flux Quantum Pulses

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***Abstract*—Superconductive logic based on Josephson junctions (JJ) is a promising technology for energy efficient supercomputers and cloud computing. This technology can deliver significant improvements in performance and energy efficiency as compared to CMOS. Superconductive circuits, however, suffer from low density integration as compared to CMOS, primarily due to the limited scalability of the inductors. To improve the scalability of superconductive logic, a logic family based on a novel JJ technology, 2ϕ-JJ, has been proposed that eliminates the inductors. In this paper, three circuits are presented which exploit this scalable inductor-less technology. This novel 2ϕ-JJ technology represents the data as half flux quantum (HFQ) pulses, which improves the energy efficiency and speed as compared to standard superconductive logic such as rapid single flux quantum (RSFQ). Unlike RSFQ, the proposed circuits dynamically switch upon receiving an HFQ pulse, saving energy. These 2ϕ-JJ logic circuits operate 2.25X faster and require 2.6X less energy as compared to RSFQ.**

I. Introduction

Demand for energy efficient computation is growing, particularly for exascale supercomputers and cloud computing. A potential technology to achieve energy efficient, high performance computing is superconductive technology [1]. Rapid single flux quantum (RSFQ) [2], energy efficient RSFQ (ERSFQ) [3], and energy efficient single flux quantum (eSFQ) [4] are examples of energy efficient, high performance superconductive logic families. RSFQ circuits have been experimentally demonstrated to operate at frequencies up to 770 GHz [5] with die-to-die communication of more than 100 Gbit/s [6], [7]. The information in RSFQ circuits is represented as a voltage pulse with a quantized area equal to a single flux quantum (SFQ), $\Phi_0 = \frac{h}{2e}$. A logic 1 is characterized by the existence of an SFQ pulse while logic 0 is the absence of a pulse. The duration of an SFQ pulse can be as fast as 2 ps with a voltage magnitude of 1 mV, as illustrated in Fig. 1.

RSFQ circuits are primarily composed of Josephson junctions (JJs) and inductors. A significant drawback of RSFQ circuits is limited improvement in density due to the inability to scale inductors in modern superconductive fabrication technologies [8]. To improve density, superconductive circuits without inductors have been proposed [8]. These inductor-less circuits use a novel JJ called 2ϕ-JJ. Although the 2ϕ-JJ passes half flux quantum (HFQ) pulses, SFQ pulses are used at the input and output of the logic gate.

2ϕ-JJ circuits produce, transmit, and represent data by HFQ pulses. Combining 2ϕ-JJs with standard JJs allows the proposed circuit technology to be scalable since inductors are not used. Several logic circuits, a Josephson transmission line (JTL), an inverter, and an OR gate, are proposed. Energy efficiency improvements of 2.6X and speed improvements of 2.25X as compared to RSFQ logic are achieved.

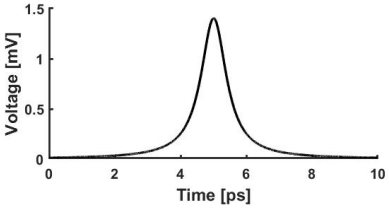


Fig. 1: Single flux quantum pulse representing a logical 1.

II. Behavior of Josephson Junction

The dynamic behavior of standard JJs and 2ϕ-JJs is explained, respectively, in Sections II-A and II-B.

A. Standard Josephson Junctions

A JJ is a multilayer device composed of a superconductive layer (S), an insulating layer (I), and a second superconductive layer (S). The JJ is described by the following expressions,

$$I = I_c \sin(\phi), \tag{1}$$

$$\frac{d\phi}{dt} = \frac{2e}{\hbar} V, \tag{2}$$

where I is the current in the JJ, I_c is the critical current of the JJ, ϕ is the phase difference between the superconductive layers, e is the electron charge, $\hbar$ is the Planck constant divided by 2π, and V is the voltage across the device.

From (1) and (2), the energy-phase relationship (EPR) of a junction is

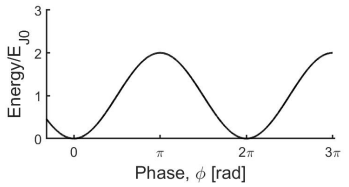
$$E_J = E_{J0}(1 - \cos(\phi)), \tag{3}$$

$$E_{J0} = \frac{\hbar I_c}{2e}. \tag{4}$$

The minimum energy of the junction occurs at a $2\pi n$ phase difference ($0,\ 2\pi,\ 4\pi\ \ldots$), where n is an integer, as depicted in Fig. 2a.

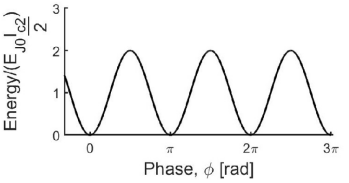
The JJ can be represented by a resistively and capacitively shunted junction (RCSJ) model [9], as illustrated in Fig. 3. Based on the RCSJ model, (1), (2), and Kirchoff's current law, the current of a JJ is

$$I = I_c \sin\phi + \frac{1}{R}\frac{\hbar}{2e}\frac{d\phi}{dt} + C\frac{\hbar}{2e}\frac{d^2\phi}{dt^2}. \tag{5}$$

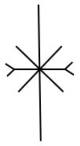


(a) Normalized EPR of a standard JJ.

(c) JJ symbol.



(b) Normalized EPR of a 2ϕ-JJ.



(d) 2ϕ-JJ symbol [8].

Fig. 2: Energy-phase relation, (a) standard JJ, and (b) 2ϕ-JJ. Symbol, (c) standard JJ, and (d) 2ϕ-JJ.

Applying a current greater than the critical current produces an SFQ voltage pulse, switching the phase of the junction by 2π.

B. 2ϕ-Josephson Junction

A JJ topology composed of a ferromagnetic (F) layer with a one spin active interface rather than an insulating layer exhibits a current-phase relationship (CPR) with a dominant second harmonic [10]–[14]. Robust junctions with a purely second harmonic [12], [15] have been experimentally demonstrated. Junctions with a second harmonic exhibit a CPR of

$$I = I_{c_1} \sin(\phi) + I_{c_2} \sin(2\phi), \tag{6}$$

and an EPR of

$$E = I_{c_1}(1 - \cos(\phi)) + \frac{I_{c_2}}{2}(1 - \cos(2\phi)), \tag{7}$$

where E is normalized by the Josephson energy E_{J0}, and I_{c_1} and I_{c_2} are the amplitude of each harmonic.

Junctions with a purely second harmonic are called 2ϕ-JJs. Unlike standard JJs, these junctions exhibit a minimum energy at a πn phase difference, as illustrated in Fig. 2b. 2ϕ-JJs can be modeled using the same RCSJ model with a supercurrent, as described in (6). Based on the RCSJ model and solving (5) for a 2ϕ-JJ, the 2ϕ-JJ switches when a π phase difference occurs, producing an HFQ voltage pulse. The HFQ pulse is half the area of an SFQ, and is produced when a junction switches by π rather than 2π. Unlike RSFQ, information in the proposed logic circuits is transmitted and stored as an HFQ pulse, which is more energy efficient than an SFQ pulse. The energy required for a standard JJ to switch by 2π is $E \approx \Phi_0 I_c$, while switching a 2ϕ-JJ by π requires half of this energy.

III. Logic Circuits Based on 2ϕ-JJs

In this section, three logic circuits based on 2ϕ-JJs and standard JJs are proposed. The primary constraint in these circuits is that the phase within each superconductive loop must sum to $2\pi n$ $(\ldots -2\pi, 0, 2\pi \ldots)$, a fundamental requirement in superconductive loops. If the phase of the junctions does not add to $2\pi n$, a circulating current is produced to add or subtract the phase of the junctions until a phase of $2\pi n$ is achieved.

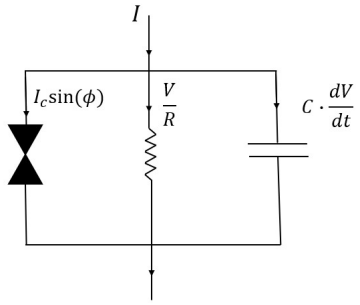


Fig. 3: RCSJ model of a JJ. The current passing through a device is composed of a superconductive current, a resistive current, and a capacitive current.

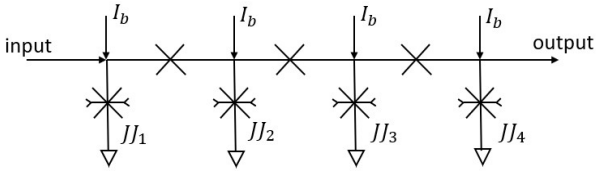


Fig. 4: Proposed multistage JTL based on 2ϕ-JJs. The inductors are replaced with standard JJs.

RSFQ logic gates are DC powered, individually clocked, and all of the junctions require a bias current below the critical current I_c. The characteristics of the proposed 2ϕ-JJ logic gates are similar to RSFQ gates. The proposed circuits contain 2ϕ-JJs based on π phase switches. Standard JJs behave as an impedance and do not switch. This trait adds design complexity but enhances the energy efficiency and replaces the inductors. The following subsections introduce the three proposed circuits and operating principles along with simulations illustrating the circuit functionality.

A. Josephson Transmission Line (JTL)

The function of a JTL is as a local interconnect to connect nearby logic gates. The output of a logic gate is connected to the input of another logic gate by one or more JTLs [16]. In RSFQ circuits, a JTL stage is composed of two JJs connected by an inductor. In this proposed JTL circuit, two 2ϕ-JJs are connected by a standard JJ rather than by an inductor. The proposed circuit is illustrated in Fig. 4.

The circuit functions as follows. An HFQ pulse is received at the input; accordingly, a current pulse enters the circuit. Most of the current passes through the initial 2ϕ-JJ, JJ_1, since the first standard JJ is in a high impedance state. The phase of JJ_1 switches by π, propagating a current pulse through the standard JJ and switching the second 2ϕ-JJ, JJ_2. Each 2ϕ-JJ produces a current pulse which switches the following 2ϕ-JJ. After the pulse is transferred from the input to the output, the phase of each 2ϕ-JJ switches by π, as illustrated in Fig. 5. The inputs in Fig. 5 are modeled as an HFQ pulse; a triangular voltage pulse with an area of $\frac{\Phi}{2}$. The switching behavior of the JJ_1 switch is therefore different from the following JJs.

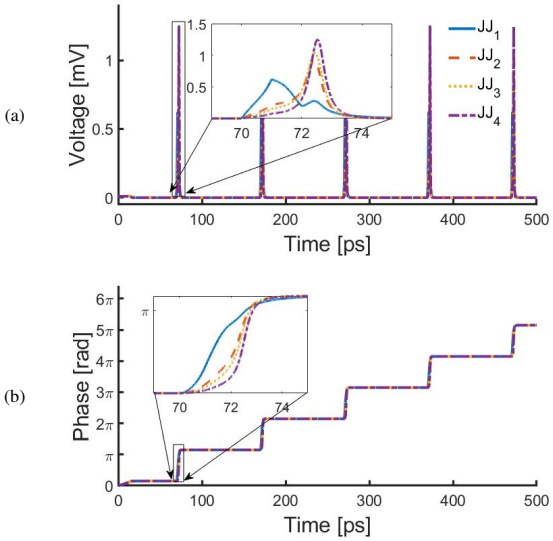


Fig. 5: JTL circuit behavior, (a) voltage pulse, and (b) phase switch.

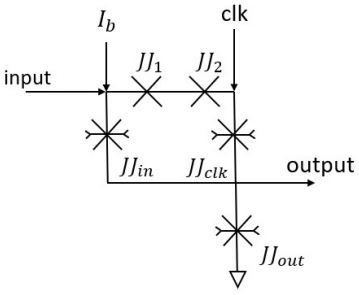


Fig. 6: 2ϕ-JJ inverter.

B. Inverter

The proposed inverter is a superconductive loop composed of two 2ϕ-JJs and two standard JJs. The additional 2ϕ-JJ, below the superconductive loop, is an output JJ, which produces and sends an HFQ pulse to the next logic gate. A schematic of the proposed inverter is shown in Fig. 6.

Once an HFQ pulse arrives at the input, most of the current proceeds through JJ_{in} since the two serially connected JJs impose a high impedance on the current, switching JJ_{in} by π. Two serial JJs are used because one standard JJ in the loop will not hold the HFQ pulse. A large circulating current would have been produced and switched JJ_{clk} to acquire a phase of 2π. However, with two serial JJs, a smaller circulating current is produced in loop $(JJ_{in} - JJ_1 - JJ_2 - JJ_{clk})$ which increases the phase of $(JJ_1 - JJ_2 - JJ_{clk})$, acquiring a total phase in the loop of 2π. The arrival of an HFQ pulse at the clock input switches the phase of JJ_{clk}. Once JJ_{clk} switches, the superconductive loop supports a total phase of 2π, π each from JJ_{in} and JJ_{clk}, resetting the loop back into the initial state without a circulating current. For a logical 1 input, an output pulse is not produced by the inverter; logic 0 is effectively produced. When an HFQ pulse arrives at the clock terminal without a preceding pulse at the input, the phase of JJ_{out}, rather than the phase of JJ_{clk}, switches by π since the bias current through JJ_{out} is greater than JJ_{clk}. The voltage and phase of the proposed inverter are shown in Fig. 7. An output pulse is not produced when a preceding input pulse is acquired.

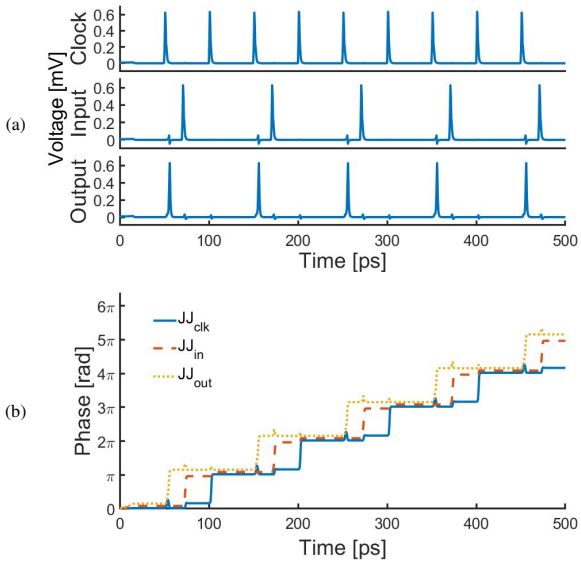


Fig. 7: Proposed inverter, (a) voltage, and (b) phase.

C. OR Gate

The proposed OR gate consists of two superconductive loops, each containing a single 2ϕ-JJ and three standard JJs with a single output 2ϕ-JJ below the two loops. A schematic of the OR gate is shown in Fig. 8.

In addition to the OR gate shown in Fig. 8, a JTL stage is also shown, drawn as a dashed line. The last stage JTL in the clock input includes a 2ϕ-JJ, unlike input1 and input2 which are connected by a standard JJ. When an HFQ pulse reaches the clock input without a preceding pulse from input1 or input2, the phase of JJ_{clk} switches by π. This switching event prevents the pulse from propagating to either of the loops or to the output, producing a logic 0 output. When an HFQ pulse enters input1, the phase of JJ_{in1} switches by π. After the junction switches, a circulating current is produced in loop $(JJ_3 - JJ_{in1} - JJ_2 - JJ_1)$ to increase the phase of the other JJs until a phase of 2π is achieved. Two serial JJs hold the HFQ pulse within the loop and impose a high impedance on the input current pulse. Once the clock pulse arrives, the phase of JJ_{in1} switches to 0 since the current in JJ_{in1} is greater than the current in JJ_{clk}. Due to JJ_{in1} switching, a current pulse propagates towards the output, switching JJ_{out} and generating an HFQ pulse, a logic 1. After JJ_{in1} switches, the phase of the $(JJ_3 - JJ_{in1} - JJ_2 - JJ_1)$ loop returns to zero. No circulating current exists, and the circuit returns to the initial state. When a symmetric HFQ pulse is passed from input2, the same functionality is achieved at the output. When an HFQ pulse arrives at both inputs, the phase of JJ_{in1} and JJ_{in2} switches by π. Upon application of a clock input pulse, the clock switches JJ_{in1}, which produces a current pulse switching JJ_{in2} to 0. Another current pulse is generated, switching

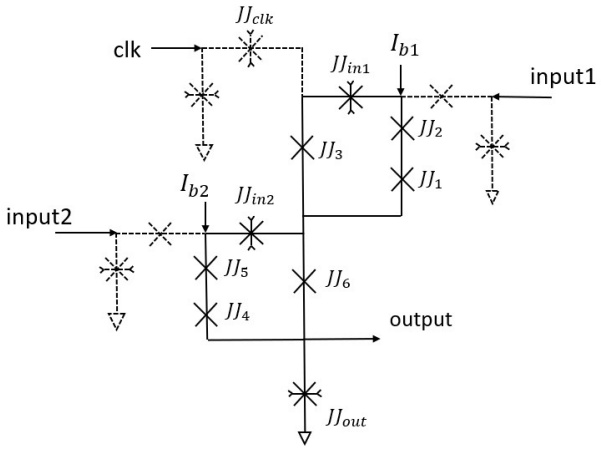


Fig. 8: 2ϕ-JJ OR gate. The dashed lines represent the JTL stage.

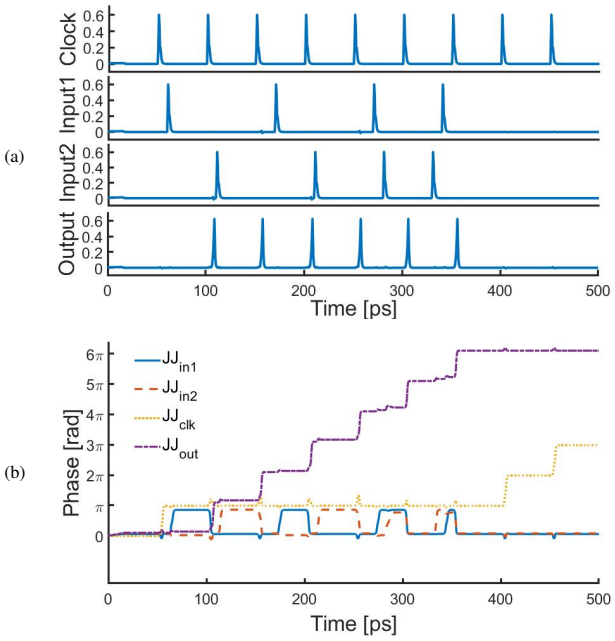


Fig. 9: Proposed OR gate, (a) voltage, and (b) phase.

JJ_{out} by π, passing an HFQ pulse (logic 1). Simulations of the OR gate are shown in Fig. 9.

IV. Evaluation of Latency and Energy

The proposed $2\phi-$JJ circuits and logically equivalent RSFQ circuits have been simulated in Cadence Virtuoso. The RSFQ circuits are from the SUNY RSFQ cell library [17]. For the standard JJ device, Whiteley Research open source Verilog-A code is used [18]. The 2ϕ-JJ circuits are modeled by revised Verilog-A code which behaves according to (6). A comparison between the proposed π circuits and conventional RSFQ circuits is listed in Table I. The critical current for the 2ϕ-JJs ranges between 100 μA and 220 μA, and for standard JJs between 100 μA and 250 μA. This provides a fair comparison between the logic circuits since the energy is linearly dependant on the critical current of the JJ.

TABLE I:
Latency and Energy Consumption of Logic Gates

JTL		Latency [ps]		Energy [zJ]	
In	Out	RSFQ [17]	2ϕ-JJ	RSFQ [17]	2ϕ-JJ
0	0	-	-	0	0
1	1	6.9	4	1499	705
Inverter		Latency [ps]		Energy [zJ]	
In	Out	RSFQ [17]	2ϕ-JJ	RSFQ [17]	2ϕ-JJ
0	1	4.5	2	389	110
1	0	-	-	698	268
OR Gate		Latency [ps]		Energy [zJ]	
In1	In2 Out	RSFQ [17]	2ϕ-JJ	RSFQ [17]	2ϕ-JJ
0	0 0	-	-	460	45.7
0	1 1	10	2.5	1506	253
1	0 1	10	3.5	1505	296
1	1 1	8	1.5	1824	400

A. Latency

Latency is the difference in time between the arrival of an output pulse upon the arrival of an input clock pulse. The latency of a three stage JTL is the difference between the input pulse and output pulse of four 2ϕ-JJ JTLs, as shown in Fig. 4. If the circuit does not produce an output pulse, the latency is undefined and the output does not change. The latency of the proposed π gates and logically equivalent RSFQ gates is listed in Table I. The proposed π-JTL, inverter, and OR gate are faster by 1.72X, 2.25X, and 2.85X, respectively, than the equivalent RSFQ JTL, inverter, and OR gate.

B. Energy

The energy of the circuits is determined by integrating the power consumed by each junction. The results, listed in Table I, are the energy consumed during one clock cycle for different input combinations. The JTL energy is for four junctions, as shown in Fig. 4, since no clock is used. The proposed π JTL, inverter, and OR gate are, respectively, 2.12X, 2.6X, and 4.5X more energy efficient than the equivalent RSFQ circuits. A lower critical current for the 2ϕ-JJ circuits would further improve the energy efficiency.

V. Conclusions

2ϕ-JJ logic eliminates the need for inductors, improving the inherent scalability of superconductive circuits. 2ϕ-JJs also enable HFQ data transmission and storage rather than SFQ for greater energy efficiency. The logic state is represented as an HFQ pulse rather than an SFQ pulse, saving energy. The first work to propose superconductive logic circuits based on this innovative 2ϕ-JJ technology with HFQ pulses is presented in this paper. Simulations show that the proposed π logic gates are 2.25X faster and require 2.6X less energy as compared to conventional RSFQ logic circuits. Further investigation into 2ϕ-JJ devices and circuits is necessary to enhance the scalability, speed, and energy of superconductive digital systems.

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