Double Magnetic Tunnel Junction-Based Nonvolatile Logic

Abdelrahman G. Qoutb, *Student Member, IEEE* and Eby G. Friedman, *Fellow, IEEE*

***Abstract*—In exascale computing, a huge amount of data is processed in real-time. Conventional CMOS-based computing paradigms follow the read, compute, and write back mechanism, which consumes significant power and time to compute and store data. *in situ* computation - where data are processed within the memory system - is considered a platform for exascale computation. A spin transfer torque perpendicular magnetic tunnel junction (PMTJ) is a nonvolatile memory device with several potential advantages (fast read/write, high endurance, and CMOS compatibility) to become a next generation memory solution. PMTJ offers the possibility of constructing both standalone and embedded RAM as well as MTJ-based VLSI computing. The double magnetic tunnel junction (DMTJ) is an emerging device composed of two serially connected PMTJs. In this paper, a DMTJ-based multi-bit memory cell that also provides a nonvolatile logic compute capability is presented. The multi-level cell provides both a high speed read/write multi-bit memory cell and a nonvolatile AND, OR, and NOT logic gate that computes and stores input data in real-time with a delay of 70 ns in a 32 nm CMOS technology node.**

***Index Terms*—STT, MTJ, *in situ* computing, SOT, memristor, PMTJ, MRAM, MLC**

I. INTRODUCTION

Many integrated systems have become data centric, where huge amounts of data are collected and processed in real-time. In data centric architectures, data motion is greatly decreased by integrating the computational process within the storage system at different levels of the memory and storage hierarchy. This capability for *in situ* computation can be achieved by exploiting an emerging memory technology that exhibits two modes of operation within the same platform, memory and compute.

The classical von Neumann separation between memory and computing expends significant energy and space. These systems are volatile and leak significant current. Non-volatile memory (NVM) technologies have been proposed to replace CMOS memory within different parts of the memory hierarchy. Some of these NVM solutions support in-memory computing, such as memristor-based logic [1]–[3] and spintronic-based compute-in-memory [4]–[7]. Memristors exhibit a low endurance rate (up to 10^{10} cycles [8]) as compared to the high endurance characteristics of spintronic systems (10^{15} write cycles [9]). This higher endurance makes spintronic memristors an effective solution for in-memory compute applications.

This research is supported in part by the National Science Foundation under Grant No. CCF-1716091, intelligence advanced research projects activity (IARPA) under Grant No. W911NF-17-9-0001, and by grants from Qualcomm and Synopsys.

A. G. Qoutb and E. G. Friedman are with the Department of Electrical and Computer Engineering, University of Rochester, Rochester, NY 14627 USA (e-mail: a.qoutb@rochester.edu, friedman@ece.rochester.edu)

Magnetic random access memory (MRAM) is a spintronic NVM considered a potential universal solution at all memory levels [10]. This breadth is supported by the development of multiple magnetic memory technologies, serving each level of the memory hierarchy [10]. Most MRAM solutions are based on a perpendicular MTJ (PMTJ) with spin transfer torque (STT). This technology has attracted considerable attention due to the high endurance rate, fast switching, CMOS compatibility, simple device structure, and ability to scale to sub-10 nm dimensions [11]. STT MRAM, however, requires a high critical current density to switch a device. Consequently, the memory cell is scaled to satisfy both density and power demands. These PMTJ devices, however, suffer from aging and low endurance. Hence, a multi-level cell is proposed here to further increase memory density. A double magnetic tunnel junction (DMTJ) is a multi-level STT PMTJ cell composed of two serially connected PMTJ devices, and exhibits four stable resistance states.

In this paper, the DMTJ structure is combined with CMOS to provide a hybrid multi-bit memory cell and a nonvolatile logic element. This logic element is based on the state diagram and physical operation of the DMTJ device. The contribution described in this paper is due to two aspects. First, a write circuit for the DMTJ-based STT PMTJ is proposed. Second, a nonvolatile AND, OR, and NOT logic gate based on the multi-level MTJ is presented. The paper is organized as follows. In Section II, the structure and physical model of the DMTJ are described. The proposed write circuit for a DMTJ-based multi-bit memory cell is presented in Section III. The operating mechanism of a DMTJ as a nonvolatile AND, OR, and NOT gate is presented in Section IV. Simulation results are presented in Section V. The paper is concluded in Section VI.

II. MULTI-LEVEL STT-MRAM CELL

An STT PMTJ multi-level cell is non-volatile [12] and exhibits a fast read/write time. The simple cell structure requires only two additional mask steps to integrate the STT storage elements into a logic compatible CMOS process [13]. A compact model capturing the static and dynamic behavior of a perpendicular magnetic anisotropy MTJ, including the influence of the device dimensions and temperature on the perpendicular magnetic anisotropy of a PMTJ, is used here [14], [15].

A DMTJ is a multi-level STT PMTJ cell composed of two serially connected PMTJ devices. The two PMTJs share the same characteristics but have different diameters, as shown in Figure 1. Each PMTJ exhibits two stable resistance states, parallel (0) and antiparallel (1), whereas the DMTJ exhibits four different resistance states, represented as R_{00}, R_{01}, R_{10},

978-1-6654-8485-5/22/$31.00 ©2022 IEEE

and R_{11}. The MSB represents the state of the large PMTJ (PMTJ2), and the LSB represents the state of the small PMTJ (PMTJ1). In the R_{01} state, PMTJ2 operates in the parallel state, and PMTJ1 operates in the antiparallel state. Since PMTJ2 has a larger diameter than PMTJ1, PMTJ2 exhibits a lower resistance than PMTJ1. Consequently, PMTJ2 requires a greater current than PMTJ1 to switch between the parallel and antiparallel states.

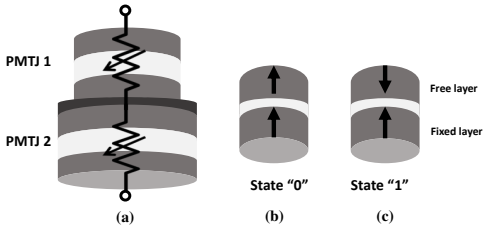


Fig. 1: Multi-level STT MRAM cell composed of two serially connected PMTJs, (a) two PMTJs connected in series modeled as a variable resistance based on the state of operation, (b) state "0" when the magnetization state of the free and reference layer is in parallel, and (c) state "1" when the magnetization state is in the antiparallel state.

The resistance-current characteristic of a DMTJ based on two serially connected STT PMTJs is shown in Figure 2, indicating the four resistance states of the DMTJ and the critical current at which each PMTJ switches. The performance and reliability of a DMTJ cell are sensitive to CMOS and MTJ device variations and thermal induced randomness. To avoid a read failure (an overlapping distribution of resistances), the size of each PMTJ within the DMTJ is critical. The distribution density of the four resistance states in a DMTJ, shown in Figure 3, is based on Monte Carlo simulations of process and temperature variations within a DMTJ device.

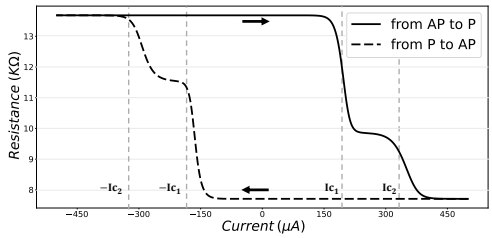


Fig. 2: AP-P transition and P-AP transition of a DMTJ. The vertical axis is the resistance of the DMTJ at 0 volts, and the horizontal axis describes the current to switch a DMTJ

A state flow diagram of a DMTJ is shown in Figure 4, where $+I_{c2}$ and $-I_{c2}$, are, respectively, the current to switch the PMTJ2 between the parallel and antiparallel state, and I_{c1} is the current to switch PMTJ1 between the parallel and antiparallel state. I_{c2} is larger than I_{c1}. In the following section, a multi-bit hybrid MTJ/CMOS memory and logic cell is proposed. The circuit requires a two step write scheme.

III. DMTJ STT PMTJ as a Multi-bit Memory Cell

To employ a DMTJ as a multi-bit memory cell, the cell should supply bidirectional current and exhibit two different

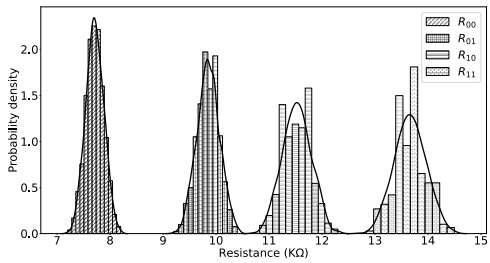


Fig. 3: Monte Carlo simulation of the four state resistance distributions of a DMTJ with process and temperature variations.

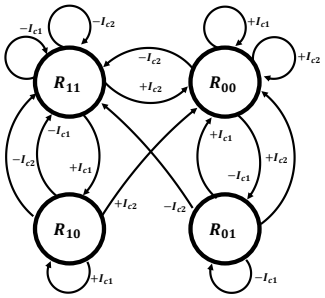


Fig. 4: State flow diagram of a DMTJ with two serially connected PMTJs. The device provides four resistance states and switches between states based on the applied current.

current levels. A circuit commonly known as an H-bridge [16] (see Figure 5(a)) was modified to achieve the write capability of the DMTJ. When switch S_0 is closed, the current supplied to the DMTJ is in the opposite direction than when switch S_1 is closed. The H-bridge has been previously adopted to switch an STT-based MTJ, while in this paper, an H-bridge circuit is modified to switch a DMTJ, as discussed later in this section.

Based on the current resistance state, a DMTJ transitions to another state in one step except for the transition between the R_{01} and R_{10} resistance states, as illustrated in the state diagram of a DMTJ shown in Figure 4. A reset step is initially required, followed by a write step. Since a sense step is not used before the write operation, a one step process writes the R_{00} or R_{11} state by applying, respectively, a high positive current pulse or a negative current pulse. The two step write process consists of a *reset* step and a *write* step to produce the other two resistance states of the DMTJ. The write and logic operations of a DMTJ are described in the following subsections.

A notation is used to represent the current supplied to a DMTJ, as follows: I_{00} represents $+I_{c2}$, I_{01} represents $+I_{c1}$, I_{10} represents $-I_{c1}$, and I_{11} represents $-I_{c2}$. The MSB is the direction of the current, positive if zero and negative if one, and the LSB represents the current magnitude, where zero is less current and one is more current. A hybrid CMOS/MTJ multi-bit memory circuit is illustrated in Figure 5(b) where I_1 and I_0 represent, respectively, the MSB and LSB of each current notation. As an example, if I_{00} is the applied circuit, $I_0 = 0$ and $I_1 = 0$. Hence, the top left CMOS network operates with the bottom right CMOS network. En_W enables the write operation, and En_S enables the sense operation.

Each switch of the write circuit shown in Figure 5(a) utilizes a CMOS network to source the critical current to

switch a DMTJ. The right side of the branch includes only one transistor; therefore, if $I_1 = 1$, two CMOS transistors are connected in series with the DMTJ. These transistors are small, providing low current to the DMTJ, sufficient to switch the small PMTJ. If both $I_1 = 1$ and $I_0 = 1$, both sides of the CMOS network produce a large current. Note that the left side transistors within the CMOS network are larger than the right side transistors to source this larger current. The size of the CMOS networks is critically dependent on the four resistance states within the DMTJ and the critical current to switch the PMTJs within the DMTJ.

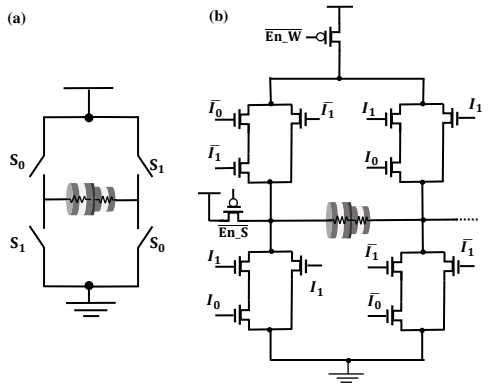


Fig. 5: Multi-bit DMTJ memory cell, (a) H-bridge circuit for bidirectional current supply. Switches S_0 and S_1 control the direction of the current within the DMTJ. (b) Proposed hybrid CMOS/DMTJ memory cell, where En_W enables the write operation, En_S enables the sense operation, and I_0 and I_1 controls, respectively, the magnitude and direction of the current supplied to the DMTJ.

IV. DMTJ STT PMTJ AS AND, OR, AND NOT LOGIC GATE

A DMTJ operates as a non-volatile logic cell in addition to a multi-bit memory cell. The behavior of a DMTJ operating as a nonvolatile logic element is illustrated in the state flow diagram shown in Figure 4. The DMTJ is treated as a state machine with two one bit inputs and four states. The two one bit inputs, I_1 and I_0, refer, respectively, to the direction and magnitude of the supplied current. The four states refer to the four resistance states of a DMTJ. The truth table of a DMTJ, as a state machine, is listed in Table I. S_1 and S_0 represent, respectively, the present state of the large PMTJ and small PMTJ, and $S_1^{'}$ and $S_0^{'}$ represent, respectively, the future state of the large PMTJ and small PMTJ.

The boolean representation of the future state bits, $S_0^{'}$ and $S_1^{'}$, in terms of the current state of a DMTJ and input current bits, illustrated in Figure 6, is, respectively,

$$S_0^{'} = I_1 \tag{1}$$

$$S_1^{'} = I_1 I_0 + S_1 I_0 + S_1 I_1. \tag{2}$$

A DMTJ transitions into a non-volatile state once a current is applied. The future memory state of a DMTJ is represented by $S_0^{'}$ and $S_1^{'}$, where $S_0^{'}$ and $S_1^{'}$ are, respectively, the future state of the small PMTJ and large PMTJ. Based on (1), $S_0^{'}$ cannot

Table I: Truth table of a DMTJ as a state machine

S_1	S_0	I_1	I_0	$S_1^{'}$	$S_0^{'}$
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	0	0
0	1	0	1	0	0
0	1	1	0	0	1
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	1	1	0
1	0	1	0	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	0	1	1	0
1	1	1	0	1	1
1	1	1	1	1	1

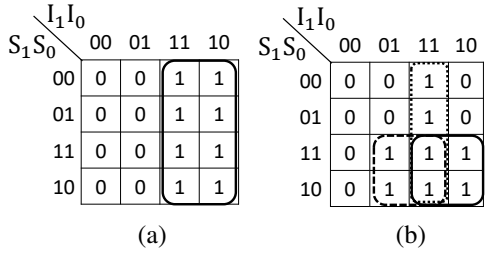


Fig. 6: Karnaugh map of the future state bits of a DMTJ, (a) $S_0^{'}$, and (b) $S_1^{'}$

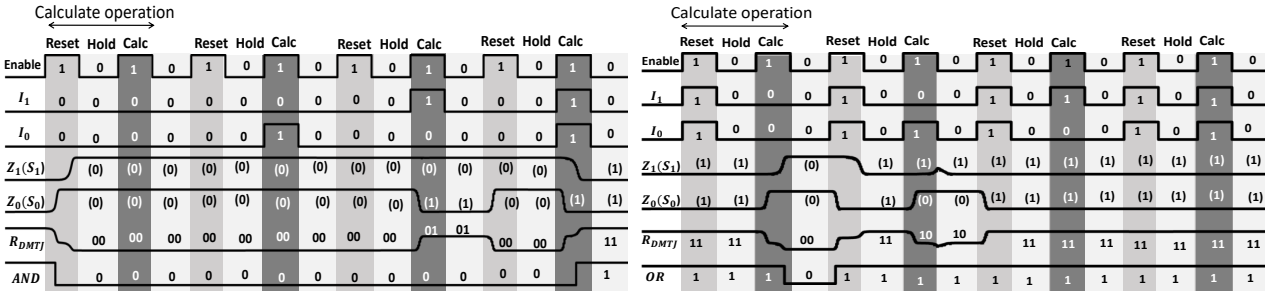
represent a logical operation of the input bits. However, as described by (2), $S_1^{'}$ is the logical computation of the input bits which can produce a logic family through the following relationship: When $S_1 = 0$, $S_1^{'} = I_1 I_0$; hence, the future memory state of the large PMTJ is the AND operation between the two input bits, I_1 and I_0. When $S_1 = 1$, $S_1^{'} = I_1 I_0 + I_0 + I_1$. $S_1^{'}$ is therefore the OR output of I_1 and I_0.

Accordingly, a DMTJ operates as an AND gate when the device is initially reset to the state where $S_1 = 0$, such as R_{00} or R_{01}. The input to the AND gate is I_1 and I_0, and the output is stored in the large PMTJ. To operate a DMTJ as an AND gate, the DMTJ is reset to the R_{00} state since only one pulse is required to set the PMTJs into this state.

To configure a DMTJ as an OR gate, the DMTJ device is initially reset to the state where $S_1 = 1$ such as R_{11} or R_{10}. The output of the OR operation is stored within the large PMTJ. The R_{11} state is chosen as a *reset* state when a DMTJ behaves as an OR gate since the R_{11} state can be written by the one pulse write scheme.

The DMTJ can be realized as a NOT gate by storing the input signal within a DMTJ; hence, the output of the NOT gate can be achieved by a CMOS inverter. To operate the DMTJ as a NOT gate, the device is initially reset to the R_{11} state, followed by a *calculate* state where the input is applied to the I_1 node, and I_0 is set to zero. Based on (2), where $S_1 = 1$ and $I_0 = 0$, $S_1^{'} = I_1$. An inverter is hence connected at the output of PMTJ1 to produce an inverted version of the input data signal.

The primary advantage of the proposed system lies in the ability to perform a logical operation and store the result concurrently as a non-volatile memory state. The proposed logical operation of a DMTJ is supported by the same memory system without requiring any additional circuitry. The oper-



(a) (b)

Fig. 7: Simulation of a DMTJ behaving as a nonvolatile DMTJ logic gate, (a) AND gate, and (b) OR gate. Enable is the control signal, I_0 and I_1 are the inputs, Z_0 and Z_1 are, respectively, the perpendicular magnetization of the small PMTJ and large PMTJ, S_0 and S_1 are, respectively, the corresponding state of the small PMTJ and large PMTJ, and R_{DMTJ} is the change in the resistance of the DMTJ

ational mechanism and simulation of a DMTJ behaving as a multi-bit memory cell and a nonvolatile logic element are described in the following section.

V. Operational Mechanism and Simulation Results

In the proposed work, a DMTJ is treated as a state machine, where the next state of a DMTJ is based on the input current and the present state of the DMTJ. The input current is based on the input bits, and the output is stored within the DMTJ in a nonvolatile state. The operation of a DMTJ as a memory element and a nonvolatile logic element is based on a macrospin model of a DMTJ composed of two serially connected STT PMTJs with a diameter of, respectively, 30 nm and 40 nm. A 32 nm predictive technology model is used to characterize the CMOS transistors [17]. The CMOS transistors are sized to provide sufficient current to switch each PMTJ based on inputs I_1 and I_0. The size of the CMOS transistors and the diameter of the two PMTJs are critical since the greater the size of a PMTJ, the lower the resistance and the larger critical current required to switch the DMTJ cell.

The proposed DMTJ-based two bit memory cell and non-volatile logic is illustrated in Figure 5(b) where the write operation is controlled by the enable write signal En_W. En_W supports two modes of operation. When $En_W = 1$, the circuit operates in the write mode and current is produced. When $En_W = 0$, the circuit operates in the *hold* mode with no supply current, hence the DMTJ is set in a stable state. The pulse width of the *write* and *hold* time signals is carefully chosen. Limitations of the *write* and *hold* time are governed by the influence of the spin transfer torque on the PMTJ. The wider the pulse of the supply current, the less critical current required to switch the PMTJ. Any limitations on the write pulse width are due to the worst case write scenario (the write signal only switches the smaller PMTJ, not the larger PMTJ). The width of the minimum write pulse is chosen to switch the smaller PMTJ, while the width of the maximum write pulse is set to not switch the larger PMTJ.

The direction and magnitude of the supplied current are, respectively, controlled by I_1 and I_0. Z_0 and Z_1 are, respectively, the orientation of the perpendicular magnetization of PMTJ1 and PMTJ2 within the DMTJ. The pinned ferromagnetic layer of the DMTJ is magnetized in the positive z direction (pointing up). As an example, if Z_0=1, then PMTJ1 is in the parallel state with S_0=0. A minimum and maximum write pulse of, respectively, 25 ns and 35 ns is required to write a state within a DMTJ. A minimum hold time of 10 ns is required once each *write* state is set to ensure the device remains in a stable state.

Operating a DMTJ as a non-volatile logic element is achieved in two steps. A *reset* state is initially written into the DMTJ based on the logical operation, the R_{00} state for an AND operation and the R_{11} state for an OR operation. This step is followed by the *calculate* state, where the logical operation is computed in real-time, and the non-volatile state is stored within the DMTJ. A waveform of a DMTJ-based AND gate and OR gate is shown, respectively, in Figures 7(a) and 7(b).

A critical current of approximately 100 μA and 140 μA is required to switch, respectively, the smaller and larger STT PMTJs. Significant development has recently been achieved to decrease the critical current required to switch an STT PMTJ. These approaches primarily use 1) low damping materials for the thick free layers [18], and 2) new composites (such as MgO_xN_{1-x}) as a tunnel barrier to overcome inter-layer diffusion [19]. These developments in STT PMTJ memory are producing higher switching speeds, greater endurance, and lower critical currents.

VI. CONCLUSIONS

In this work, the DMTJ is proposed as a multi-bit memory element and as a nonvolatile logic element. A hybrid CMOS/DMTJ circuit supports nonvolatile logic operations. In the proposed work, the DMTJ is treated as a state machine, where the next state of a DMTJ is based on the input current and the present state of the DMTJ. The DMTJ is reset to an initial state followed by a calculate state. The output of the logical operation is stored as a nonvolatile state within the DMTJ. The DMTJ behaves as a nonvolatile AND, OR, and NOT logic gate with a delay of 70 ns for a 32 nm CMOS technology node. The multi-bit memory cell exhibits an access time of 35 ns with a one step write scheme to write either the R_{00} state or R_{11} state, and 70 ns for a two step write scheme to write either the R_{01} state or R_{10} state.

REFERENCES

[1] S. Kvatinsky, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-Based Material Implication (IMPLY) Logic: Design Principles and Methodologies," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 10, pp. 2054–2066, October 2013.

[2] H. Li, T. F. Wu, S. Mitra, and H. . P. Wong, "Resistive RAM-Centric Computing: Design and Modeling Methodology," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 9, pp. 2263–2273, June 2017.

[3] Y. Zhou, Y. Li, L. Xu, S. Zhong, H. Sun, and X. Miao, "16 Boolean Logics in Three Steps With Two Anti-Serially Connected Memristors," *Applied Physics Letters*, vol. 106, no. 23, p. 233502, June 2015.

[4] Y. Pan *et al.*, "A Multilevel Cell STT-MRAM-based Computing In-Memory Accelerator for Binary Convolutional Neural Network," *IEEE Transactions on Magnetics*, vol. 54, no. 11, pp. 1–5, July 2018.

[5] R. Zand, A. Roohi, D. Fan, and R. F. DeMara, "Energy-Efficient Nonvolatile Reconfigurable Logic Using Spin Hall Effect-Based Lookup Tables," *IEEE Transactions on Nanotechnology*, vol. 16, no. 1, pp. 32–43, January 2017.

[6] L. Wang *et al.*, "Voltage-Controlled Magnetic Tunnel Junctions for Processing-In-Memory Implementation," *IEEE Electron Device Letters*, vol. 39, no. 3, pp. 440–443, March 2018.

[7] T. Hanyu *et al.*, "Standby-Power-Free Integrated Circuits Using MTJ-Based VLSI Computing," *Proceedings of the IEEE*, vol. 104, no. 10, pp. 1844–1863, September 2016.

[8] K. M. Kim *et al.*, "Voltage Divider Effect for the Improvement of Variability and Endurance of TaO_x Memristor," *Scientific Reports*, vol. 6, no. 1, pp. 1–6, February 2016.

[9] J. J. Kan *et al.*, "A Study on Practically Unlimited Endurance of STT-MRAM," *IEEE Transactions on Electron Devices*, vol. 64, no. 9, pp. 3639–3646, August 2017.

[10] X. Fong, Y. Kim, R. Venkatesan, S. H. Choday, A. Raghunathan, and K. Roy, "Spin-Transfer Torque Memories: Devices, Circuits, and Systems," *Proceedings of the IEEE*, vol. 104, no. 7, pp. 1449–1488, April 2016.

[11] K. Watanabe, B. Jinnai, S. Fukami, H. Sato, and H. Ohno, "Shape Anisotropy Revisited in Single-Digit Nanometer Magnetic Tunnel Junctions," *Nature Communications*, vol. 9, no. 1, pp. 1–6, February 2018.

[12] K. Lee *et al.*, "1Gbit High Density Embedded STT-MRAM in 28nm FDSOI Technology," *Proceedings of the IEEE International Electron Devices Meeting*, pp. 2.2.1–2.2.4, December 2019.

[13] Y. Chih *et al.*, "13.3 A 22nm 32Mb Embedded STT-MRAM with 10ns Read Speed, 1M Cycle Write Endurance, 10 Years Retention at 150°C and High Immunity to Magnetic Field Interference," *Proceedings of the IEEE International Solid-State Circuits Conference*, pp. 222–224, February 2020.

[14] H. Wang, W. Kang, Y. Zhang, and W. Zhao, "Modeling and Evaluation of Sub-10-nm Shape Perpendicular Magnetic Anisotropy Magnetic Tunnel Junctions," *IEEE Transactions on Electron Devices*, vol. 65, no. 12, pp. 5537–5544, November 2018.

[15] S. Prajapati, S. Verma, A. A. Kulkarni, and B. K. Kaushik, "Modeling of a Magnetic Tunnel Junction for a Multilevel STT-MRAM Cell," *IEEE Transactions on Nanotechnology*, vol. 18, pp. 1005–1014, October 2018.

[16] A. Skirda, E. Tokhtuev, C. Owen, and V. Slobodyan, "H-Bridge Control Circuit," U.S. Patent No. 12/370,362, August 2010.

[17] "Predictive Technology Model (PTM)." [Online]. Available: http://ptm.asu.edu/

[18] N. Perrissin *et al.*, "A Highly Thermally Stable Sub-20 nm Magnetic Random-Access Memory Based on Perpendicular Shape Anisotropy," *Nanoscale*, vol. 10, no. 25, pp. 12 187–12 195, May 2018.

[19] M. G. Moinuddin, A. H. Lone, S. Shringi, S. Srinivasan, and S. K. Sharma, "Low-Current-Density Magnetic Tunnel Junctions for STT-RAM Application Using MgO_x N_{1-x} ($x = 0.57$) Tunnel Barrier," *IEEE Transactions on Electron Devices*, vol. 67, no. 1, pp. 125–132, January 2020.