Converter Topologies for On-Package Voltage Stacking

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***Abstract*—The rise of mobile technologies and cloud computing has increased the importance of energy consumption. On-package voltage stacking, where current is recycled between multiple cores, is a potentially effective solution to this growing issue. Two converters, a load-to-load ladder buck converter and a bus-to-load isolated resonant converter, are particularly appropriate for on-package voltage stacking. A four core system composed of either converter topology is evaluated under several current mismatch scenarios in terms of transient and DC voltage drops, voltage ripple, settling time, and power efficiency. The load-to-load buck converter exhibits higher power efficiency and smaller transient voltage drops as compared to the bus-to-load resonant converter. The resonant converter is lower cost, smaller in area, and provides isolation.**

***Index Terms*—Voltage stacking, current recycling, differential power processing, microprocessor power supplies, DC-to-DC converters, voltage regulation**

I. Introduction

Performance and energy use, particularly with the importance of cloud computing and mobile technologies, are limited by the power consumption and power density of the processors. Semiconductor scaling requires a substantially smaller supply voltage. Parallel computing, in the form of multicore processors, has now become a standard approach to lower energy use [1]. According to the 2020 International Roadmap for Devices and Systems [2], power dissipation is the primary limitation of multicore processor performance due to higher ambient on-chip temperatures.

Higher levels of parallelism and lower voltages require larger voltage conversion ratios and supply currents, posing challenges on the overall power management system and, in particular, increasing losses within the off-chip power delivery system [3]. On-chip converters, alternatively, suffer from low efficiency at high conversion ratios. For example, a 4-to-1 conversion ratio requires high quality on-chip capacitors and inductors [4]–[7]. One approach to tackle this issue is voltage stacking, where the cores are serially connected [8]–[10]. For the same power, the voltage across serially connected loads is larger and the supplied current is smaller as compared to a parallel configuration connecting the same cores [11].

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Voltage stacking, also described as current recycling, has generally been applied to small mismatches in the current, where the loads consume almost 50% of the current [1], [12], [13]. A significant mismatch in the current at one load is assumed here to be ten times larger than the current on the main bus, much greater than is typically considered. The converters, placed at the package level, compensate for these differences in the load current. Furthermore, if the load changes within a short time interval, a transient voltage drop with a longer transition time is produced within the other cores. To improve the performance of the converter under this condition, two topologies are proposed.

While many topologies can be used in voltage stacking, certain types of converters are preferable. Linear dropout (LDO) regulators, for instance, dissipate significant power [14], [15] similar to other linear regulator type converters. A switched-capacitor (SC) converter occupies large area [16]–[18] at the high mismatch currents considered here, and are mostly suitable for higher voltage and lower power applications similar to other converters which rely on an electric field to store energy. Unlike these two converter types, converters which rely on a magnetic field for energy storage are more suitable, as these converters provide high efficiency and relatively small area in high current applications. Additionally, these converters need to be bidirectional to both pass and remove excess current. Two promising converter topologies for voltage stacking which meet these requirements are considered here. These converters are the ladder buck-boost converter [1], [18] and the isolated resonant converter [19]. These converters are illustrated, respectively, in Figs. 1 and 2. A comparison of these topologies is provided in terms of transient and DC voltage drops, voltage ripple, rise time, settling time, and power efficiency.

The ladder buck-boost converter and isolated resonant converter are described in Section II. A comparison of the two converter topologies applied to current recycling is provided in Section III. Some conclusions are drawn in Section IV.

II. Converters in Voltage Stacked System

Two converters, a ladder buck-boost converter and an isolated resonant converter, are considered in this work. The topology of a ladder buck-boost converter (buck converter) is load-to-load [1], where the loads are connected to different

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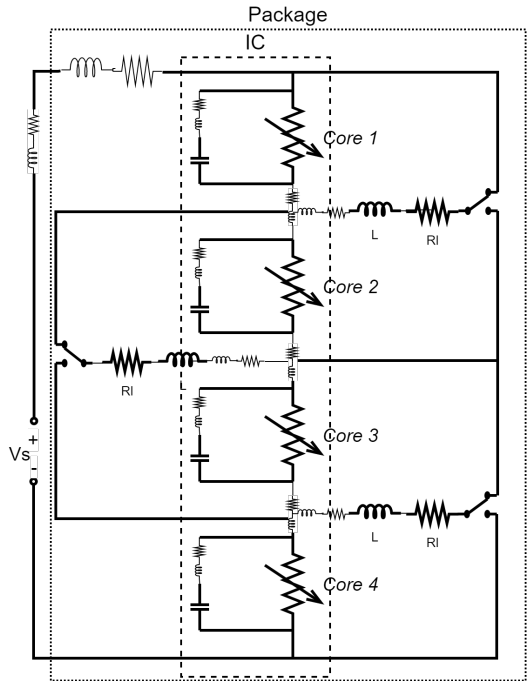

Fig. 1: Load-to-load topology based on buck converters.

TABLE I: Parameters of the four stage buck converter

N parallel phases	16
Frequency	100 MHz
On-chip capacitors	4 x 12 μF
On-package capacitors	4 x 100 μF
On-chip inductors	16 x 3 x 50 pH

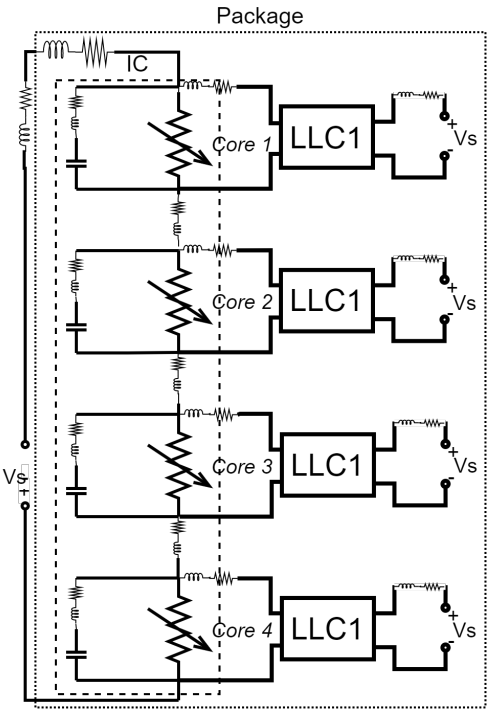

Fig. 2: Bus-to-load topology based on LLC converters.

TABLE II: Parameters of the four stage LLC converter

Parameters	**Value**
Effective series inductance, Lp	2.1 nH
Series resonant inductance, Lr	0.351 nH
Resonant capacitor, Cr	4 x 0.72 μF
Turns ratio, N	4 x 2.2

stages. In the resonant LLC converter, however, each load is managed by a separate converter. An LLC converter exhibits several advantages, such as high efficiency, high power density, and low EMI. Since each stage of a bus-to-load converter is individually connected to each of the cores, each stage is independent, as opposed to the load-to-load converter. Therefore, with a bus-to-load converter, power disturbances in one of the cores do not affect the other cores.

The simulation setup is reviewed in Section II-A. Voltage waveforms illustrating the different conditions of the buck converter and LLC converter are discussed, respectively, in Sections II-B and II-C.

A. Simulation Setup

Both multilevel converters drive four cores, modeled as a variable resistor. Each core consumes a steady state current of 8 amperes at 0.8 volts. To evaluate changes in the current consumption of each core, the current in one core is increased over a 10 ns time interval. The change in current being considered ranges between 2X to 10X, up to 80 amperes. The voltage drop, voltage ripple, and power consumption are evaluated in Matlab Simulink [20].

The load-to-load buck converter is depicted in Fig. 1. The specifications of the converter are listed in Table I. The LLC converter is illustrated in Figs. 2 and 4. The parameters of the isolated resonant converter are listed in Table II.

B. Output Voltage Waveforms of the Load-to-Load Converter Topology

Voltage waveforms of the serially stacked cores connected to a load-to-load ladder buck-boost converter (across each core in Fig. 1) are illustrated in Fig. 3. The current within core 2 is increased ten times, from 8 amperes to 80 amperes at t = 2 µs. The voltage within core 2 drops to approximately 750 mV, while the voltage in the other cores experience a short rise in voltage. The voltages subsequently return to 800 mV within all of the cores due to the feedback control which adjusts the voltage by the width of the switching pulse.

C. Output Voltage Waveforms of the Bus-to-Load Converter Topology

The current consumption of the bus-to-load LLC converter is increased from 8 amperes to 80 amperes within a single core at $t = 20$ µs. A voltage waveform across each core (see

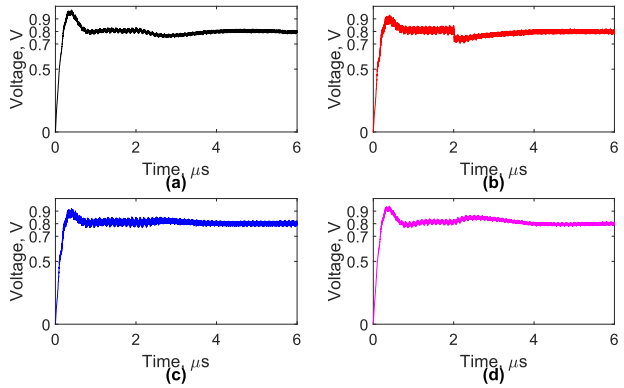

Fig. 3: Voltage waveform of each core within a four core, serially stacked system with a load-to-load buck converter. The current consumed by core 2 is increased from 8 amperes to 80 amperes at 2 μs. Voltage in a) core 1, b) core 2, c) core 3, and d) core 4.

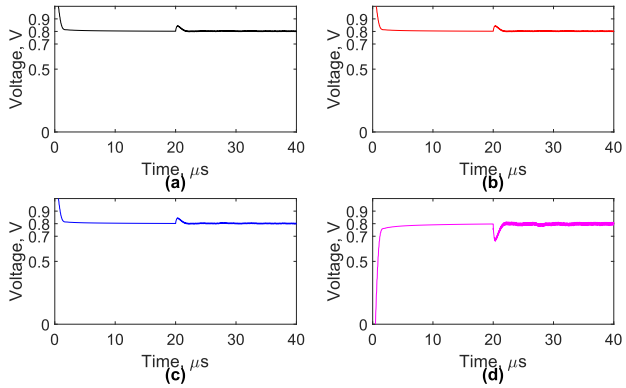

Fig. 5: Voltage waveform of each core within a four core, serially stacked system with the bus-to-load LLC converter. The current in core 4 is increased from 8 amperes to 80 amperes at 20 μs. Voltage in (a) core 1, (b) core 2, (c) core 3, and (d) core 4.

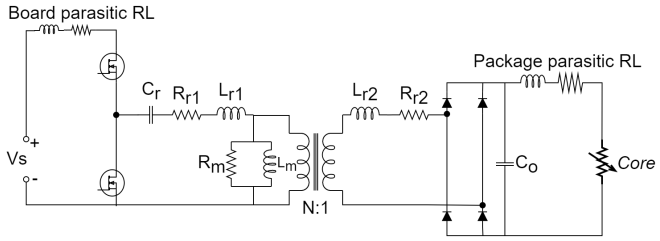

Fig. 4: Single LLC converter connected to a core.

Fig. 4) is depicted in Fig. 5. A transient voltage drop of 130 mV is observed in core 4 with a ten times increase in current. The voltage in the other cores simultaneously rise during the settling time. The voltages are subsequently adjusted by the feedback mechanism to maintain an output voltage of 0.8 volts.

III. Comparison of Converters

A performance comparison of both configurations is described in this section. The voltage drop and power efficiency for different scenarios are discussed in the following subsections. The transient voltage drop across both converter topologies is described in Section III-A, while the power efficiency of both systems are compared in Section III-B. Some general comments are offered in Section III-C.

A. Transient and DC Voltage Drop

The transient voltage drop in both systems is shown in Figs. 6 and 7. The voltage drop across the buck converter for both scenarios is similar, where the current increases in core 2 (scenario A) and core 4 (scenario B). In this configuration, the voltage drop ranges up to 55 millivolts (for a ten times increase in current). A maximum transient drop below 7% over a settling time of 0.1 μs is exhibited. The voltage drop of the LLC converter is, however, more than twice as high, ranging up to 130 millivolts. Up to a 16% drop in voltage over 2 μs is noted. Also note that the voltage drop is linearly related to the increase in load current.

B. Power Efficiency

Although switching regulators ideally consume no power, practical DC-DC converters dissipate power due to the non-ideal characteristics of the circuit elements. The power efficiency of a four core, serially stacked system with a load-to-load buck converter and bus-to-load LLC converter for different unbalanced conditions is compared. The efficiency of the buck converter and LLC converter for different current conditions is depicted, respectively, in Figs. 6 and 7. As noted in these figures, the power efficiency of the load-to-load buck converter is higher under all conditions. The power efficiency of the buck converter ranges from 88% to 94%, while the LLC converter ranges from 71% to 89%.

C. General Comments

Other performance characteristics of the converters, such as the transient and DC voltage drop, voltage ripple, and settling time after the change in current is completed, are summarized in Table III. The efficiency of the load-to-load buck converter is higher than the bus-to-load LLC converter, while the transient voltage drop and voltage ripple are lower. Additionally, the settling time of the buck converter is shorter than the settling time of the LLC converter. Considering these characteristics, the performance of the load-to-load synchronous buck converter is superior to the buck-to-load LLC converter when used as an interface between cores in a voltage stacked system. However, since the load-to-load buck converter consists of 16 parallel phases and the bus-to-load LLC converter only requires a single phase, the cost of the bus-to-load LLC converter is significantly less. Additionally, the LLC converter consists of a capacitor, transformer, two switches and four diodes/switches while the buck converter consists of 48 inductors and 96 switches. The LLC converter

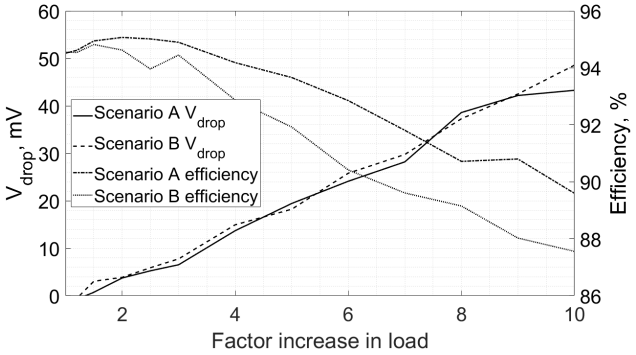

Fig. 6: Transient voltage drop and efficiency in a four core, serially stacked system with a load-to-load buck converter. The values are measured when the current in core 2 (or core 4) is two to ten times larger.

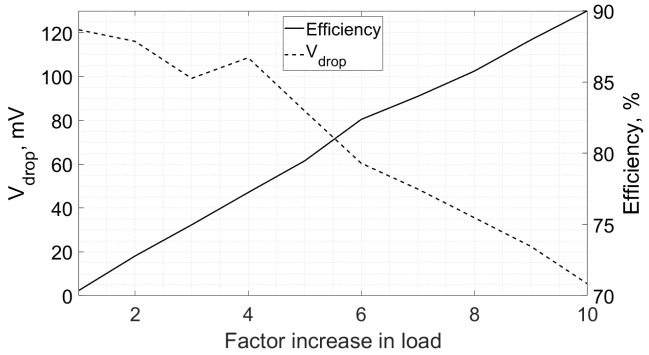

Fig. 7: Transient voltage drop and efficiency in a four core, serially stacked system with a bus-to-load LLC converter. The values are measured when the current in core 2 is two to ten times higher.

therefore requires significantly less area. Also note that an LLC converter isolates the cores from the voltage bus.

TABLE III: Comparison of the load-to-load and bus-to-load converters

	Load-to-Load Buck Converter	**Bus-to-Load LLC Converter**
Power efficiency	88%	71%
V_{drop}, transient, worst-case	55 mV	130 mV
V_{drop}, DC	0 mV	0 mV
V_{ripple}	0.1 mV	11 mV
Settling time, t	0.1 μs	2 μs
N, phases	16	1
Frequency, f	10 MHz	10 MHz
Capacitors, on-chip	4 x 12 μF	4 x 12 μF
Capacitors, on-package	4 x 100 μF	4 x 100 μF
Inductors	16 x 3 x 50 pH	4 x 1.4 nH

IV. Conclusions

The continuous scaling of semiconductors and increasing use of parallel computing have lead to higher voltage conversion ratios, larger supply currents, and greater power losses, posing significant challenges on the power management system. One solution to this growing problem is voltage stacking (current recycling) in serially stacked cores. Different mismatch conditions, up to a ten times increase in current, and two different converter configurations, load-to-load and bus-to-load, are considered. The load-to-load buck converter and bus-to-load LLC converter are evaluated for a four core system. The converters are compared in terms of transient and DC voltage drops, voltage ripple, settling time, and power efficiency. At 10 MHz, the load-to-load buck converter exhibits a minimum 88% power efficiency when the load current is increased by ten times, while the minimum efficiency of the bus-to-load LLC converter is 71%. Additionally, the transient voltage drop of the load-to-load buck converter is 58% less, the voltage ripple is 110 times smaller, and the settling time is 95% shorter than the bus-to-load LLC converter. The load-to-load buck converter, when applied to a voltage stacked system, is therefore the preferable converter topology. Nevertheless, the area and cost of the LLC converter are significantly less than the buck converter, as the LLC converter requires only one phase versus 16 parallel phases for the buck converter. Additionally, an LLC converter provides isolation between the input voltage and the cores.

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