A PARTITIONABLE CLOCK DISTRIBUTION SYSTEM FOR SEQUENTIAL VLSI CIRCUITS

Eby Friedman

Hughes Aircraft Company
6155 El Camino Real
Carlsbad, California 92008

Abstract

The primary control signal for the synchronization of sequential data is the processing clock. This signal typically constrains the performance and throughput of the entire digital system being integrated. In this paper, the synchronous clock distribution problem in VLSI and a methodology for its solution is described. A design technique which minimizes on-chip clock skew as well as providing an environment for concurrent VLSI circuit design is discussed. This approach permits the clock distribution design effort to be hierarchically partitionable among a VLSI design team without impacting chip level performance or cohesiveness.

I. Introduction

In most digital systems, the transfer of data between functional elements is synchronized by a single control signal, the processing clock. This signal typically constrains the timing and performance behavior of an entire system. Therefore, it is imperative that a design methodology exists which will permit the clock distribution system to operate as fast as possible without creating any unnecessary timing uncertainties or decreasing functional chip yield. This clock distribution design methodology must also provide an environment for hierarchical design of a VLSI circuit, thus permitting the VLSI design effort to be partitionable into smaller design problems. This paper describes a design methodology for distributing clock networks in a VLSI circuit design environment. The methodology considers all hierarchical levels of design detail and permits design of a clock distribution network that provides optimal performance, such as negligible clock skew, while still permitting the overall design problem to be functionally partitionable and therefore better suited for a multi-person design team environment.

Section II of this paper describes the requirements of a clock distribution system for a classical sequential VLSI circuit. In section III, the particular design approach of the partitionable clock distribution network is discussed while in section IV the advantages and disadvantages of this clock distribution scheme are described. Finally, in section V, some concluding comments are made describing the relative benefits of this design approach to VLSI circuits.

II. Design Requirements of a Clock Distribution System

Clock distribution systems perform the task of synchronizing the flow of data in digital systems. As a clock signal arrives at a sequential register, it triggers the data from one bank of sequential registers to the next through a combinatorial network, which performs manipulations of the data in an appropriate functional manner (see Figure 1). When designing the specific combinatorial logic resident between the sequential registers, careful attention must be paid to insure that each path's timing requirements are maintained. The delay of a specific sequential signal path consists of five factors:

1) $t_{C->Q}$ - the clock-to-Q delay of the originating register in the signal path.
2) t_{logic} - the propagation delay due to the particular RC time constants of the specific path's logic and interconnect.
3) t_{set-up} - the set-up time of the final register in the signal path.
4) t_{skew} - the time difference between the triggering edge of the processing clock presented to two different sequential registers in the signal path. A critical race condition can result if the final register clock signal significantly leads or lags the originating register clock signal.
5) $\Delta t_{r/f}$ - the additional delay of a cell due to differences in signal rise and fall times. This time delay can increase or decrease all of the above delay factors depending upon the relative transition times of the signal.

Therefore, the total propagation delay between two registers in a sequential signal path is given by equation 1.

$$t_{PD} = t_{C->Q} + t_{logic} + t_{set-up} + t_{skew} + \Delta t_{r/f} \quad (1)$$

For a design to meet its specified requirements, the largest propagation delay of any signal path being enabled by the clock system must be less than the inverse of the circuit's maximum clock frequency (equation 2) [1].

CH2255-8/86/0000-0743 $1.00 © 1986 IEEE

functional elements by parameterizing each of the functional elements' clock buffers resident in the central clock buffering circuit [1]. This assumes that the difference in parasitic interconnect impedance is sufficiently small. As shown in Figure 2, each functional element requires its own precisely tuned clock signal to minimize the variation in clock skew between each of the functional elements. Also shown, each of the functional elements are constrained to a K-stage clock distribution system, in order to ensure that each functional element is triggered by the same clock edge. Finally, the clock signal transition time seen by each on-chip sequential register should be constrained to a maximum level. This maintains the chip level integrity of each of the functional elements clock distribution systems.

Accurate resistive and capacitive interconnect parasitics at the intra-element level are extracted [9, 10] and used to characterize the interconnect impedances between the functional elements and the central clock buffer circuit. To compensate for the variation in interconnect and fanout loading of each of the functional elements, finely tuned parameterized buffers are placed within the central clock buffer circuit to drive each particular clock line. Each of these parameterized buffer cells is chosen with precisely the correct level of current drive (i.e. channel resistance) to compensate for the variation in interconnect and fanout loading that each functional element requires. Thus, the chip level clock distribution system produces extremely small clock skew across the entire chip.

The number of stages necessary to implement an optimal clock distribution system is dependent upon the fanout and interconnect loading and the application specific speed/area tradeoffs. This technique permits an optimal number of buffer stages [8, 11 and 12] to be configured hierarchically, thereby providing all the performance benefits of a carefully cascaded inverter chain while still permitting a hierarchical design team environment and minimal clock skew.

IV. Advantages and Disadvantages of the Minimal Clock Skew Design Technique

A key advantage to this design technique is in reducing clock skew. Also, overall clock delay, from the input pin to sequential register, is reduced. This occurs from improved partitioning of the RC loads. The clock buffers are physically closer to their loads, thereby minimizing the interconnect resistance of these nodes. The higher resistive intra-element interconnect drives intermediate clock buffers with relatively small capacitance. Thus, the RC time constants at both points are reduced, which reduces the overall clock delay and skew.

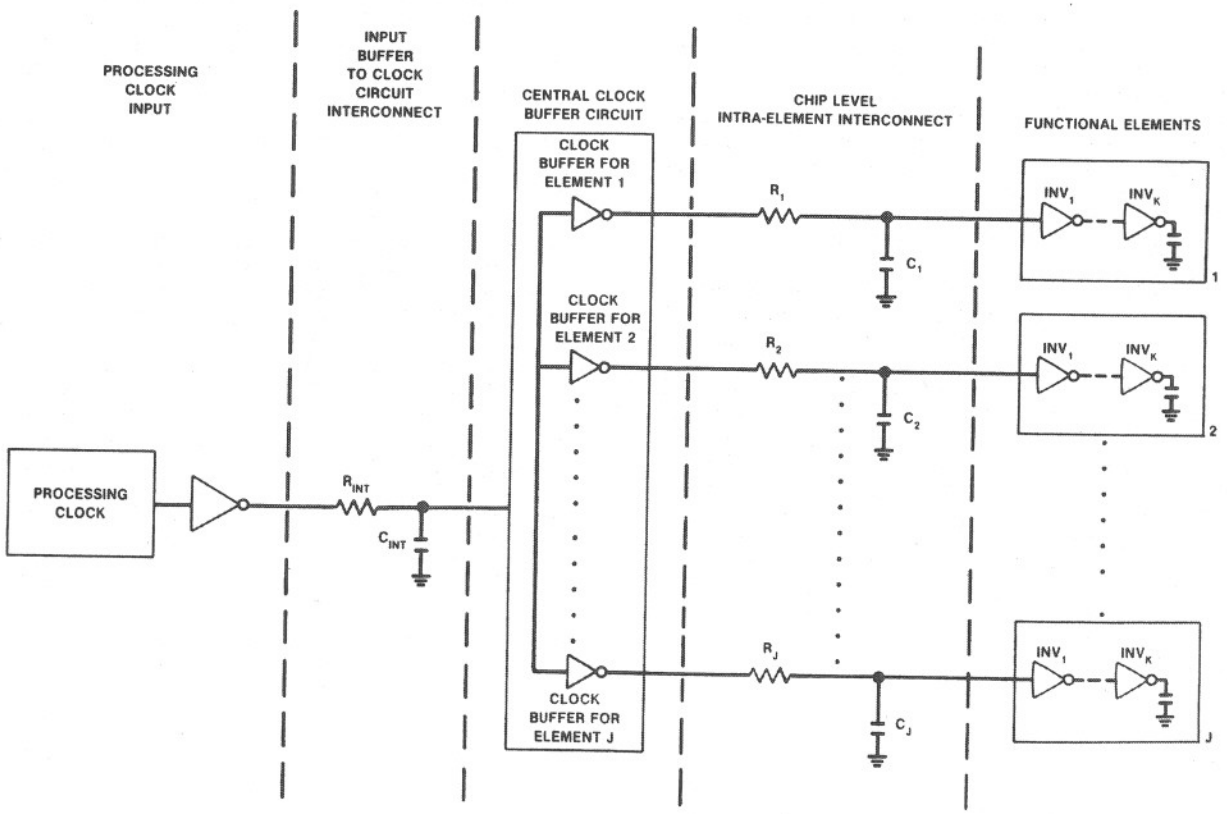

FIGURE 2. CLOCK DISTRIBUTION SYSTEM FOR MINIMAL CLOCK SKEW

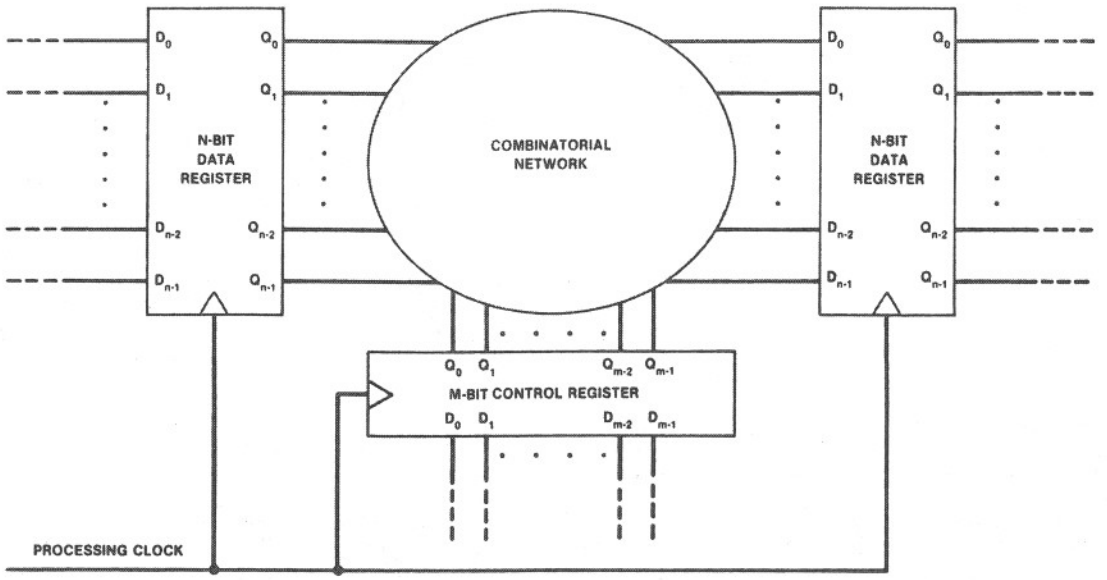

FIGURE 1. CLASSICAL SEQUENTIAL DATA FLOW

$$t_{PD_{max}} < t_{\substack{clock \\ period}} = \frac{1}{fclk} \qquad (2)$$

Therefore, in order to permit maximum performance in a VLSI circuit, special attention must be given to decreasing non-functional parasitic time delays. This is commonly exhibited within the industry by an effort to decrease parasitic device and interconnect impedances [2] common in all integrated circuits. The purpose of this paper is to describe a design technique for minimizing the clock skew in sequential VLSI circuits while still maintaining a useful design team environment. By minimizing the clock skew, the propagation delay of a path decreases, thereby permitting a higher frequency of operation and improving the data throughput of the overall system being integrated.

III. A Design Technique for Minimizing Clock Skew

When designing a clock distribution system in a VLSI circuit, it is imperative that the clock skew between each register in the circuit be limited. A common technique for equalizing the parasitic impedances between each clock branch is to use a generally symmetric organization of the clock lines (e.g. equalizing line lengths) which, to a first order approximation, equalizes the parasitic loading of each clock signal as seen by each clock buffer [1,3]. The difficulty with this technique occurs when one wants to hierarchically partition the overall chip design into separate functional elements, as is commonly done in large VLSI circuits. Ideally, each large functional element would contain its own locally optimized clock distribution system to satisfy its own particular timing constraints. However, local optimization within a functional element does not necessarily lead to global optimization of the overall chip level clock distribution system.

In many large VLSI circuits, there is a separate functional circuit which performs the clock buffering for the entire chip [4]. In a fairly large VLSI circuit, the parasitic interconnect impedances required to connect each of the functional elements to the central clock buffering circuit would be significant, as compared to its gate delays, and would vary from element to element. This variation in parasitic interconnect impedances between each of the functional elements and the central clock buffering circuit can lead to excessive chip level clock skew [1,5]. Thus, in an optimally designed VLSI circuit with significant hierarchical partitioning of the chip's functionality, a significant variation in propagation delay exists between each of the functional elements' clock signals. Therefore, a technique is needed to compensate for this variation in propagation delay between the clock lines of each of the functional elements.

As described in [6], parameterized buffer cells can be used to geometrically size an inverter to provide an appropriate level of current drive. The effective output impedance of these devices coupled with the distributed resistive and capacitive impedances of the buffer's interconnect and fanout define precisely the timing response of that logic stage [7,8]. Therefore, one can compensate for the variation of clock propagation delay between each of the

Another significant advantage in using this technique in a synchronous VLSI circuit is the ability to partition each of the functional elements among a VLSI design team. The overall chip design can be partitioned hierarchically into a manageable domain of information with an emphasis on optimal clock distribution. Each functional element's clock distribution system is therefore optimized for its particular requirements while still maintaining overall chip-level clock integrity. The usefulness of this technique is dependent upon the ability to characterize the VLSI circuit's device and interconnect impedances. Careful attention must be given to characterizing and modeling these resistances and capacitances to minimize the chip level clock skew.

Lastly, unlike interconnect impedances, transistor transconductances tend to be very sensitive to both process and environmental variations (e.g. temperature, radiation, etc.). Therefore, the performance of an optimally designed clock distribution system designed under nominal conditions would tend to fluctuate under worst case and best case conditions. In particular, a processing clock signal path whose performance is dominated by interconnect impedances changes differently than a clock signal path that is dominated by device impedances. Thus, situations occur where the absolute propagation delays of clock signals significantly decrease under best case conditions while the clock skew actually increases under these same conditions due to the greater sensitivity of one signal path as compared with another signal path to changes in device transconductance. However, for a finely tuned design where close attention has been given to reducing interconnect resistance when using this minimal clock skew technique, the effect on clock skew is fairly minimal.

V. Conclusions

An efficient design technique for a clock distribution system oriented to sequential VLSI circuits has been described. The technique can be used to minimize clock skew within a chip, thereby improving the circuit's overall performance. The design technique also provides an environment for concurrent VLSI circuit design, thereby permitting the clock distribution design effort to be hierarchically partitionable among a VLSI design team without impacting chip level performance or cohesiveness. Lastly, the technique has exhibited some sensitivity to process and environmental variations, but this effect is relatively small.

VI. Acknowledgements

The author would like to acknowledge the technical contributions of G. Yacoub, S. Powell, W. Marking, P. Pandya, L. Tsu, D. Barach, T. Cesear, and R. Rapoza. He is also extremely grateful to G. Persky for his sincere encouragement and advice in writing this paper.

VII. References

[1] D. F. Wann and M. A. Franklin, "Asynchronous and Clocked Control Structures for VLSI Based Interconnection Network," IEEE Trans. on Computers, Vol. C-32, No. 3, pp. 284-293, March 1983.

[2] A. K. Sinha, J. A. Cooper, Jr., and H. J. Levinstein, "Speed Limitations due to Interconnect Time Constants in VLSI Integrated Circuits," IEEE Electron Device Letters, Vol. EDL-3, No. 4, pp. 90-92, April 1982.

[3] S. Dhar, M. A. Franklin, and D. Wann, "Reduction of Clock Delays in VLSI Structures," International Conference on Computer Design (ICCD), pp. 778-783, October 1984.

[4] R. Woudsma and J. M. Noteboom, "The Modular Design of Clock-Generator Circuits in a CMOS Building-Block System," IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 3, pp. 770-774, June 1985.

[5] F. Anceau, "A Synchronous Approach for Clocking VLSI Systems," IEEE Journal of Solid-State Circuits, Vol. SC-17, No. 1, pp. 51-56, February 1982.

[6] E. Friedman, W. Marking, E. Iodice, and S. Powell, "Parameterized Buffer Cells Integrated into an Automated Layout System," Custom Integrated Circuits Conference (CICC), pp. 389-392, May 1985.

[7] P. Penfield, Jr. and J. Rubinstein, "Signal Delay in RC Tree Networks," 18th Design Automation Conference, pp. 613-617, June 1981.

[8] C. M. Lee and H. Soukup, "An Algorithm for CMOS Timing and Area Optimization," IEEE Journal of Solid-State Circuits, Vol. SC-19, No. 5, pp. 781-787, October 1984.

[9] S. Powell, W. R. Smith, and G. Persky, "A Parasitics Extraction Program for Closely-Spaced VLSI Interconnects," International Conference on Computer-Aided Design (ICCAD), pp. 193-195, November 1985.

[10] E. Friedman, G. Yacoub and S. Powell, "A CMOS/SOS VLSI Design System," Journal of Semicustom ICs, Vol. 2, No. 4, pp. 5-11, June 1985.

[11] H. C. Lin and L. Linholm, "An Optimized Output Stage for MOS Integrated Circuits," IEEE Journal of Solid-State Circuits, Vol. SC-10, No. 2, pp. 106-109, April 1975.

[12] R. Jaeger, "Comments on 'An Optimized Output Stage for MOS Integrated Circuits'," IEEE Journal of Solid-State Circuits (Corresp.), Vol. SC-10, No. 3, pp. 185-186, June 1975.